Hybrid DPWM with Process and Temperature Calibration

A Thesis Presented

by

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To my family.
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List of Acronyms

**PMIC**  Power Management Integrated Circuits.

**DPWM**  Digital Pulse Width Modulation.

**DC-DC**  A DC-to-DC converter is an electronic circuit which converts a source of direct current (DC) from one voltage level to another.

**CMOS**  Complementary Metal Oxide Semiconductor. Use both NMOS and PMOS to build circuits.

**PWM**  Pulse Width Modulation

**PTAT**  Proportional To Absolute Temperature

**PID**  Proportional-Integral-Derivative
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Jing Lu
Abstract of the Thesis

Hybrid DPWM with Process and Temperature Calibration

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In this thesis, a 12-bit high resolution, power and area efficiency hybrid DPWM with process and temperature calibration is proposed for DPWM controller IC for DC-DC converters. The hybrid structure of DPWM combines a 6-bit differential segmented tapped delay line structure and a 6-bit counter-comparator structure, resulting in a power and area saving solution. Furthermore, the 6-bit differential segmented delay line structure serves as the clock to the high 6-bit counter-comparator structure, thus a high frequency clock is eliminated and power is significantly saved. In order to have simple delay cell and flexible delay time controllability, voltage controlled inverter is adopted to build the differential delay cell, which allows fine-tuning of the delay time. The process and temperature calibration circuit is composed of process and temperature monitors, two 2-bit flash ADCs, and a lookup table. The monitor circuits sense the process and temperature variations, and the flash ADC converts the data into digital code. The lookup table combines both the process and the temperature digital information and provides an appropriate value to the control voltage of the differential delay cell. The complete circuits design has been verified under different corners of CMOS 0.11um process technology node.
Chapter 1

Introduction

Nowadays Power Management Integrated Circuits (PMIC) provide highly integrated, high-performance power management solutions for a wide range of applications in the automotive, consumer and industrial markets. Technological advancements and increasing demand for battery operated devices and automobiles are the major factor driving the market keep growing. Research and development on PMIC are continuously hot and demanding. Digital control implemented in switching power converter is receiving increasing attention. It offers additional advantages in system configuration, such as more flexibility and functionality. It also reduces the dependence on process technology and sensitivity to noise. However, digital approach has disadvantages such as delay and less accuracy. Therefore, a customized low power digital controlled (DC-DC) controller is becoming a hot research area this decade.

1.1 Motivation

According to the report given by Transparency Market Research \cite{1}, the PMIC market will be worth $46 billion by 2019, comparing $29.9 billion in 2012. Its application include every where of life and industry: automobile, telecommunications, networking, computing, consumer electronics, military, medical electronics and other industrial purpose \cite{1}. For such a big, strong, long-lasting market, innovation and revolution is ever requiring. There are two trends of PMIC. One is developing smaller, high efficiency, more environmental friendly product under current paradigm. The other one is exploring new, more intelligent paradigm. The emerging digital controlled DC-DC converters catering the latest trend are very promising technology for future blossom.
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Currently analog control methods are dominant of the PMIC due to their low power consumption and high level of controllability. However, analog controllers require individually tailored circuit to the specific needs, thus a relatively long design process and sometimes completely redesign procedure is needed for different product. As such, they are not suitable for monolithic integration with rapidly changing digital based product. Moreover, in the latest Complementary Metal Oxide Semiconductor (CMOS) processes, not all analog blocks can be implemented due to analog’s own performance requirement. On the other hand, digital controllers allows easier system integration and process migration. Supported by automated design tools, system redesign and expansion can be fairly easy.

Digital controllers have improved flexibility and increased functionality compared to an analog design. Analog controllers need external components to configure their loop stability and other system configuration, which will require more pins and larger application boards size. Plus external pins and components introduce more parasitic factors and noise interface. In contrast, advanced digital algorithm and computation unit that is capable of self-diagnose, estimation and auto calibrations in digital controller optimizes the system performance without external components and I/Os. Moreover, auto-tuning or online tuning features in digital controllers can handle a range of power stage parameters such as different inductor and capacitor values in one controller, which requires experienced engineer to configure an analog controller in the field. Sophisticated digital programming also enables online monitoring and communications between different controllers and system management.

On the other hand, digital controller falls short compared to the infinite-resolution and sample-free analog control. One of the setbacks of digital control is the resolution of the two main building blocks of the digital loop: ADC and DPWM. While, the conventional analog control is ideally assumed to have infinity resolution. This feature could also bring the instability due to the discrete values of duty cycle, called limit cycle, which will be further discussed in Chapter 2. Also, the sampling process adds delay to the system. This delay will add loop phase delay, which will potentially cause instability. Ten times higher than the switching frequency sampling rate is ideal to minimize the phase delay and avoid reconstruction problems.

With the structure analysis and No limit cycle criteria of DPWM controller IC for DC-DC converter in Chapter 2, one can tell that its major disadvantage is that the performance is limited by the realistic resolution of ADC and DPWM. Meanwhile, the resolution of DPWM should always be higher than that of the ADC to prevent an unstable state called limit-cycle. Therefore a high resolution DPWM is always demanded in such systems. Reference runs simulation on the
CHAPTER 1. INTRODUCTION

output precision versus the resolution of ADC and the resolution of DPWM. The result shows that the optimum precision is reached when the DPWM is 12-bit and the ADC is approximately 11-bit. Beyond this resolution, the output ripple becomes the limiting factor of the output accuracy. Although [12] successfully designed a 12-bit DPWM but the delay cell is area consuming and suffered from process and temperature variation, which will cause the switching frequency change over different process corner and external environment. The motivation of this thesis is to develop a high resolution, low area and cost DPWM with process and temperature calibration.

1.2 Contribution

The thesis proposed a 12-bit hybrid DPWM that incorporates a low 6-bit differential segmented tapped delay line structure with process and temperature calibration and a high-resolution 6-bit counter-comparator structure. Usually the delay line structure excels in its low power but occupies more silicon area. Meanwhile, the counter based structure utilizes $2^n$ times faster clock to realize n-bit resolution, which impose design stress on the high speed clock and excessive power consumption. The proposed hybrid structure combines the advantageous of the two methods and significantly counteracts their drawbacks, which makes it a promising choice. For the proposed architecture, a voltage controlled differential inverter delay cell is proposed in this paper. The differential structure can save as much as 37.5% area [12]. The proposed voltage controlled inverter is economic in size and convenience in fine-tuning of the delay time for its additional voltage control node. Furthermore, process and temperature calibration circuit are proposed to address the delay time dependency on process and temperature variation. The overall design is completed on 0.11um technology node. The simulation results shows the proposed DPWM can achieve the design goal and has good linearity.

1.3 Thesis Outline

The thesis is organized into four chapters. Chapter 1 introduces the research background and motivation, which states that high resolution low power DPWM with calibration is really a requirement and design challenge. The proposed structure is better in its simpler delay cell and calibration functionality. Chapter 2 describes the general operation of a Buck converter and provides a brief insight into traditional analog controller. More detailed analysis is written on digital controller and its limit cycle conditions. Furthermore, different structures of DPWM is summarized
CHAPTER 1. INTRODUCTION

and compared. Chapter 3 describes the operation of the proposed 12-bit hybrid DPWM Delay cell, process monitor circuit, temperature monitor circuit, ADC and look-up table are all displayed and their working principle is well explained with simulation results. Chapter 4 concludes of the thesis work and to suggestions for future work.
Chapter 2

Background

The goal of DC-DC converter is to converter an undesirable DC input to different DC voltage, with specification met requirement. LDO is good at this, but the efficiency is not good. Since the handhold electronic devices are most popular these days, how to extend the battery life and reduce the time to recharge the battery is a key problem in their power supply. Switching regulators can reach 90% peak efficiency [13], together with other efficiency improvement technology. All the switching regulators enjoy some similarities because the basic principle is to use Pulse Width Modulation (PWM) to regulate the output voltage. In this thesis, Buck converter is used as the prototype development.

2.1 Synchronous Buck Converter

The synchronous Buck converter is shown in the dot outline in Figure 2.1. It consists of two power transistors MP and MN, one inductor L and one output capacitor C. The rest of the diagram is the Buck analog controller. The control waveform is shown in Figure 2.2 [13]. When the switch is closed (on-state, VP and VN are low) for ton time, the voltage across the inductor is \( V_L = V_i - V_o \). The current through the inductor rises linearly. When the switch is open (off-state, VP and VN are high) for toff time, the voltage across the inductor is \( V_L = -V_o \). The current through the inductor decreases. In the steady state, the increase and decrease of current in inductor should be the same. Defining the switching period is T and duty ratio is D. Thus the on state equation is given as,

\[
\Delta I_{L-on} = \int_0^{t_{on}} \frac{V_L}{L}\,dt = \frac{V_i - V_o}{L} t_{on} \quad (2.1)
\]

\[
t_{on} = DT \quad (2.2)
\]
Chapter 2. Background

The off-state equation is given as,

\[ \Delta I_{L-off} = \int_{t_{on}}^{T} \frac{V_L}{L} \, dt = \frac{-V_o}{L} t_{off} \]  \hspace{1cm} (2.3)

\[ t_{off} = (1 - D)T \]  \hspace{1cm} (2.4)

Assuming that the converter operates in steady state, the energy stored in each component at the end of a commutation cycle \( T \) is equal to that at the beginning of the cycle. That means that the current \( I_L \) is the same at \( t = 0 \) and at \( t = T \). So we can write from the above equations:

\[ \frac{V_{IN} - V_{OUT}}{L} t_{on} - \frac{V_{OUT}}{L} t_{off} = 0 \]  \hspace{1cm} (2.5)

So the \( V_o \) can be written as:

\[ V_o = DV_i, D < 1 \]  \hspace{1cm} (2.6)

The most common control method, shown in Figure 2.1 is \textbf{PWM}. It is a negative feedback. First the output voltage is sensed and then subtracted from a reference voltage to establish a small error signal \( (V_e) \). This error signal is compared to the oscillator ramp signal to generate a pulse waveform, which controls the power switches. When the circuit output voltage changes, \( V_e \) also

Figure 2.1: Synchronous Buck Converter with analog PWM controller
CHAPTER 2. BACKGROUND

Figure 2.2: Buck Converter working waveform

changes and that will cause the pulse duty ratio to change. This duty ratio change always pulls output voltage back to its nominal value, thus completing the control loop.

2.2 Digital PWM Controller

The analysis in the former section demonstrates that the output of a Buck regulator is determined by the pulse width, or the duty ratio of its switching signal. The benefit of this feature is that a well-regulated Buck output can be created by use of a controller that compares the actual Buck converter output voltage with a desired value. Based on the difference between these two voltages the controller can correct the output voltage by varying the duty ratio of the switch control signal. A DPWM controller is working in the same principle but in the discrete version. The block diagram is shown in Figure 2.3

First, the sensed output is digitized and compared to the desired reference value, $V_{ref}$ in the $N_{ADC}$ bit ADC. The resulting signal, $e[n]$ is $N_{ADC}$ bit error signal. Then $e[n]$ is processed in the computation unit, where PID compensation and other advanced control algorithm can be added to modulate the controller to be more stable and smarter. The output signal is the digital duty cycle command $d[n]$. This signal has $N_{DPWM}$ bit. The DPWM is a digital-to-time converter, which will transfer $d[n]$ into a pulse signal to control the ON-OFF stage of the Buck converter, thus regulate the output voltage.
CHAPTER 2. BACKGROUND

Compared to its analog counterpart, DPWM controller enjoys several advantages. First, the control law is digitally implemented by writing code in the computation unit, which makes it easier to be modified and promptly reprogrammed without hardware modification. This is in contrast to the many analog component (resistors and capacitors) to configure the controller to different application in the analog field. Second, the all digital environment makes it is easier to migrate to different manufacture process, reducing the time-to-market time and more reliable in the product. It nearly immunes to aging and temperature, which increases the reliability compared to the analog version. Third one, more complicated control techniques, which are hard to implemented in the analog PWM controller can be accomplished in the DPWM controller like the non-linear control techniques, auto-tuning algorithm, on-line tuning method.

On the other hand, DPWM controller falls short compared to the infinite-resolution and sample-free analog control [9] [10] [11]. One of the setbacks of digital controller is the limited resolution of the two main building blocks of the digital loop: ADC and DPWM. While, the conventional analog control is ideally assumed to have infinity resolution. This feature also could bring the instability due to the discrete values of duty cycle, called limit cycle, which will be further discussed in the following section. Also, the sampling process adds delay to the system. This
delay will add loop phase delay, which will potentially cause instability. Ten times higher than the
switching frequency sampling rate is ideal to minimize the phase delay and avoid reconstruction
problems.

2.2.1 Limit Cycle

Since only discreted values of duty cycle code can be generated, only discrete values of
the output voltage can be achieved at the load side. In case of not enough resolution to set a desired
output voltage, which guarantees a zero error signal, the feedback loop will continually alternate
between two closest values of the duty cycle. This kind of large signal oscillation is referred as limit
cycle oscillation.

Considering a system with effective ADC resolution of \(N_{ADC}\) bits and DPWM resolution
of \(N_{DPWM}\) bits, the ADC quantization will be \(\Delta V_{ADC} = V_o / 2^{N_{ADC}}\) and the DPWM will have a
\(T / 2^{N_{DPWM}}\) time resolution, which also means \(\Delta V_{DPWM} = V_{in} / 2^{N_{DPWM}}\) output voltage resolution.
If there is no DPWM level that maps into the ADC bin corresponding to the reference voltage \(V_{ref}\)
(zero-error bin), in steady state, the controller will be attempting to drive \(V_o\) alternate between the
adjacent DPWM levels. This results in steady-state limit cycle.

From above analysis, the controller system should have a DPWM level that maps into the
zero-error bin under all circumstances. This can be guaranteed when the resolution of the DPWM
module is finer than the that of the ADC \[10\],

\[
\Delta V_{DPWM} < \Delta V_{ADC} \tag{2.7}
\]

A one-bit difference in the resolutions, \(N_{DPWM} = N_{ADC} + 1\), is always considered sufficient in
most applications since it provides two DPWM levels per one ADC level.

2.3 DPWM State of the Art Structures

As the DPWM controller is becoming more and more sophisticated, it reveals a new set
of challenges in DPWM design. The popular DPWM structures can be divided into two groups.
One is physical achievements, including counter-comparator based DPWM \[14\], delay line based
DPWM \[15,16\], hybrid DPWM \[17\], and segmented delay line DPWM \[18\]. The other group is
algorithm based, which are dithering DPWM, sigma-delta DPWM, and delay locked loop. This thesis
focuses on the physical approach. Following is a detailed discussion of each of theirs advantages and
disadvantages.
Figure 2.4: Qualitative behavior of $V_o$ with (a) DPWM resolution lower than the ADC resolution, and (b) DPWM resolution two times the ADC resolution. (The switching ripple is not shown, for clarity.)
2.3.1 Counter Comparator based DPWM

This is a very straightforward architecture translated from its analog counterpart. It employs a faster clock that has a frequency of $2^n f_{sw}$ counting up $n$-bit to generate a digital saw-tooth signal of frequency $f_{sw}$. This digital counting signal then is compared to the duty cycle value coming from the compensator, $d[n]$ as clarified in Figure 2.3. The duty cycle is set high when $d[n]$ is smaller than the counting up number in each switching period as shown in Figure 2.5. The sub-clock determines the resolution of this DPWM structure. It is obvious that the this sub-clock’s frequency goes up in the exponential of DPWM bits. It is impractical to achieve such high clock frequency under power consumption restriction.

![Diagram of Counter-comparator based DPWM structure]

Figure 2.5: Counter-comparator based DPWM structure

2.3.2 Delay Line based DPWM

Based on the propagation delay in the digital gates, this kind of DPWM uses the propagation delay time to represents a digital code, as shown in Figure 2.6. The duty cycle is reset to low when the delay reaches the delay cell represent $d[n]$. This structure helps eliminate the high frequency clock needed for the counter-comparator based DPWM, but $2^n$ delay cell is needed at the same time. It consumes a lot of silicon area. It reduces the power consumption, but it brings the device matching issue as well. It suffers more from the temperature and process variation, which causing the total delay time may skew from the switching frequency. Additional technology such as calibration and digital lock loop may be needed.
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2.3.3 Hybrid Approach

Combining the advantages above mentioned two structures, the hybrid approach is more area and power efficient. The delay line is configured as a ring oscillator which feeds the clock to the counter. The higher bits of DPWM can be achieved by the counter-comparator structure [17].

2.3.4 Segmented Delay Line Architecture

This configuration is a grouped version of the delay line which can more easily handle large bits of delay line-based DPWM [18]. Unlike the conventional $N_{DPWM}$ delay line architecture, which
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requires $2^{N_{DPWM}} \times 1$ multiplexer; the segmented version has multiple smaller multiplexer for each line instead of one big multiplexer. For example, a 6-bit DPWM ($N_{DPWM} = 6$) can be segmented to three 2-bit delay lines ($N_{DPWM_{seg}} = 2$). Each has 4 delay elements ($2^{N_{DPWM_{seg}}} = 2^2 = 4$) and a $4 \times 1$ multiplexer as shown in Figure 2.8, which will result in easier multiplexer design requirements.

![Figure 2.8: Segmented DPWM structure](image-url)
Chapter 3

Hybrid Differential DPWM

The conventional hybrid DPWM is analyzed in [17, 19]. A tapped delay line and a digital counter together with comparator are used to build the structure. This structure smartly combines the existing small size counter-comparator DPWM and low power tapped delay-line ring-mux DPWM. Reference [12] improves the conventional structure by employing differential delay line cells to further reduce the area. Reference [12] utilizes the delay-line ring oscillator as the clock of the counter so that a high frequency clock generation circuit is saved. However, the structure proposed in [12] suffers two major problems. One is that its delay cell is an analog differential amplifier with common feedback loop, which causes its delay cell to be much larger than the conventional digital delay cell. The other one is that the delay line is usually highly dependent on the process and temperature, which results that the switching frequency will vary as the process and temperature change. To overcome these problems, a novel 12-bit DPWM with process and temperature calibration is proposed in this paper as shown in Figure 3.1. Eight 1X cells and three 4X cells are connected into a ring oscillator frame. The low 3-bit \([L_0 - L_7]\) and middle 3-bit \([M_0 - M_7]\) are tapped out as denoted in Figure 3.1. The relationship of the low 6-bit signals is shown in Figure 3.2(a), where \(T_d\) is the oscillation period of the delay line. The rising edge sequence is from \(L_7\) to \(L_0\) and \(M_0\) to \(M_7\). For the final DPWM pulse, the Low 3-bit determines the starting edge of the pulse and the high six bits \([H_6 - H_{11}]\) determines how many \(T_d\) is following, and the middle three bits determine the falling edge of the pulse. The total period is \(2^6 \times T_d\) as illustrated in Figure 3.2(b). The differential tapped delay line ring oscillator is composed of 8 1X delay cells and three 4X delay cells. A control voltage called \(V_c\) can adjust all the cells delay time. The control voltage is generated by the process and temperature calibration circuit, which works as following. First, the process and temperature monitor circuits keep monitoring the process and temperature variations and output an analog output.
CHAPTER 3. HYBRID DIFFERENTIAL DPWM

The output is converted to digital code by two 2-bits flash ADC. Combining the information of process and temperature variations, an appropriate voltage is selected through a loop-up table. The detailed circuits are given in the following section. Figure 3.3 shows the simulation results of $L_7$ to $L_0$ and $M_0$ to $M_7$. The top waveform is $L_7$ to $L_0$. The middle waveform is $M_0$ to $M_3$ and the bottom waveform is $M_4$ to $M_7$. The simulation results is well matched with the diagram shown in Figure 3.2.

![Diagram of hybrid DPWM with process and temperature calibration]

**Figure 3.1**: Proposed 12-bit hybrid DPWM with process and temperature calibration

![Time chart of proposed DPWM]

**Figure 3.2**: Time chart of proposed DPWM
CHAPTER 3. HYBRID DIFFERENTIAL DPWM

Figure 3.3: Simulation results of time chart of proposed DPWM

3.1 Differential Segmented Taped Delay Line Structure

The differential segmented tapped delay line part is composed of two segments as shown in Figure 3.4. Instead of a 64-to-1 multiplexer, the segmented structure needs only two 8-to-1 multiplexers, which significantly reduces the complexity and size of the multiplexer. One segment is denoted as the $1X$ delay cells, which represents the low three bits $d[2 : 0]$. The other segment consists of three $4X$ delay cells, which is four times delay time as the $1X$ delay cell. The delay cells are a combination of delay element and inverters, which will enhance the integrity of signal. A control voltage called $V_c$ is used to adjust the delay element’s delay time.

The detailed structure of $1X$ cell in Figure 3.4 is revealed in Figure 3.5(a). It is composed of two voltage controlled inverter delay elements in parallel and two minimum sized inverters connected head to tail between the outputs of two delay elements, which are to ensure the opposite phase of the differential output. The delay element, as shown in Figure 3.5(b), is constructed by a voltage controlled inverter and a gain boost inverter, which provides sharper transient edges, and a full digital output swing for the delay element. The voltage-controlled inverter has an additional NMOS transistor $M_c$ in the pull-down of the inverter controlled by a control voltage $V_c$. Equation (3.1) below gives the delay time. Besides the $W/L$ ratio of the transistors, the delay time is also
CHAPTER 3. HYBRID DIFFERENTIAL DPWM

Differential Segmented Tapped Delay Line Ring Oscillator

\[ t_p = \frac{1}{2}(t_{pLH} + t_{pHL}) = \frac{C_L}{2} \left( \frac{1}{k_p V_{DD}} + \frac{V_{DD}}{k_n V_c^2} \right) \]  (3.1)

Figure 3.4: Differential segmented taped delay line

inversely proportional to the square of \( V_c \), giving a flexible factor for fine tuning of the delay time.

3.2 Temperature Monitor

For temperature monitor, it is necessary to design an effective circuit that is process insensitive and linear to temperature. Although [20] proposed a temperature monitor circuit, it works in sub-threshold region, which is not reliable in the real implementation. A traditional Proportional To Absolute Temperature (PTAT) current generator [21] together with buffer output can meet the temperature monitoring requirements as illustrated in Figure 3.6. The start-up circuit is used to prevent the PTAT circuit from the zero current state. Once the circuit is activated, transistor \( M_s \) is off and isolates the start-up circuit from the PTAT current generation circuit. For the PTAT current

Figure 3.5: (a) Differential delay cell (b) Voltage controlled delay element
CHAPTER 3. HYBRID DIFFERENTIAL DPWM

generation part, \( M_{p1} - M_{p2} \) and \( M_{n1} - M_{n2} \) are identical pairs and formed in the current mirror frame, thus the current in two branches is equal, \( I_1 = I_2 \). Thus the source voltages of \( M_{n1} \) and \( M_{n2} \) are approximately the same. The voltage across \( R_1 \) is calculated as

\[
V_{R_2} = V_{BE1} - V_{BE2} = V_T \ln n,
\]

Where \( n \) is the size ratio of \( Q_2 \) to \( Q_1 \), and \( V_T \) is the thermal voltage, given by

\[
V_T = K \times \frac{T}{q},
\]

Where \( K \) is Boltzmann’s constant, \( T \) is the absolute temperature, and \( q \) is the electron charge. \( I_o \) is the mirrored current and has the same value as \( I_1 \) and \( I_2 \). Therefore, the output voltage can be expressed as

\[
V_{out} = V_{ref} - \frac{R_2}{R_1} V_T \ln n,
\]

where \( V_{ref} \) is a level shift voltage. \( R_1 \) and \( R_2 \) cancel each other’s temperature effect. \( V_{out} \) is inversely proportional to the absolute temperature.

The simulation results are summarized in Table 3.1. The waveforms at different process corners are also included in Figure 3.7. The output voltage differs a lot as temperature changes but only with little process variation. The 2-bit flash ADC described in next sub-section will encode three cases of temperature output.

Figure 3.6: temperature monitor circuit
CHAPTER 3. HYBRID DIFFERENTIAL DPWM

Table 3.1: Temperature monitor circuit simulation results

<table>
<thead>
<tr>
<th>Temp.</th>
<th>Vout (ff)</th>
<th>Vout (tt)</th>
<th>Vout (ss)</th>
<th>$T_1/T_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-40^\circ$C</td>
<td>487.9 mV</td>
<td>487.5 mV</td>
<td>487.4 mV</td>
<td>11</td>
</tr>
<tr>
<td>25$^\circ$C</td>
<td>427.5 mV</td>
<td>427.3 mV</td>
<td>427.1 mV</td>
<td>10</td>
</tr>
<tr>
<td>125$^\circ$C</td>
<td>337.2 mV</td>
<td>337.0 mV</td>
<td>336.5 mV</td>
<td>01</td>
</tr>
</tbody>
</table>

Figure 3.7: Simulation results of temperature monitor (a) ff corner (b) tt corner (c) ss corner
3.3 Process Monitor

[20] also proposed a process monitor circuit. However, its still designed for sub-threshold operation, which is not reliable in the real implementation. The proposed process monitor circuit is illustrated in Figure 3.8. It is composed of start-up circuit, PTAT current generation circuit, and a process dependent output. The start-up circuit and PTAT current generator are the same as the ones shown in Figure 3.6. The output voltage equals the gate source voltage of $M_5$ plus the voltage drop between $R_2$ as written in Equation (3.5). $M_5$ has the same dimension as $M_c$ in Figure 3.5(b).

The $V_{GS}$ has a negative temperature coefficient and the voltage across $R_2$ provides a positive temperature coefficient. Choosing suitable $R_2/R_1$, it is possible to make the overall temperature coefficient zero at room temperature. $V_{out}$ will be affected by the large threshold-voltage variation in different process corner since $V_{GS}$ is highly related to the threshold voltage $V_{th}$. The simulation results are summarized in Table 3.2. The $V_{out}$ changes more than 50mV at different process corner, but only varies less than 8mV across the whole temperature range. Figure 3.9 shows more in details the performance of this process monitor. All three corners have small temperature variation but distinguish value between corners.

\[ V_{out} = V_{GS(M5)} + \frac{R_2}{R_1} V_T \ln n \]  
\[ \frac{\partial V_{out}}{\partial T} = \frac{\partial V_{GS}}{\partial T} + \frac{R_2}{R_1} \times \frac{K}{q} \times \ln n = 0 \text{@25°C} \]  

Figure 3.8: Process monitor circuit
CHAPTER 3. HYBRID DIFFERENTIAL DPWM

Table 3.2: Process monitor circuit simulation results

<table>
<thead>
<tr>
<th>Corner</th>
<th>Vout (−40°C)</th>
<th>Vout (25°C)</th>
<th>Vout (125°C)</th>
<th>$P_1$ $P_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>ss</td>
<td>491.8 mV</td>
<td>491.8 mV</td>
<td>498.0 mV</td>
<td>11</td>
</tr>
<tr>
<td>tt</td>
<td>415.9 mV</td>
<td>414.1 mV</td>
<td>418.1 mV</td>
<td>10</td>
</tr>
<tr>
<td>ff</td>
<td>344.9 mV</td>
<td>341.9 mV</td>
<td>344.9 mV</td>
<td>01</td>
</tr>
</tbody>
</table>

Figure 3.9: Simulation results of process monitor (a) tt corner (b) ff corner (c) ss corner
3.4 2-bit Flash ADC

![2-bit Flash ADC with bubble error correction](image)

Figure 3.10: 2-bit Flash ADC with bubble error correction

In the proposed DPWM, the process and temperature monitoring circuit output is quantized into two bits, and a 2-bit flash ADC can complete this job. Higher bits can obtain better accuracy in the process and temperature calibration, but it will consume more power and area. One can choose appropriate resolution for a different system specification. Bubble error may occur due to device mismatch, offset voltage, and etc. In this thesis a two bit flash ADC with bubble error correction and digital encoding \[22\] is designed as shown in Fig.3.10. The output code is listed in Table.3.1 and Table.3.2.

3.5 Look-up Table

Both the process and the temperature will affect the delay time at the same time. Table.3.3 lists all possible combination of process and temperature variations. A look-up table circuit is designed to select different output according to the process and temperature output code as shown in Fig.3.11. A driving stage is added to drive the large delay line load.
Table 3.3: look-up table for different corners

<table>
<thead>
<tr>
<th>Process Corner</th>
<th>Temperature</th>
<th>Control Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>ss tt ff</td>
<td>-40°C</td>
<td>25°C</td>
</tr>
<tr>
<td>11 11</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>11 10</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>11 01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 11</td>
<td></td>
<td>11</td>
</tr>
<tr>
<td>10 10</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>10 01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01 11</td>
<td></td>
<td>11</td>
</tr>
<tr>
<td>01 10</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td>01 01</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CHAPTER 3. HYBRID DIFFERENTIAL DPWM

3.6 DPWM Simulation Results

In order to verify the function of temperature monitor, a enable signal is added to the temperature monitor. When temperature monitor is disabled, the default state is room temperature. When temperature monitor is enabled, different control voltage will be selected to adjust the delay time, thus the frequency of the delay line oscillator. Figure 3.12(a) shows that when the temperature monitor is enabled at 400ns, the control voltage $V_c$ gradually drops 15 mV to a new state in the case of a high temperature. The top delay line waveform also shows different frequency versus adjusted control voltage $V_c$. Figure 3.12(b) illustrates the opposite situation when a low temperature is detected.

The same function is also added to process monitor. When the process monitor is disabled at the first place, the control voltage output the default value. However, once it is enabled, different process corner is detected followed by the adjustment of the control voltage immediately. Figure 3.13 presents the delay line frequency change and control voltage change after different process corner is picked up.

These two group of waveforms verify that both temperature and process environment will dramatically affect the performance of the delay line. With the proposed calibration method, the error can be corrected into a really good state.

The ultimate goal of DPWM is to translate 12-bit digital code into a pulse. The duty cycle should increase linearly with the code and has a duty cycle resolution of $1/4095 \times 100\% = 0.02\%$. Figure 3.14 presents the duty cycle relationship with 12-bit digital code. From the results details showing in A, the minimum duty ratio is 1.7%. This is due to the clock comparator’s minimum counting number is one period. In the actual design, the minimum duty ratio is also limited for other reason, so we can set the minimum duty ratio to be 5%. Also when the duty ratio reaching 100%, the system can not reach 100% for reset reason. For the whole system design, we should also limit the maximum duty ratio to 99%. In the middle, we can see the linearity and resolution is very close to the ideal value. The LSB represents 0.02% duty ratio change in the real design. The total design specification is met.
Figure 3.12: Temperature sensor enabled when (a) high temperature detected (b) low temperature detected
When process monitor enabled

Figure 3.13: process sensor enabled (a) ff corner detected (b) ss corner detected
Figure 3.14: Duty cycle as digital code increase with three detailed section
Chapter 4

Conclusion

The thesis explores digital pulse width modulation (DPWM) with the objective of achieving improvements in high resolution and high accuracy over conventional approaches. Major conclusions achieved are summarized as follows:

Digital controllers, compared with analog controllers, are in favorable position to provide low cost but great flexibility control methodology. However, digital controllers suffer from the discrete resolution and loop delay, which will cause serious situation of limit cycle. One major criteria to eliminate the limit cycle condition is the resolution of DPWM should be at least one bit higher than that of the ADC. The key design issues and challenges of high resolution and high accuracy DPWM have to be explored.

Conventional DPWM structures are categorized as counter based DPWM, delay line based DPWM, counter-delay line hybrid DPWM, and segmented DPWM. Each of them is analyzed and compared in this thesis. The counter based DPWM requires high frequency clock and high power consumption, but low silicon area requirement. The delay line based DPWM is low in power consumption, but too large silicon requirement. Combining these two structures comes to the hybrid DPWM structure. It enjoys both the advantages of counter based DPWM structure and delay line based DPWM structure. High resolution can be easily achieved. The segmented DPWM structure divides the delay line based DPWM into more segments, so that more bits with less complicated mux can be achieved. For the design challenge of a 12-bit DPWM, only hybrid DPWM structure is not enough since the low 6-bit delay line structure will need $2^6 = 32$ to 1 mux, which is unrealistic in digital circuit design. Finally, the proposed 12-bit DPWM adopts the hybrid DPWM structure with low 6-bit segmented into 2 parts delay line. In this way, only two 8 to 1 muxes are needed.

Calibration is widely used method of high precision circuits, which is usually to correct
CHAPTER 4. CONCLUSION

the device mismatch, process corner variation and temperature influence etc. In this thesis, the original 12-bit [DPWM] itself also suffers from the process and temperature variation which causes the switching period the Buck converter changing over time. This will introduce a lot of uncertainties of whole system performance and miserable real application. Through literature reading and comparing, firstly a tunable delay cell is chosen; secondly process and temperature calibration circuits are proposed to tune the delay cell in time. The whole [DPWM] is designed with 0.11um technology. Each sub-circuit is carefully verified by simulation and together with the whole [DPWM] works great with all specification met. The overall simulation of [DPWM] shows that the process and temperature calibration circuits can tuned the [DPWM] into target frequency. What’s more, the duty ratio simulation shows good linearity for a large range.

Although [DPWM] has been done at this thesis, more works are left to complete the whole digital controller design. First, a 11-bit ADC is need to sample the output voltage. Then a computation unit with Proportional-Integral-Derivative (PID) control should be added to complete the stable negative feedback loop. Furthermore, advanced control algorithm can also been explored to added to the system. Finally a tape-out will serve the best purpose of verification of the whole design.
Bibliography


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