A Low Jitter PLL Using High PSRR Low-Dropout Regulator

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by
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To my family.
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List of Acronyms

PLL  Phase Locked Loop.

DLL  Delay Locked Loop.

PFD  Phase and Frequency Detector.

CP   Charge Pump.

LPF  Low Pass Filter.

VCO  Voltage Controlled Oscillator.

OA   Operational Amplifier.

LDO Regulator  Low DropOut Regulator.

PSRR or PSR  Power Supply Rejection Ratio.

PTAT  Proportional To Absolute Temperature.

CTAT  Complimentary To Absolute Temperature.
Acknowledgments

Here I wish to thank those who have supported me during the process of the thesis work....
Abstract of the Thesis

A Low Jitter PLL Using High PSRR Low-Dropout Regulator

by

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Northeastern University, June 2015

Dr. Yong-Bin Kim, Adviser

In the recent years, the world has seen a huge boom in portable electronic products like cell phones, tablets, etc. Most of the products are powered by a battery that requires a power supply noise management circuitry to optimize the performance. As a result, lots of recent researches have been proposed across the world in battery’s power supply noise management field to improve power consumption and also to reduce the cost of integrated chips.

Phase-Locked Loop (PLL) is a feedback system that forces a voltage controlled oscillator to replicate and track the frequency and phase at the input when in lock[1][2]. It is a control system allowing one oscillator to track with another. The PLL is widely used and its usage is continuously increasing in modern integrated circuit design such as synthesizers and clock generators [3].
One of critical performance, an output jitter, increases as the required frequency increases in modern IC design. Reference clock noise is small since it is generated by a crystal oscillator, but VCO noise is usually higher than the reference clock noise [1]. The output jitter should be reduced in order to provide the good timing clock signal to other systems. Due to the output jitter issue, the PLL is often designed with high power efficiency low-dropout regulator (LDO) and low pass filter (LPF) to reduce high frequency supply noise and any other noises for a desired frequency output[4, 5, 6, 7, 8].

This thesis presents low power and low jitter phase locked loop (PLL) design using proposed LDO regulator and active loop filter on 110nm CMOS technology node and with 1V power supply voltage. In order to reduce jitter, the supply voltage is regulated by low-dropout (LDO) regulator which regulates supply voltage with minimal noise and delivers the low noise power to the active loop filter (ALF), clock distribution buffers, phase and frequency detector, divider, and charge pump, and VCO. The active Butterworth low-pass filter filters high frequency noise of the VCO control voltage with a regulated supply voltage. The supply voltage delivered to VCO and ALF has minimal noise since the supply noise and device noise from other blocks are filtered out using subtractor inside the LDO regulator.

In this thesis, the supply noise is 100mV_{pk−pk} with 100KHz before regulation. The proposed LDO provides 0.8 V output, 83 dB PSRR with entire PLL load, 100μA of I_Q, 0.578 mW power consumption, and with 40mA load condition. The proposed LDO is composed of a folded operational amplifier with 71dB gain, a gain compensation stage increasing amplitude of op-amp output to be same as supply noise amplitude for the perfectly cancellation, pass transistor with W/L size of 7500μm/1μm, and zero compensation stage pushing zero to high frequency. The jitter without and with LDO and ALF is 44.9 ps and 4.6 ps, respectively. Another jitter simulated by monte carlo simulation is 17.2ps with 10 times orthogonal process variations.
Chapter 1

Introduction

1.1 Motivation

In the recent years, the world has seen a huge boom in portable electronic products like cell phones, tablets, etc. Most of the portable products are powered by a battery that requires a power supply noise management circuitry to optimize the performance. As a result, lots of recent researches have been researched across the world in battery’s power supply noise management field to improve power consumption and also to reduce the cost of integrated chips.

Fig. 1.1 describes a way to convert a battery voltage to an necessary voltage for a certain application in general. First of all, the battery supplies to the switching converter such as a buck converter that steps down the battery supply voltage to wanted lower output voltage with small ripples at its switching frequency. The ripples affects critical performance factor on the application such a voltage controlled oscillator. Therefore, a linear regulator is added right before the load block to remove the ripples.

Figure 1.1: Generation of power supply voltage
CHAPTER 1. INTRODUCTION

Phase-Locked Loop (PLL) is a feedback system that forces a voltage controlled oscillator to replicate and track the frequency and phase at the input when in lock\[^{1,2}\]. The PLL is widely used because the all electronic products are required controlling digital circuit by a clock.

There are many important circuit metrics that represent PLL performances. One of critical parameters is an output jitter which increases as the required frequency increases in modern IC design. Reference clock noise is small since it is generated by a crystal oscillator, but VCO noise is usually higher than the reference clock noise \[^{1}\]. The jitter has to be reduced in order to provide the good timing clock signal to other systems. Due to the jitter issue, the PLL is often designed with high power efficiency low-dropout regulator (LDO) and loop filter (LP) to reduce supply noise and any other noises for a desired frequency output\[^{4,5,6,7,8}\].

Two methods that reduce power supply noise are presented in this thesis to reduce the PLL output jitter. The first one is active low-pass filter, which suppresses supply noise from the other blocks. It makes the control voltage of VCO stable and has relatively small resistance and capacitance than passive filter. The other one is LDO regulator, which provides a clean power supply voltage to VCO by subtracting pass transistor control voltage ripple from power supply noise since VCO is very sensitive to $V_{dd}$. In order to cancel the pass transistor biasing voltage and supply noise ripple effectively, a compensated circuit is added for finite amplifier’s gain.

1.2 Organization of Thesis

Chapter II reviews the analysis of how the PLL performs and suffers from supply noise in each conventional block, phase frequency detector, charge pump, loop filter, voltage controlled oscillator and divider. In addition, the difference between DLL and PLL is shown in the chapter to understand the general clock generation system methods. In chapter III, it discusses classification of the LDO regulator. In case of the LDO regulators, it shows design considerations such as choice of input transistor in error amplifier, pass elements, and pole compensation for an high PSRR LDO regulator against supply noise. Chapter IV describes
CHAPTER 1. INTRODUCTION

supply-regulated current starved voltage controlled oscillator design with active loop filter and the proposed enhanced PSRR LDO regulator, and Chapter V illustrates simulation results and compares jitters with and without the proposed approach, followed by conclusion in Chapter VI. All circuits in the thesis are based on 110nm standard CMOS technology with 1V power supply voltage of proposed LDO regulator. The PLL blocks are supplied by the LDO output voltage which is 0.8V.
Chapter 2

Supply Noise Analysis in Phase-Locked Loop

Phase-locked loop (PLL) is known as low-pass system and generates well-timed on-chip clock for various applications. The basic concept of phase locking has remained the same since its invention in the 1930s [1]. But, the design and implementation of PLL have been researched continuously since it is challenging for high frequency requirement. In order to understand the challenges and trade-off of PLL, this chapter provides a brief study.

Section 2.1 and 2.2 provide operation theory of each block in PLL and comparison between PLL and delay-locked loop for understanding general clock generation method. The supply noise analysis of each block, phase and frequency detector, charge pump, loop filter, divider, clock buffer, and voltage controlled oscillator are discussed in section 2.3. In addition, summary of the PLL supply noise analysis is presented in section 2.4.
2.1 Phase-Locked Loop

Phased-locked loop, shown in Fig. 2.1, is essential building block composing of five components, which are a phase frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), a voltage controlled oscillator (VCO), and a frequency divider.

The phase frequency detector compares two input signals, which are clock_in and divided clock, and sends the difference to the next block, charge pump. The charge pump charges or discharge current to a capacitor over time which exists between the charge pump and low pass filter depending on the PFD’s frequency difference. Then, the current is converted to a voltage in the capacitor. The voltage controlled oscillator is controlled to generate a desired output frequency signal propagating to the divider block. The VCO output frequency can be divided by N to increase the VCO frequency by N depending on the performance requirement. The importance of PLL is continuously increasing in modern integrated circuit design such as synthesizers and clock generators [3]. The closed-loop transfer function of PLL, \( H_{closed}(s) \), can be written as Eq. (2.1) where \( H_{open} \) is open loop transfer function and \( \left( \frac{1}{N} \right) \) represents divider block. The open-loop transfer function is shown in Eq. (2.2). \( H_{open} \) is proportional to voltage-to-frequency conversion gain \( (K_{VCO}) \), charge pump current over phase range \( (\frac{I_{CP}}{2\pi}) \), low-pass filter transfer function \( (F(s)) \), and gain of phase and frequency detector \( (K_{PFD}) \).

![Figure 2.1: Phase locked loop in general](image)
CHAPTER 2. SUPPLY NOISE ANALYSIS IN PHASE-LOCKED LOOP

\[
\frac{Clock_{out}}{Clock_{in}}(s) = H_{closed}(s) = \frac{H_{open}(s)}{1 + H_{open}(s)} \cdot \frac{1}{N} \tag{2.1}
\]

\[
H_{open}(s) = K_{PFD} \cdot \frac{I_{CP}}{2\pi} \cdot F(s) \cdot \frac{K_{VCO}}{s} \tag{2.2}
\]

2.2 Delay-locked Loop

In section 2.1, the voltage controlled oscillator based loop system is explained. On the other hand, the delay line based frequency generating loop system is defined as a delay-locked loop (DLL) as shown in Fig. 2.2. Other blocks in DLL are similar to the PLL except that a variable delay line replaces the oscillator \[9\]. In case of the DLL, it only detects phase while the PLL detects phase and frequency. It is also known as single pole system. A phase detector (PD) measures phase difference between clock\_in and delay\_out. Then, the phase error is sent to the low pass filter. To correct the phase error of delay\_out, DLL requires an integrator similar to PLL that have a charge pump and capacitor as an integrator for accumulating phase errors. Therefore, the integrator has to be used as LPF to eliminate phase offset of DLL since DLL corrects the error by the time constant of the loop \[10\] \[11\].

The closed-loop transfer function, \(H_{closed}(s)\) is equal to Eq. (2.3). The open-loop transfer function, \(H_{open}\), is shown in Eq. (2.4). It is proportional to voltage-to-delay conversion gain (\(K_{dly}\)), Low-pass filter transfer function (\(K_{F}/s\)), and gain of phase detector (\(K_{PD}\)). By comparison between DLL and PLL transfer functions, the DLL has simple characteristics.

\[
\frac{Delay_{out}}{Clock_{in}}(s) = H_{closed}(s) = \frac{H_{open}(s)}{1 + H_{open}(s)} \tag{2.3}
\]

\[
H_{open}(s) = K_{PD} \cdot K_{F} \cdot \frac{K_{dly}}{s} \tag{2.4}
\]
CHAPTER 2. SUPPLY NOISE ANALYSIS IN PHASE-LOCKED LOOP

Nevertheless, the DLL has its own limitations even though it has a simple loop characteristics. First, for clock generation, only one input clock is available so the clock is used as the input to the delay line as well as the phase detector [12]. Thus, any high frequency noise can directly inject to the delay output block, delay line. In contrast, PLL can eliminate high frequency noise in reference clock by lowering its bandwidth. Secondly, the delay lines usually have a finite delay range [12]. Limited delay range of the delay lines causes not to lock properly. Third, it is not as easy to multiply the reference frequency [13]. But, PLL can be any higher frequency than reference clock.

These advantages of PLL over DLL encourage us to focus on a design of PLL in this thesis. Jitter reduction techniques are similar to DLL since PLL and DLL have many similar components.
2.3 Supply Noise Analysis

2.3.1 Fundamental of Jitter

Before supply noise of PLL blocks is analyzed, jitter should be clearly defined for correct analysis since the purpose of this thesis is minimizing output jitter in PLL.

Phase jitter is defined as the standard deviation, $\sigma_{\Delta \phi}$, of the phase difference between the first cycle and $m$ th cycle of the output clock. Timing jitter can be expressed in terms of phase jitter by $\sigma_{\Delta \phi} = \frac{1}{\omega_o} \cdot \sigma_{\Delta \phi}$, where the clock period, $T$, is $\frac{2\pi}{\omega_o}$ [14]. It is called short-term jitter for small $\Delta T$ and long term jitter as $\Delta T$ goes to infinity. The tracking jitter, $\sigma_{tr}$, is a commonly used metric for a PLL output clock. It is measured as the phase difference between a clean reference clock and the PLL output clock as shown in Figure 2.3. The tracking jitter is related to timing jitter by $\sigma_{tr} = \frac{\sigma_{\Delta \phi}}{\sqrt{2}}$ at very large $\Delta T$ [15].

2.3.2 Supply Noise Path in PLL

In integrated circuit designs, PLL components cannot avoid from the supply noise effect since supply voltage of PLL usually comes from dc-dc converter which has ripple through the output [3]. The noise increases PLL’s timing uncertainty and lock-in time. In the recent

![Figure 2.3: Jitter in general a) timing jitter b) tracking jitter](image)
CHAPTER 2. SUPPLY NOISE ANALYSIS IN PHASE-LOCKED LOOP

years, many researches \[4, 8, 15, 16, 17, 18, 19, 20, 21\] have been proposed as PLL supply noise mitigation techniques for lowering output jitter.

Even though all the blocks in PLL are affected by the supply noise, the most sensitive block to the supply noise is the VCO since all supply noises from other blocks are propagated through the VCO control voltage. Fig. 2.4 illustrates how the supply noise affects the output jitter in each block. For simplicity, the reference and VCO clock buffers are not shown. The noisy signals from PFD, charge pump, divider migrate into the VCO in the PLL. As a result, the supply noise migration into the VCO is appeared in its output as a jitter. Excessively large jitter consumes some of the clock budget and it can cause error propagation as well as intercommunication errors between chips \[16\]. Therefore, for an accurate output frequency of PLL, the supply noise have to be perfectly eliminated by proper regulating methods.

Figure 2.4: Supply noise migration in PLL
2.3.3 Phase and Frequency Detector and Charge Pump

A common architecture for clock generation uses a phase-frequency detector (PFD) for simultaneous phase and frequency acquisition. Generating high frequency clock increases the difficulty of the design of the PFD for systems with a high input clock frequency and minimum multiplication. For the fast lock-in time in PLL, the PFD is required to be wide range, well-timed detection and minimum propagation delay.

A phase and frequency detector, allowing for wide frequency locking range, potentially entire VCO tuning range detects frequency and phase by comparing phase difference between the reference clock and the divided output clock, generates up and down signals, and sends them to charge pump. In general, the PFD is composed of two D flip-flops and

![Diagram of Phase and Frequency Detector and Charge Pump](image)

Figure 2.5: Supply noise effect on phase and frequency detector
one AND gate. Each D flip-flop detects rising edge of the reference clock and divided clock
in one cycle and then generates its differences, up and down signals. The signals are sent to
not only a charge pump, but also the AND gate for resetting current frequency and phase
differences and preparing to next incoming clock cycle. The gain of PFD, $K_{PFD}$, can be
presented as $\frac{2}{2\pi} = \frac{1}{\pi}$, where $2\pi$ is frequency detection range of input signals in PFD.

Fig. 2.5 (a) presents design of conventional PFD that has noisy $V_{dd}$. If the PFD got
influenced by supply noise, the output signals, up and down, are faltered. In practice,
it is important to pay attention carefully to the mismatch between UP and DN paths to
suppress reference spurs or equivalently, in time domain, to minimize deterministic jitter
[22]. However, the noise effects of up and down signals can be canceled each other since
the signals waveforms are exactly symmetric [3]. The noise effects may not be canceled if
non-balanced output wave forms are generated due to device mismatches. Therefore, it is
understood that the PFD is the most immune block to supply noise. In addition, when short
output pulses due to small phase error, are produced by PFD, it cannot effectively propagate
these pulses to a switch of charge pump. As the result, it causes low loop gain and increases
jitter. It is called a dead zone. In order to minimize dead zone, the delay line, the shaded
area as depicted in Fig. 2.5 (a), should be added to generate a minimum up and down pulse
length [23].

A charge pump is most commonly employed structure that charges and discharges of the
current, $I_{CP}$ and generates control voltage by combination of charge pump and loop filter
capacitor, $C_P$, depending on the up and down signals as shown in Fig. 2.5 (b). The charge
pump has the same amount of charging and discharging current for accurate control voltage
and fast lock-in time. For these reasons, the charge pump gain, $\frac{I_{CP}}{2\pi C_P} \cdot \phi$, where $\phi$ is phase
difference between reference clock and divided output clock, should be designed to be $\frac{V_{DD}}{2}$.

To find the frequency response of the input current, we can represent as follow:
CHAPTER 2. SUPPLY NOISE ANALYSIS IN PHASE-LOCKED LOOP

\[ I(s) = \frac{V_{\text{out}}}{Z(s)} = \frac{V_{\text{out}}(s)}{sC_p} \]  

(2.5)

where \( Z(s) \) is the complex impedance. So the current source can be modeled as:

\[ \frac{I(s)}{\Delta \phi} = \frac{I_{CP}}{2\pi} \]  

(2.6)

where \( \Delta \phi \) is the phase difference. Unfortunately, this charge pumps are very sensitive to supply noise. This susceptibility arises from up/down current mismatch induced by: i) finite output impedance of the current sources and ii) asymmetric noise coupling into the up and dn current sources through the bias circuitry [22].

If charge pump is exposed by supply noise, the amount of charging and discharging current would be different. Furthermore, the current can be leaked due to the fact that the previous signals, up and down, are flickered, and can affect the loop filter and VCO. Therefore, the supply noise induces waver signal that affects next block.

2.3.4 Voltage Controlled Oscillator

An oscillator is defined as an autonomous system that accomplishes a periodic output clock by controlling voltage, \( V_{ctl} \). A CMOS ring oscillator consisting of inverter chain that has fast transition characteristic as shown in Fig. 2.6. The inverter chain is possible to be

![Figure 2.6: Conventional ring oscillator composing of inverter chain](image-url)

Figure 2.6: Conventional ring oscillator composing of inverter chain
CHAPTER 2. SUPPLY NOISE ANALYSIS IN PHASE-LOCKED LOOP

represented as its resistance and capacitance. As a result, the frequency of oscillation can be written as follow:

\[ f_{osc} = \frac{1}{2 \cdot N \cdot \tau} \]  \hspace{1cm} (2.7)

where \( N \) is number of inverter and \( \tau \) is time constant that delay due to each element, \( \frac{1}{R_{tot}C_{tot}} \). The number of inverter is determined by the desired clock output of system.

The slope of frequency versus control voltage is called voltage-to-frequency conversion gain, \( K_{VCO} \); \( K_{VCO} = \Delta f_{VCO} / \Delta V_{ctl} \). The phase which is integral of frequency, can be written as \( \phi_{VCO} = \int K_{VCO} \cdot V_{ctl} \cdot dt \). Therefore, the VCO in the frequency domain is modeled as \( \frac{\phi_{VCO}}{V_{ctl}}(s) = \frac{K_{VCO}}{s} \).

The voltage controlled oscillator, placed in PLL’s clock output, is a core component. According to [3], the VCO is the most sensitive block that has to be regulated by proper method in PLL. To get low output jitter, the VCO has to be designed with wide-swing frequency range for increasing the power supply rejection ratio (PSRR).

2.3.5 Frequency Divider and Clock Buffer

A frequency divider, composed of D flip-flops, is needed for compensating frequency limitation of crystal oscillator in a frequency synthesizer application or clock multiplier application. A clock buffer, used by two inverters in series, is needed for propagating the output signals to other application blocks since the signals are attenuated by wire resistance and parasitic inductance and capacitance.

Frequency divider and clock buffer are digital block in PLL and it also contributes significantly to the output jitter. Therefore, to analyze supply-noise sensitivity of the digital building blocks easily, they can be understood simply by examining the CMOS inverter as shown in Fig. 2.7(a) [22]. The CMOS inverter is converted to small signal model that
CHAPTER 2. SUPPLY NOISE ANALYSIS IN PHASE-LOCKED LOOP

shows the supply noise effect as shown in Fig. 2.7(b). The noisy $V_{dd}$, $\Delta V_{dd}$, directly injects to the inverter and the output voltage, $V_{out}$, is represented as follow:

$$V_{out} = \frac{r_{dsn}}{r_{dsp} + r_{dsn}} \Delta V_{dd}$$  \hspace{1cm} (2.8)

where, $r_{dsp}$ and $r_{dsn}$ are output resistance of PMOS and NMOS, respectively. According to Eq. 2.8 the $V_{out}$ is changed by variation of $V_{dd}$. Therefore, the supply noise is critical parameter for the output jitter.

As the number of inverters are increased, the more output jitter is induced. If the $V_{dd}$ is faltered, it directly affects the delay of the inverter. Therefore, the output jitter is getting worse due to supply noise. Thus, the supply noise has to be eliminated by proper regulation method since the clock buffers are placed in clock-out for lowering output jitter and fast transition.

![Figure 2.7: Supply noise analysis for a CMOS inverter (a) a simple CMOS inverter (b)](image)
CHAPTER 2. SUPPLY NOISE ANALYSIS IN PHASE-LOCKED LOOP

2.3.6 Loop Filter

A loop filter is a common architecture of PLL that affects the dynamic characteristics of PLL such as bandwidth, lock ranges, and transient response. Resistor and capacitor are widely used for loop filter in PLL since passive devices have high quality factor and they are very reliable. These parameters have to be determined carefully or it may take the loop too long to lock, or once locked, even small variations in the input data may cause the loop to unlock [2]. The low-pass filter accepts the output from the phase detector, removes the high frequency noise and produces a dc level [24].

Loop filters can be divided into two distinct types: active loop filters and passive filters as shown in Fig. 2.8. Their transfer functions of the passive filter and active filter, \( F(s)_{\text{passive}} \) and \( F(s)_{\text{active}} \), are written as follows:

\[
F(s)_{\text{passive}} = \frac{1}{1 + sR \cdot C}
\]

\[
F(s)_{\text{active}} = -\frac{C_1}{C_2} \cdot \frac{sR_2 \cdot C_2 + 1}{sR_1 \cdot C_1 + 1}
\]

where \( R \) is resistance of passive filter \( R_1 \), and \( R_2 \) are resistance of passive filter and \( C \) is capacitance of passive filter and \( C_1 \), and \( C_2 \) are capacitance of active filter. Active loop

![Figure 2.8: Comparison between active and passive filters: (a) 1st order passive filter (b) active lag filter](image)

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CHAPTER 2. SUPPLY NOISE ANALYSIS IN PHASE-LOCKED LOOP

filters contain amplifying devices to increase signal strength while passive do not contain amplifying devices to strengthen the signal. The low pass filters attenuate the signal and have a gain of less than one beyond $f_{3dB}$.

The passive and active filter has its advantages and disadvantages as follows: First, the passive filter is linear. By using definition of linear property, the passive filter satisfies homogeneity and superposition while active filter has an operational amplifier that has limited linear region. Secondly, passive filter has relatively low noise than active filter. The active filter uses combination of an operational amplifier and passive elements to reduce size of resistance and capacitance by using transresistance. But, each MOSFET in op-amp has disadvantage of its own noise sources. Third, passive filter has unlimited frequency range. The passive filter can change frequency range by varying resistance and capacitance size. It is not appropriate to the IC since the chip die size is fixed. In the case of the larger size of resistance (>100KΩ) and capacitance (>100pF), they can be used as external components in general.

By comparing the passive with active filters, the trade-off is distinctly distinguished through their advantages and disadvantages. In case of integrated circuit systems, there is area limitation, therefore the active filter is preferred if the supply noise is eliminated by proper regulation.

2.4 Summary

This chapter discussed the basic concept of the PLL and its operation that are significant to understand design consideration of each block against generating clock skew and output jitter. In addition, supply noise makes its degenerated performance such as high output jitter and delayed lock-in time.

The DLL is described as a single pole system, simple transfer function and small area
CHAPTER 2. SUPPLY NOISE ANALYSIS IN PHASE-LOCKED LOOP

occupation. In addition, the architecture is similar to the PLL except that a variable delay line replaces the oscillator. In delay line, high frequency noise from reference clock directly injects and causes higher output jitter than PLL. Furthermore, it does not accumulate phase error while PLL does. Due to limited delay range, it is not locked properly. For these disadvantages of DLL, this thesis focuses on PLL.

According to [3], the most sensitive block in PLL is a voltage controlled oscillator by simulating PAC analysis to get power supply noise rejection (PSNR). Example of the VCO is shown as ring oscillator for simple and understandable analysis. Since supply noise propagates through PLL components, the effect of supply noise results in clock output with its jitter. Supply noise effect in clock buffers is critical since the clock in and out signals pass through them. Clock buffers, ring oscillator, and divider can be converted to the inverters. It is understandable to see how the supply noise directly affect the blocks.
Chapter 3

PSRR Improvement in Low-Dropout Regulator

For the PLL to achieve low jitter, the supply noise regulation is desirable in integrated circuit. In the recent years, many researches have been proposed for supply regulation techniques by using a low dropout regulator (LDO). Since LDOs don’t use a zener diode, they are the most efficient and highly accurate regulators under the class of linear regulators compared to shunt or series voltage regulator [25].

In section 3.1, a few types of regulator are presented in order to understand definition of the regulators and its merits and drawbacks. Section 3.2 presents the conventional LDO regulator’s components and briefly explains operation theory. In section 3.3, power supply rejection ratio(PSRR) is explained because it is a significantly critical parameter among line and load regulations, PSRR, load current, and voltage dropout since main purposes of using a LDO regulator is to reject the ripple of a switching converter. In addition, section 3.3 illustrates the prior arts of the LDO regulator, followed by summary in section 3.4.
CHAPTER 3. PSRR IMPROVEMENT IN LOW-DROPOUT REGULATOR

3.1 Types of Voltage Regulator

A voltage regulator is a universal component in portable electronics since dc-dc converter is not rarely used to reduce the size of the integrated chip. Sometimes, combination of regulator and converter are used for low ripple. As the usage of portable electronics increases, the regulator are solely used and higher PSRR is required.

3.1.1 Switching Regulator

A switching regulator is known as the most efficient type of regulator. The switching regulator takes in a DC voltage, converts it into high-frequency voltage, then filters AC voltage to convert it back into a DC voltage at the output. While it generates the DC output, it has an AC ripple with its clock frequency. In addition, to filter out the AC ripple, a low-pass filter is placed in parallel with an load at output.

The switching regulator has been implemented with over 90% efficiency, even with the power loss during transistor on and off time [26]. The efficiency is determined as follow:

\[
\eta(\%) = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{in}} - P_{\text{loss}}}{P_{\text{in}}} \cdot 100
\]

(3.1)

where \( P_{\text{loss}} \) is total power dissipation at output and \( P_{\text{in}} \) is total power dissipation at input and, \( P_{\text{loss}} \) defines sum of losses that consists of commutation, driver, and conduction due to non-idealities of passive and active components. Since the switching regulator is AC to DC conversion, it is hard to use to sensitive load in supply voltage. Moreover, size of inductor is inversely proportional to the ripple as follow:

\[
L = \frac{V_L \Delta t}{\Delta i_L}
\]

(3.2)

where \( V_L \) is an inductor voltage and \( \Delta t \) is a time variation in duty cycle (D) and period (T) and, \( \Delta i_L \) is amplitude of current ripple (peak to peak).
Finally, the size of capacitor can be critical and its size is determined as follow:

\[ C = \frac{i_C \Delta t}{\Delta V_C} = \frac{\Delta i_L}{8 \cdot \Delta V_C \cdot \Delta t} \tag{3.3} \]

where \( i_C \) is current of capacitor and \( \Delta t \) is a time variation in duty cycle (D) and period (T) and, \( \Delta V_C \) is amplitude of voltage ripple (peak to peak). Due to bigger size of capacitance and inductance in the low-pass filter, it is hard to implement on-chip application.

### 3.1.2 Linear Regulator

A linear regulator uses a transistor operated in its linear region as a variable resistor in a voltage divider network to obtain the desired output voltage, \( V_{out} \) as shown in Fig. 3.1. When the circuit is no longer sensitive to \( V_{out} \), the system enters the dropout region. One or more transistors enter their ohmic or triode regions, where gain is low. As a result, the loop loses its gain and becomes insensitive and the bias voltage does not adjust with variation of the \( V_{out} \). While the regulator keeps the fixed output voltage, the output voltage has small variation.

The linear regulator is less efficient than switching regulators because the transistor at the output, usually a PMOS, is always dissipating power in the form of heat. Charge pumps are sometimes used to increase efficiency, but they occupy a lot of area and increase the complexity and power consumption of the circuit. However, linear regulators are stable with various loads since the transistor can be continuously adjusted. Also, because linear regulators do not use storage elements to convert between AC and DC voltage, output voltage ripple and noise are lower than switching regulators. For the same reason, linear regulators respond faster than switching regulators to changes in the unregulated supply voltage and load current.
3.2 Conventional Low-Dropout Regulator

3.2.1 Definition of Low-Dropout Regulator

As supply voltage shrinks, the requirement of maintaining high power supply rejection ratio (PSRR) becomes significant in systems-on-chip (SoC) while the supply voltage of LDO is reduced [7]. Moreover, the switching frequency of a DC-DC converter is desired to be high to reduce the size of reactive components, which increases the ripple frequency [11].

A conventional LDO is one of linear regulators that are composed of an error amplifier (EA), a pass transistor, feedback resistors (R1,R2), an output capacitor (CL) and its output capacitance (c_0-a) and resistance (r_0-a) as shown in Fig. 3.2.

Power efficiency and accuracy are important parameters in the design of the LDO. The error amplifier amplifies the voltage difference between the reference and the feedback voltage, and then its output biases the pass transistor. The op-amp keeps same dropout voltage through the feedback voltage between R1 and R2 while changing output load (RL).
CHAPTER 3. PSRR IMPROVEMENT IN LOW-DROPOUT REGULATOR

The LDO regulator output depends on the bandgap reference voltage ($V_{ref}$), $A_{OL}$ (open loop gain of the LDO), $A_{EA}$ (error amplifier gain) as shown in Eq. 3.4:

$$V_{OUT} = \left( \frac{A_{OL}}{1 + A_{OL}} \right)(1 + \frac{R_1}{R_2})(V_{ref} + \frac{V_{in}}{A_{EA}})$$  \hspace{1cm} (3.4)

A dropout voltage ($V_{DO}$) is defined as the difference between the unregulated supply voltage and regulated output voltage. Lowering the dropout voltage can lower the required voltage of the unregulated power supply and the power consumption of the regulator.

A bandwidth is another specification in linear regulator design. It is inversely proportional to op-amp output resistance ($r_o-a$) and capacitance ($c_o-a$) as shown in Eq. 3.5. The higher bandwidth of a regulator, the more quickly it can react to the changes in input and power supply and keep the output voltage constant. High bandwidth also improves the power supply rejection ratio of the regulator. The bandwidth of LDO has to be larger than PLL

![Conventional low dropout regulator structure](image)

Figure 3.2: Conventional low dropout regulator structure
bandwidth in order not to have additional poles \[^7\].

\[ BW_A = \frac{1}{2\pi r_{o-A} c_{o-A}} \quad (3.5) \]

### 3.2.2 Performance Metrics

There are two general categories that evaluate the performance of LDO regulator \[^7\]. One of them is an accuracy of regulator which is line and load regulations, transient response, and power supply rejection (PSR).

A line regulation is a steady-state metric that specifies how much the output changes in response to the input changes, but often pronounced variation in the supply voltage as follow:

\[
\text{Line Regulation} = \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} \quad (3.6)
\]

A load regulation is a measure of the circuits ability to maintain the specified output voltage under varying load conditions. Load regulation is defined by

\[
\text{Load Regulation} = \frac{\Delta V_{\text{out}}}{\Delta I_{\text{in}}} \quad (3.7)
\]

A transient response is the maximum allowable output voltage variation for a load current step change. It is a function of the output capacitor value (\(C_o\)), the equivalent series resistance (ESR) of the output capacitor, the bypass capacitor (\(C_b\)) that is usually added to the output capacitor to improve the load transient response, and the maximum load-current (\(I_{o,max}\)) \[^28\]. The maximum transient voltage variation is defined by

\[
\Delta V_{tr,max} = \frac{I_{o,max}}{C_o + C_b} \cdot \Delta t + \Delta V_{ESR} \quad (3.8)
\]
CHAPTER 3. PSRR IMPROVEMENT IN LOW-DROPOUT REGULATOR

Where ∆t₁ corresponds to the closed loop bandwidth of an LDO regulator. ∆V_{ESR} is the voltage variation resulting from the presence of the ESR (R_{ESR}) of the output capacitor.

PSR or PSRR is defined as how well linear regulators reject noise from \( V_{in} \) to the output voltage as follow:

\[
\text{PSRR} = \frac{1}{A_{in}} = \frac{\Delta V_{in}}{\Delta V_{out}}
\] (3.9)

From a dc-dc converter, an output ripple is usually generated between 10mV_{pk−pk} and 50mV_{pk−pk} with its frequency between 20KHz and 10MHz [7].

Finally, it is a power-conversion efficiency ranges are given as follows:

\[
\eta_c(\text{worst case}) = \frac{I_{load,max} \cdot V_{out}}{(I_{load,max} + I_{Quiescent}) \cdot V_{in,min}}
\] (3.10)

\[
\eta_c(\text{best case}) = \frac{I_{load,max} \cdot V_{out}}{(I_{load,max} + I_{Quiescent}) \cdot (V_{in,min} + V_{DO})}
\] (3.11)

where \( I_{Quiescent} \) is a current which is difference between input and output currents. Low \( I_{Quiescent} \) is necessary to have higher efficiency. These parameters are presented in most researches for evaluating the performance.

3.3 Design Considerations

In the LDO regulator, there are major components, error amplifier, pass transistor, and output capacitor that determine its power supply rejection ratio, bandwidth(BW), and loop stability. Its PSRR and BW are the most important component for mitigation of supply noise. EA and pass transistor have to be carefully chosen based on its application.
3.3.1 General PSRR Analysis

Power supply rejection ratio is a critical factor which is affected by three components limit at high frequency. In order to analyze the regulator, the ac components (parasitic capacitances) of the pass transistor and supply noise path are presented as shown in Fig. 3.3. First, in path 1, the supply noise couples through the error amplifier. Due to injection of supply noise, the output of the error amplifier has a DC offset with its ac ripple. In addition, since current mirrors are used for converting the differential signal to a single-ended signal, asymmetry presented in the circuit is a major issue of the single-ended error amplifier [29]. Most LDOs employing standard single-ended error amplifiers have a limited common mode and supply noise rejection. In addition, to minimize the effects of the supply noise, the loop gain of the regulator has to be increased. Secondly, in path 2, noise modulation of \( V_{dd} \) of the gate voltage through the gate-source capacitance, \( C_{gs} \), converted into current by

![Supply noise path in LDO regulator](image)

Figure 3.3: Supply noise path in LDO regulator
the transconductance of the pass transistor, $g_{mp}$ [29]. The supply noise coupled with the parasitic capacitance that induces a current through the path 2 and then modulates the $V_g$ signal. This path requires a compensation block for increasing error amplifier’s gain [30, 31] or loop stability. Finally, in path 3, the modulation of $V_{dd}$ is coupled with the finite output impedance of the pass transistor, $r_{ds}$, and $C_{db}$ [29]. Since the size of pass transistor is huge, the $r_{ds}$ is small and the current flows to the path 3. Each path in the LDO regulator requires compensation block for better high PSRR regulator.

### 3.3.2 Choice of Error Amplifier

A choice of input transistors in a conventional differential pair is significant to determine its PSRR performance. Moreover, the usage of PMOS and NMOS is different depending on what input signal passes through. A conventional error amplifier which has a NMOS input differential pair with PMOS is shown in Fig. 3.4 (a). To ease the analysis of PSRR, the transistor model is converted to a small signal model as shown in Fig. 3.4 (b). This model is obtained by grounding the input terminals and applying a small signal supply voltage at $V_{dd}$. $R_1$ and $R_2$ represent the channel resistance for PMOS and NMOS, respectively. $2C_{gs}$ represents the parasitic capacitance sitting at the gate of PMOS mirror. Assuming that $g_m$ of the PMOS is large, $C_{gs}$ can be assumed to be short due to $1/g_m$. Then, the $i_{R_2}$ can be written as follow:

$$i_{R_2} = \frac{V_{dd}}{g_m R_2}$$  \hspace{1cm} (3.12)

Since $1/g_m$ is small, $i_{R_2}$ can be approximate to be,

$$i_{R_2} = \frac{V_{dd}}{R_2}$$  \hspace{1cm} (3.13)

Applying superposition in the output node, the output voltage is,

$$V_{out} = V_{dd} \cdot \frac{R_2}{R_1 + R_2} + i_{R_2} \cdot \frac{R_1 \cdot R_2}{R_1 + R_2}$$  \hspace{1cm} (3.14)
CHAPTER 3. PSRR IMPROVEMENT IN LOW-DROPOUT REGULATOR

\[ V_{out} = V_{dd} \cdot \frac{R_2}{R_1 + R_2} + V_{dd} \cdot \frac{R_1}{R_1 + R_2} = V_{dd} \]  \hspace{1cm} (3.15)

Thus, with the assumption that \(1/g_m\) is small, we observe that the entire ripples in the power supply is transferred to the output node of a single stage amplifier. Similar results were obtained when two stage amplifier were considered.

Another conventional error amplifier which has a PMOS input differential pair with NMOS is shown in Fig. 3.5 (a). To ease the analysis of PSRR, the transistor model is converted to a small signal model as shown in Fig. 3.5 (b). With same assumption as above, the \(i_{R2}\) is,

\[ i_{R2} = \frac{V_{dd}}{R_1} \]  \hspace{1cm} (3.16)

\[ V_{out} = V_{dd} \cdot \frac{R_2}{R_1 + R_2} - i_{R2} \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \]  \hspace{1cm} (3.17)

![Diagram of NMOS input error amplifier and its small signal model with supply noise, \(\Delta V_{dd}\)](image)

Figure 3.4: NMOS input error amplifier and its small signal model with supply noise, \(\Delta V_{dd}\)
CHAPTER 3. PSRR IMPROVEMENT IN LOW-DROPOUT REGULATOR

![PMOS input error amplifier and its small signal analysis](image)

Figure 3.5: PMOS input error amplifier and its small signal analysis

\[
V_{\text{out}} = V_{\text{dd}} \cdot \frac{R_2}{R_1 + R_2} - V_{\text{dd}} \cdot \frac{R_1}{R_1 + R_2} = 0 \tag{3.18}
\]

As the result of the Eq. 3.18, there is no ripple from the PMOS transistor with NMOS load to output voltage in PSRR analysis while the NMOS transistor with PMOS load has \( \Delta V_{\text{dd}} \) at the output. We can conclude that PMOS input has higher PSRR than NMOS input. The following Table 3.1 is summary of the input transistor versus its DC PSRR and bandwidth [32].

### 3.3.3 Pass Transistors

Designing in a low voltage and low quiescent current environment causes difficult challenges that contradict performance and stability [33]. A linear regulator’s pass element determines its dropout voltage and quiescent current, which determine the types of applications for which the regulator is suitable. Bipolar transistors have a base current
CHAPTER 3. PSRR IMPROVEMENT IN LOW-DROPOUT REGULATOR

Table 3.1: Comparision of error amplifier architectures

<table>
<thead>
<tr>
<th>Pass Transistor</th>
<th>Error Amplifier Load</th>
<th>DC PSRR</th>
<th>PSRR BW</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>NMOS Mirror</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td></td>
<td>PMOS Mirror</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>NMOS</td>
<td>NMOS Mirror</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td></td>
<td>PMOS Mirror</td>
<td>Low</td>
<td>High</td>
</tr>
</tbody>
</table>

which leads to a higher quiescent current compared to MOS transistors. However, MOS-FETs require a higher voltage supply than BJTs for the same driving current. Furthermore, some configurations exchange dropout voltage by quiescent current like the Darlington configuration\[34\]. Each of the four main pass elements used today has a different transistor and unique characteristics that make it ideal or not so ideal for certain applications \[35\].

![Figure 3.6: Four types of pass elements (a) npn (b) pnp (c) PMOS (d) NMOS](image)

Figure 3.6: Four types of pass elements (a) npn (b) pnp (c) PMOS (d) NMOS
CHAPTER 3. PSRR IMPROVEMENT IN LOW-DROPOUT REGULATOR

First, NPN regulator shown in Fig. 3.6(a) allows high device output current, but the large input to output voltage drop that results from operating the NPN as an emitter follower often requires a substantial heat sink \[34\]. Secondly, PNP regulator shown in Fig. 3.6(b) introduces LDO’s reduction of the input to output voltage drop using a PNP transistor as the pass element. Due to high efficiency than others, it uses as battery powered applications. However, its high output impedance, due to its common emitter configuration, means that an output within a certain range of capacitance and equivalent series resistor (ESR) is required for stability \[7\]. Third, PMOS regulator shown in Fig. 3.6(c) is a popular element in recent architecture that makes dropout voltage low, because the \(r_{ds(on)}\) is easily adjusted to a low value by sizing the transistor. Since PMOS regulator has relatively high gate capacitance, it also requires output capacitor and its ESR. Finally, NMOS regulator, shown in Fig. 3.6(d), is easier to compensate at low loads and dropout due to the higher output impedance of PMOS. Its LDO requires the VDD rail to be higher than Vin, while a PMOS does not. To do this, a charge pump is usually required with accompanying disadvantages of higher quiescent current and extra charge pump noise \[36\].

Each type of linear regulator has its own advantages and disadvantages. Ultimately, it is up to the designer to determine whether a certain type of linear regulator is appropriate for the application based on its dropout voltage, ground current, and stability compensation method requirements.

3.3.4 Pole Compensation For High PSRR

There are three poles, \(\omega_a\) (pole frequency at the amplifier output), \(\omega_i\) (pole frequency at the amplifier input) and \(\omega_o\) (pole frequency at the regulator output), in the conventional LDO regulator. \(\omega_i\) is relatively small input capacitance than other poles and ignored in the PSRR pole analysis. Thus, depending on these poles, its PSRR and bandwidth may be varied as shown in Fig. 3.7.
CHAPTER 3. PSRR IMPROVEMENT IN LOW-DROPOUT REGULATOR

There are two frequency compensation cases, $\omega_a > \omega_o$ and $\omega_a < \omega_o$ for PSRR. The regulator has good PSRR in both cases at low frequency. But, in case of the $\omega_a < \omega_o$, the noise rejection degrades beyond the amplifier pole at the same rate as the loop gain would reduce. Consequently, in order to achieve good supply rejection in the vicinity of the PLL bandwidth, the amplifier output pole, $\omega_o$, should be moved to high frequency. The design requirement incurs severe power penalty $[3, 22]$. Therefore, to secure stability of the regulator, general strategy used for compensating an output-compensated PMOS regulator is to place the output pole at low frequency in order to dominate over all other poles and zeros in the circuit.

Figure 3.7: Power supply rejection ratio curves in conventional LDO
3.4 Prior Arts

To eliminate supply noise, many researchers have proposed the architecture of the LDO regulators. In Fig. 3.8 (a) [37], it shows a 1\textsuperscript{st} order RC filter that reduces the external power supply noise ripple prior to the input of LDO regulator for noisy V\textsubscript{dd}. The method is the simplest way to regulate the supply noise ripple to the input of regulator, but the voltage drop between V\textsubscript{dd} and the input of the regulator is critical since the resistor in RC filter is connected to the regulator. Thus, the power efficiency is too poor to use it.

Another method consisting of two regulators in series is shown in Fig. 3.8 [38] (b). Cascaded regulators of noisy supply voltage are not sufficient in order to satisfy for the size of pass transistor and voltage drop between v\textsubscript{dd} and its output voltage even though the ripple of output voltage is small. The trade-off between area and PSRR is critical.

In Fig. 3.9 (a) [39], it shows a complicated architecture of LDO regulator. The noisy V\textsubscript{DD} is regulated by RC filter and voltage buffer for less wavering a bias voltage to the pass transistor. In this architecture, the cascode device is always on due to the NMOS with its filtered biasing voltage, V\textsubscript{DD}. It causes much power loss since the cascode device is always on and consumes voltage headroom. Even though the charge pumps are sometimes used to increase efficiency, it occupies a lot of area and increases the complexity and power

![Figure 3.8: Prior arts of LDOs](image-url)
In Fig. 3.9(b)\[40\], it presents cascoded regulator consisting of RC filter with NMOS at upside and a conventional regulator at downside. Although the architecture is simpler than others, the voltage headroom is critical due to the NMOS transistor. Since the PMOS transistor is used at downside, it may have limitation of various loads due to voltage headroom.

Finally, Fig. 3.10\[41\] shows a buffered LDO regulator. By using the buffer between error amplifier and pass transistor, isolating EA’s output impedance from pass transistor can be achieved. It potentially increases not only the bandwidth of regulator and but also fast transient response to bias the pass transistor gate voltage. But, due to an additional pole between buffer and pass transistor, phase margin may be narrowed.
3.5 Summary

This chapter discussed the basic concept of a linear regulator, its operation theory, and design considerations of each component such as error amplifier’s input transistor, pole location, and pass elements for high PSRR.

A switching regulator has higher power efficiency than others. On the other hand, due to the large passive elements in low-pass filter, the linear regulator has higher preference on its usage. Furthermore, the linear regulators are stable with various loads since the transistor can be continuously adjusted. According to [7], as supply voltage shrinks, the requirement of maintaining high power supply rejection ratio (PSRR) becomes significant in systems-on-chip (SoC) while the supply voltage of LDO regulator is reduced. For high PSRR regulator, the design considerations of the regulator are as following: a PMOS input differential pair with NMOS load has more powerful power supply rejection ratio than a NMOS input differential pair through the PSRR analysis. To evaluate the performance of
CHAPTER 3.  PSRR IMPROVEMENT IN LOW-DROPOUT REGULATOR

LDO regulator, performance metrics are presented such as line and load regulation, transient response, and PSRR.
Chapter 4

Proposed Design of Supply-Regulated PLL

The proposed LDO regulator, used to reduce supply noise in the PLL, is presented in this chapter. The proposed low-dropout regulator with enhanced gain of an error amplifier provides a clean power supply voltage to the PLL by subtracting pass transistor control voltage ripple from power supply noise.

Section 4.1 presents proposed LDO regulator with its components and PSRR analysis. In section 4.2 and 4.3, a current starved voltage controlled oscillator and active loop filter are shown, respectively. In section 4.4, bandgap voltage reference is presented for the regulator’s reference voltage.

4.1  Design of Proposed Low Dropout Regulator

A conceptual block diagram of the proposed LDO regulator is shown in Fig. 4.1(a). The proposed LDO regulator consists of gain compensation, error amplifier, zero compensation, pass transistor, and feedback blocks. In Fig. 4.1(b) gain compensation and pole...
Figure 4.1: Proposed LDO regulator
compensation blocks are presented to get its high PSRR and wide phase margin. The gain compensation block consists of cascaded common source amplifier which consists of NMOS-input/NMOS-load common source followed by PMOS-input/NMOS-load configuration. The gain of the compensation stage leads to follows

\[ A_{v1st} = -\frac{g_{m21}}{g_{m20}} \]  
\[ A_{v2nd} = -\frac{g_{m22}}{g_{m23}} \]  
\[ A_v = \frac{g_{m21} \cdot g_{m20}}{g_{m20} \cdot g_{m23}} \]

where, \( g_{mxx} \) is transconductance of each transistor. According to [29], large gain of the loop increases the regulator’s PSRR. Therefore, lack of error amplifier’s gain is strengthened by the gain stage.

An error amplifier is one of the components in the regulator. The gain of the error amplifier determines the regulator’s PSRR. Therefore, the error amplifier (EA) should have high gain for the high PSRR. Fig. 4.2(a) describes a folded cascode amplifier that provides 71 dB of gain, and its gain is easily adjusted by changing \( R_{out} \). To reduce supply noise, the EA also requires high output swing since pass transistor biasing voltage, \( V_g \), should have the same amplitude as the supply noise in order to subtract pass transistor control voltage ripple from power supply noise. By using self-biased the op-amplifier, it is possible to obtain output swing between \( V_{out(min)} \) of \( 2\sqrt{2} V_{DS(sat)} \) and \( V_{out(max)} \) of \( V_{DD} - 2V_{DS(sat)} \). In addition, the gain of the amplifier can be written as follow:

\[ A_v = \frac{V_{out}}{V_{in}} = g_{m1} \cdot R_{out} \]  

where, \( R_{out} \) is \( (r_{ds2R} + r_{ds3R}) \parallel (r_{ds4R} + r_{ds5R}) \) and \( g_{m1} \) is transconductance of the input PMOS transistor.

EA’s biasing voltage generator is shown in Fig. 4.2(b). A current, flowing through \( M_6 \), is mirrored with 1:1 ratio through \( M_{10} \). All the transistors are in deep saturation region in
CHAPTER 4. PROPOSED DESIGN OF SUPPLY-REGULATED PLL

Figure 4.2: A folded cascode operational amplifier and its biasing voltage in the regulator

(a) transistor level of folded cascode operational amplifier

(b) bias voltage generator
Figure 4.3: Small-signal equivalent circuit of the proposed regulator for stability analysis

To minimize effects of process variations and modulation of $V_{dd}$, the biasing voltages, $V_{BP1}$, $V_{BP2}$, and $V_{BN1}$, have to be the same voltage for high swing of its output signal as shown in Fig. 4.2(a), respectively.

Fig. 4.3 shows small-signal equivalent circuit of the proposed regulator for stability analysis. The regulator can be represented as 4 gain stages, output resistance, and capacitance of each stage. A loop gain of the regulator can be written as follow

$$L(s) = \frac{g_{mea} \left( r_{o2R} + r_{o3R} \right) \left( r_{o4R} + r_{o5R} \right)}{\left( r_{o2R} + r_{o3R} \right) \left( r_{o4R} + r_{o5R} \right)} \left( g_{m21} \left( g_{m22} \left( g_{mp} \cdot R_L \cdot \beta(s) \right) \left( 1 + s \left( C_{oa} \right) \right) \left( 1 + \frac{sC_1}{g_{m20}} \right) \left( 1 + \frac{sC_2}{g_{m23}} \right) \left( 1 + sR_L C_L \right) \right) \right. \left( 1 + s \left( C_{oa} \right) \right) \left( 1 + \frac{sC_1}{g_{m20}} \right) \left( 1 + \frac{sC_2}{g_{m23}} \right) \left( 1 + sR_L C_L \right)$$

The loop gain has four poles and one zero due to $\beta(s)$ in the loop gain as shown in the Eq. 4.5. The pole at the LDO output $P_4$ is the dominant pole of the loop. The poles at the outputs $P_2$ and $P_3$ of the second and third stages can be neglected because they are at high frequency. Due to the high gain of the folded cascode error amplifier, its phase margin causes unstable output signal. In addition, the zero is located at low frequency. To compensate the zero, the compensation capacitor, $C_Z$, is located between the error amplifier’s input and output as shown in Fig. 4.1(b).
CHAPTER 4. PROPOSED DESIGN OF SUPPLY-REGULATED PLL

4.2 Design of Current-Starved VCO

A core component in PLL is a ring oscillator which is comprised of a number of delay stages, with the last output stage fed back to the first input stage. To achieve oscillation, the inverter chain must provide a phase shift of $\pi$ and have unity voltage gain at the oscillation frequency. This current starved VCO is designed using ring oscillator and its operation is also similar to that. From the schematic circuit shown in the Fig. 4.4, it is observed that $M_{24}$ and $M_{25}$ operate as current source and mirror to $M_{26}$ and $M_{28p}$. The current sources, $M_{28p}$ and $M_{28n}$, limit the current available to the inverters; in other words, the inverter is starved for the current. The MOSFETs $M_{25}$ and $M_{24}$ drain currents are the same and set by input control voltage. The R is added for enhancing linearity of the VCO. The oscillation frequency of the CSVCO can be written as follow

$$f_{osc} = \frac{1}{N \cdot (t_1 + t_2)} = \frac{I_D}{N \cdot C_{tot} \cdot V_{DD}} \quad (4.6)$$

![Figure 4.4: A current starved voltage controlled oscillator](image-url)
CHAPTER 4. PROPOSED DESIGN OF SUPPLY-REGULATED PLL

where, \( N \) is number of stage in the VCO, \( C_{tot} = C_{out} + C_{in} = \frac{5}{2} C'_{ox}(W_pL_p+W_nL_n) \), \( t_1 = C_{tot} \cdot \frac{V_{SP}}{I_{D28p}} \) and \( t_2 = C_{tot} \cdot \frac{V_D-D-V_{SP}}{I_{D28n}} \).

The CSVCO is preferred in this thesis because the output frequency of the conventional VCO is not stable when it is dependent on noisy \( V_{dd} \). Therefore, it is made stable by supplying current to each inverter by the control voltage and \( V_{dd} \) instead of only one \( V_{dd} \).

4.3 Design of Active Loop Filter

A loop filter is common architecture of PLL that affects the dynamic characteristics of PLL such as bandwidth, lock ranges, and transient response. Resistor and Capacitor are widely used for loop filter in PLL since passive devices have high quality factor and they are very reliable. But, an active loop filter is used rather than passive filter for small passive components size in this thesis.

![Two-pole low-pass butterworth filter](image)

Figure 4.5: Two-pole low-pass butterworth filter
In Fig. 4.5, a 1st order Butterworth low-pass filter is presented. Transfer function of the ALF is written as follows:

\[ T(s) = \frac{\frac{1}{R}}{\frac{1}{R} + sC_2\left(\frac{2}{R} + sC_1\right)} = \frac{1}{1 + sR \cdot C_2(2 + sR \cdot C_1)} \]  (4.7)

In Eq. 4.7, \( s = j\omega = 0 \) is equal to 1 at zero frequency while \( s = j\omega = \infty \) is equal to 0 at high frequency. The filter is a maximally flat magnitude filter and its transfer function is designed such that the magnitude of the transfer function is as flat as possible within the passband of the filter [42]. The magnitude of the transfer function is

\[ |T(s)| = \left[(1 - \omega^2 \tau_1 \tau_2)^2 + (2\omega \tau_2)^2\right]^{-\frac{1}{2}} \]  (4.8)

where \( \tau_1 \) is \( R \cdot C_1 \) and \( \tau_2 \) is \( R \cdot C_2 \).

For a maximally flat filter, which defines the Butterworth filter, we set

\[ \frac{d|T|}{d\omega}\bigg|_{\omega=0} = 0 \]  (4.9)

Taking derivative and setting the derivative equal to zero at \( \omega = 0 \) yields

\[ \frac{d|T|}{d\omega}\bigg|_{\omega=0} = 4\omega \tau_2 [1 - \omega^2 \cdot \tau_1 \cdot \tau_2 + 2\tau_2] \]  (4.10)

Eq. 4.6 is satisfied when \( 2\tau_2 = \tau_1 \) or \( 2C_1 = C_2 \). For this condition, the transfer function is

\[ |T| = \frac{1}{[1 + 4(\omega \tau_4)^4]^\frac{1}{2}} \]  (4.11)

Its cutoff frequency is \( \omega_{3dB} = 2\pi f_{3dB} = \frac{1}{\tau_2 \sqrt{2}} = \frac{1}{\sqrt{2}RC_2} \). \( C_2 \) becomes 0.707\( C \) since general \( \omega_{3dB} = \frac{1}{RC} \). Finally, the transfer function is
\[ |T| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_{\text{sat}}}ight)^4}} \]  
\[ (4.12) \]

In the active low-pass filter, R, C_1, C_2 are 100\,\Omega, 20.48\,\text{pF}, and 10.24\,\text{pF}, respectively.

### 4.4 Bandgap Voltage Reference

A general purpose of voltage reference is a circuit used to generate a fixed voltage, V_{\text{REF}}, that is independent of the power supply voltage V_{DD}, temperature, and process variations [2]. Most cases of the voltage reference, V_{\text{REF}} varies with temperature. The temperature coefficient of the proportional to absolute temperature (PTAT) and complimentary to absolute temperature (CTAT) are canceled each other for a static voltage called a bandgap voltage reference. If the reference voltage increases with increasing temperature, it can be said PTAT while the reference voltage decreases with temperature, it is called CTAT. To get a fixed reference voltage, it is important to find a certain point that sum of positive slope of the PTAT and negative slope of CTAT references becomes zero, causing very little change of the voltage with temperature variations.

A self-biased bandgap reference is shown in Fig.4.6. The pnp BJTs, D_1 and D_2 together with the resistor, R_{bgr2}, form a PTAT current generator. To provide a CTAT current, additional resistor, R_{bgr1}, is placed to sum with the PTAT current. As temperature increase, the diode voltage decreases, causing the current through R_{bgr2} to decrease CTAT. Therefore, the PTAT current is

\[ I_{\text{PTAT}} = \frac{n \cdot V_T \cdot \ln K}{R_{bgr2}} \]  
\[ (4.13) \]

where, V_T is thermal voltage, K is number of pnp BJTs and n is emission coefficient. In addition, the CTAT current is written as follow:
CHAPTER 4. PROPOSED DESIGN OF SUPPLY-REGULATED PLL

\[ I_{CTAT} = \frac{V_{D1}}{R_{bgv1}} \]  

(4.14)

The total current is driven through the \( R_{bgv3} \) to generate the reference voltage

\[ V_{REF} = nV_T \cdot N \cdot \ln K + \frac{N}{L} \cdot V_{D1} \]  

(4.15)

The temperature behavior of the BGR is

\[ \frac{\partial V_{REF}}{\partial T} = n \cdot N \cdot \ln K \cdot \frac{\partial V_T}{\partial T} + \frac{N}{L} \cdot \frac{\partial V_{D1}}{\partial T} \]  

(4.16)

For zero TC, we get an L and N from the Eq. \( 4.12 \). The resistor, \( R_{bgv1}(489k\Omega) \), is L (9.4) \( \cdot R_{bgv2}(52k\Omega) \).

4.5 Summary

For mitigation of supply noise in PLL, the LDO regulator is proposed. In the regulator, a folded cascode amplifier is used as error amplifier for high voltage gain. Since the error
amplifier do not satisfy infinite gain, compensation gain block is needed for high PSRR. The lack of the voltage gain is replenished by additional gain stages, cascaded common source amplifiers, between the error amplifier’s output and pass transistor. In the proposed LDO regulator, there are 4 poles and one zero but, $P_2$, $P_3$ can be negligible since two dominant poles, $P_1$, $P_4$ are existed. According to [29], the large gain of the loop increases the regulator’s high PSRR. But, due to high gain of error amplifier, the frequency response of the regulator is located on unstable region or narrowed phase margin. Thus, additional capacitor is placed between error amplifier’s output and input in order to push zero to high frequency.
Chapter 5

Simulation Results

5.1 Proposed LDO regulator

5.1.1 Bandgap Voltage Reference

The bandgap voltage reference is used for biasing fixed voltage of the error amplifier. Its voltage output has to be fixed with various conditions such as process, voltage, and temperature (PVT). Fig. 5.1 shows its output voltage, $V_{\text{ref}}$, with process (FF,TT,SS), voltage (0~1.2V), and temperature (0~100°C). We set up the peak to peak of supply noise as 100mV$_{\text{pk-pk}}$ and $V_{\text{ref}}$ as 0.5V. Therefore, the biasing voltage variation should be small within the range between 0.9mV and 1.1V. $V_{\text{ref}}$ versus $V_{DD}$ of FF corner is shown in Fig. 5.1(a). The variation of $V_{\text{ref}}$ at 1V and between 0.9V and 1.1V are 5.56mV and 4.15mV, respectively. In case of TT corner, $V_{\text{ref}}$ versus $V_{DD}$ curve is shown in Fig. 5.1(b). The variation of $V_{\text{ref}}$ at 1V and the injected supply noise range are 11mV and 3.2mV, respectively. Finally, $V_{\text{ref}}$ versus $V_{DD}$ of SS corner is shown in Fig. 5.1(c). The variation of $V_{\text{ref}}$ at 1V and the injected supply noise range are 3mV and 1mV, respectively.
CHAPTER 5. SIMULATION RESULTS

(a) $V_{ref}$ with PVT variation in FF corner

(b) $V_{ref}$ with PVT variation in TT corner

(c) $V_{ref}$ with PVT variation in SS corner

Figure 5.1: Bandgap voltage reference output voltage with various PVTs
CHAPTER 5. SIMULATION RESULTS

5.1.2 Error Amplifier

Folded cascode amplifier simulation is shown in Fig. 5.2. The error amplifier is designed with conventional PMOS input folded cascode operational amplifier for high PSRR. The error amplifier has relatively high gain of 71dB which is higher than the differential pairs as shown in Fig 5.2(a). The zero shown in Fig 5.2(b) is close to its injected supply noise causing unstable its output and low mitigation of supply noise in the regulator. In addition, its phase and unity gain bandwidth are -49° and 70MHz, respectively. According to gain bandwidth product, the gain of the amplifier has to be lowered for stable output. In the phase curve, the phase margin is secured at the right locations. But, zero exists at 70MHz. Due to the location of zero, the zero compensation capacitor is placed between its input and output in the proposed regulator. The capacitor makes the zero push to high frequency.

5.1.3 Loop Gain, Phase, and PSRR

Fig. 5.3 shows its loop gain and phase margin simulations carried with different load conditions between 100µA and 40mA and output load capacitor (100pF). In addition, supply noise is injected to the LDO regulator with 100KHz frequency sine wave and 100mV_{pk−pk}. Fig. 5.3(a) shows loop gain of the proposed regulator. The loop gain of the regulator is 83dB at low frequency and 68dB at the supply noise frequency with the PLL load, 766µA. With 40mA load, it is 60dB at low frequency and 51dB at the supply noise frequency. In case of full load, the bandwidth of the regulator is less than the supply noise frequency. At the full load, the output of the regulator may have wide peak to peak range. But, the regulator is designed for usage of the PLL application. The average current of the PLL is 800 µA. The amount of the load current that the regulator can generate depends on the size of pass transistor. For the purpose of regulating supply noise in the PLL, the pass transistor should be less size. Furthermore, the bandwidth of the regulator is acceptable with 100KHz supply noise. The PSRR and its bandwidth, shown in Fig. 5.4, is similar to the 0A load condition at
CHAPTER 5. SIMULATION RESULTS

Figure 5.2: Error amplifier’s loop gain and phase margin
CHAPTER 5. SIMULATION RESULTS

Figure 5.3: The proposed LDO regulator’s loop gain and phase margin with various loads
CHAPTER 5. SIMULATION RESULTS

Figure 5.4: PSRR of LDO regulator

the PLL average current.

5.1.4 Load transient

Even though the stability is checked with the help of the open loop AC response, it’s always wise to check the stability through transient response. The supply noise is injected to the power of the regulator. Load transient simulation with its output capacitor is shown as Fig. 5.5 for load current switching between 100µA and 40mA. The output signal is backed to stable signal 6.37µs after changing load current. Fig. 5.6 shows the load current switching between 40mA and 100µA. The results are shown in Fig. 5.5(a), Fig. 5.5(b), Fig. 5.6(a) and Fig. 5.6(b).
CHAPTER 5. SIMULATION RESULTS

Figure 5.5: Load transient 100\(\mu\)A to 40mA
Figure 5.6: Load transient 40mA to 100µA
CHAPTER 5. SIMULATION RESULTS

5.2 Phase Locked Loop

5.2.1 Active Low-pass Filter

The ALF suppresses supply noise ripple for VCO’s control voltage. If the ripple of the control voltage is high, it causes high output jitter in the PLL. Fig. 5.7 shows the transfer function of the ALF. The gain transfer function shown in Fig. 5.7(a) is low-pass filter that mitigates beyond 100KHz noise in order to control accurate VCO’s frequency. Fig. 5.7(b) shows its phase of 49° at the corner frequency and it provides a wide phase margin. The wide phase margin generates stable output. The unity gain bandwidth is 41.5MHz. The comparison between passive and active filters is shown in Fig. 5.8. The 1st order active filter has better ripple mitigation, 654µV_{pk−pk}, as shown in Fig. 5.8(a) while the 1st order passive filter has 2.82mV_{pk−pk} of ripple as shown in 5.8(b).

5.2.2 Divider and PFD

The divider and the phase frequency detector’s delay should be less in order to compare accurately divided frequency with the reference frequency to generate the up and down pulses. The T_{p,div}, the propagation delay of the divider, is equal to 98.9 ps as shown in Fig. 5.9(a). The PFD’s T_{p,PFD} is 668.7 ps which is sum of t_{pLH} (169.7ps) and t_{pHL} (499ps) as shown in Fig. 5.9(b). The PFD has long propagation delay than divider since the PFD should generate short output pulse either up or down to reset next incoming clock cycle.

5.2.3 Jitter

The critical parameter that evaluates the PLL performance is the output jitter. The jitter is simulated by two different conditions as shown in Fig. 5.11. First, Fig. 5.11(a) shows the output jitter without the proposed LDO regulator. The peak to peak jitter is about 44.9ps.
CHAPTER 5. SIMULATION RESULTS

Figure 5.7: ALF transfer function

(a) Gain

(b) Phase
CHAPTER 5. SIMULATION RESULTS

Figure 5.8: Comparison passive and active filters’ ripple

(a) 1st order passive filter

(b) 1st order active filter
(a) Divider

(b) PFD

Figure 5.9: Propagation delays in Divider and PFD
CHAPTER 5. SIMULATION RESULTS

Table 5.1: Comparison with the Prior Arts

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<th>[18]</th>
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<td>65 nm</td>
<td>180 nm</td>
<td>130nm</td>
<td>110 nm</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.8 V</td>
<td>1.0V</td>
<td>1.8 V</td>
<td>1.0V</td>
<td>1V</td>
</tr>
<tr>
<td>Supply Noise</td>
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<td>50mV</td>
<td>N/A</td>
<td>10mV @ 1MHz</td>
<td>100mV @ 100KHz</td>
</tr>
<tr>
<td>Operating Frequency</td>
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<td>N/A</td>
<td>0.5 - 2.5GHz</td>
<td>0.5 - 2.5GHz</td>
<td>0 - 2.2GHz</td>
</tr>
<tr>
<td>Jitter_{rms}</td>
<td>5.2ps</td>
<td>4.82ps</td>
<td>3.29ps</td>
<td>3.95ps</td>
<td>N/A</td>
</tr>
<tr>
<td>Jitter_{pk−pk}</td>
<td>41ps</td>
<td>38ps</td>
<td>N/A</td>
<td>N/A</td>
<td>17.2ps</td>
</tr>
<tr>
<td>Total Power</td>
<td>3.3mW @ 1.5GHz</td>
<td>0.99mW @ 1.6GHz</td>
<td>25mW @ 2.4GHz</td>
<td>9.6mW @ 1.4GHz</td>
<td>0.944mW @ 1.6GHz</td>
</tr>
</tbody>
</table>

Secondly, Fig. 5.11(b) shows the jitter with the proposed LDO regulator. The output jitter is significantly reduced to 4.6ps, which is significant reduction by 90% from 44.9ps of the PLL without the proposed LDO regulator. In addition, the proposed supply regulation on LDO and ALF consumes a low power compared to other prior arts as shown in Table. 5.1. Fig. 5.10 presents the Monte Carlo simulation with 10 samples of orthogonal process variations. The jitter_{pk−pk} is 17.2ps.
CHAPTER 5. SIMULATION RESULTS

(a) Jitter without the proposed LDO regulator and ALF

(b) Jitter with the proposed LDO regulator and ALF

Figure 5.11: Output jitter in PLL
Chapter 6

Conclusion

This thesis demonstrates a 1.6GHz supply-regulated PLL design using active Butterworth low pass filter and high power supply rejection ratio LDO regulator in 110nm standard CMOS technology with 1.0V power supply. The regulator output is 0.8V which supplies to all the PLL blocks. For low output jitter, supply noise is regulated by the proposed LDO regulator which is enhanced high PSRR and wide phase margin by cascade common source amplifier and zero compensation capacitor. In the PLL, the output jitter $\Delta t_{pk−pk}$ is significantly reduced to 4.6ps, which is significant reduction by 90% from 44.9ps of the PLL without the proposed LDO regulator. By using monte carlo simulation with 10 times orthogonal process variations, the jitter $\Delta t_{pk−pk}$ is 17.2ps The power consumption of the proposed supply regulation on overall circuit is 0.578mW at 0.8V internal PLL power supply voltage including 1.0V LDO regulators power supply voltage. The proposed supply regulation on LDO and ALF consumes a low power compared to other prior arts as shown in Table. 5.1 It is demonstrated that our proposed scheme is a viable solution for high frequency and low power applications.
Bibliography


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Appendix A

SPICE netlist for A Low Jitter PLL using Active Loop Filter and Low Dropout Regulator

// Generated for: HspiceD
// Generated on: May 20 16:45:31 2015
// Design library name: LDO

// Design cell name: ripple cancellation
// Design view name: schematic
// Library name: LDO
// Cell name: ErrorAmplifier Test
// View name: schematic
subckt ErrorAmplifier Test GND VDD Vin Vout Vref
R0 (VDD VB3) resistor r=20K
PM6 (VBN2 VB VDD VDD) pch w=(2.457u) l=246n as=737.1f ad=737.1f
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

```
ps=5.514u pd=5.514u nrd=122.1m nrs=122.1m sa=300n sb=300n
m=(1)*(1)
PM0 (VB VB VDD VDD) pch w=(5.85u) l=246n as=1.755p ad=1.755p ps=12.3u
pd=12.3u nrd=51.2821m nrs=51.2821m sa=300n sb=300n m=(1)*(1)
PM90 (Vout VBP2 net47 VDD) pch w=(22.5u) l=2.172u as=6.75p ad=6.75p
ps=45.6u pd=45.6u nrd=13.3333m nrs=13.3333m sa=300n sb=300n
m=(1)*(1)
PM94 (net47 VBP1 VDD VDD) pch w=(4.5u) l=2.172u as=1.35p ad=1.35p
ps=9.6u pd=9.6u nrd=66.6667m nrs=66.6667m sa=300n sb=300n
m=(1)*(1)
PM4 (net036 VBP1 VDD VDD) pch w=(900n) l=246n as=159.545f ad=159.545f
ps=1.33636u pd=1.33636u nrd=196.97m nrs=196.97m sa=1.689u
sb=1.689u m=(1)*(11)
PM3 (VBPI VBP2 net036 VDD) pch w=(900n) l=246n as=156.6f ad=148.5f
ps=1.308u pd=1.23u nrd=183.333m nrs=193.333m sa=3.74985u
sb=3.74985u m=(1)*(30)
PM2 (VBP2 VBP2 VDD VDD) pch w=(1.755u) l=246n as=526.5f ad=526.5f
ps=4.11u pd=4.11u nrd=170.94m nrs=170.94m sa=300n sb=300n
m=(1)*(1)
PM91 (net37 VBP2 net48 VDD) pch w=(22.5u) l=2.172u as=6.75p ad=6.75p
ps=45.6u pd=45.6u nrd=13.3333m nrs=13.3333m sa=300n sb=300n
m=(1)*(1)
PM96 (net48 VBP1 VDD VDD) pch w=(4.5u) l=2.172u as=1.35p ad=1.35p
ps=9.6u pd=9.6u nrd=66.6667m nrs=66.6667m sa=300n sb=300n
m=(1)*(1)
PM92 (net46 Vref net31 VDD) pch w=(10.8u) l=912n as=3.24p ad=1.782p
```
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

ps=22.2u pd=11.13u nrd=15.2778m nrs=27.7778m sa=643.97n sb=643.97n
m=(1)*(2)

PM95 (net31 VB VDD VDD) pch w=(21.6u) l=2.262u as=6.48p ad=6.48p
ps=43.8u pd=43.8u nrd=13.8889m nrs=13.8889m sa=300n sb=300n
m=(1)*(1)

PM93 (net45 Vin net31 VDD) pch w=(10.8u) l=912n as=3.24p ad=1.782p
ps=22.2u pd=11.13u nrd=15.2778m nrs=27.7778m sa=643.97n sb=643.97n
m=(1)*(2)

PM1 (VBN1 VB VDD VDD) pch w=(2.457u) l=246n as=737.1f ad=737.1f
ps=5.514u pd=5.514u nrd=122.1m nrs=122.1m sa=300n sb=300n
m=(1)*(1)

NM4 (VB3 VB3 GND GND) nch w=(135n) l=246n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

NM0 (VBP2 VB3 GND GND) nch w=(135n) l=246n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

NM3 (VBP1 VB3 GND GND) nch w=(135n) l=246n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

NM56 (Vout VBN1 net46 GND) nch w=(4.5u) l=2.442u as=1.35p ad=1.35p
ps=9.6u pd=9.6u nrd=66.6667m nrs=66.6667m sa=300n sb=300n
m=(1)*(1)

NM53 (net46 net37 GND GND) nch w=(1.215u) l=2.442u as=364.5f ad=364.5f
ps=3.03u pd=3.03u nrd=246.914m nrs=246.914m sa=300n sb=300n
m=(1)*(1)
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

NM2 (VBN1 VBN1 GND GND) nch w=(135n) l=246n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

NM1 (VB VB3 GND GND) nch w=(135n) l=246n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

NM55 (net37 VBN1 net45 GND) nch w=(4.5u) l=2.442u as=1.35p ad=1.35p
ps=9.6u pd=9.6u nrd=66.6667m nrs=66.6667m sa=300n sb=300n
m=(1)*(1)

NM54 (net45 net37 GND GND) nch w=(1.215u) l=2.442u as=364.5f ad=364.5f
ps=3.03u pd=3.03u nrd=246.914m nrs=246.914m sa=300n sb=300n
m=(1)*(1)

NM5 (VBN2 VBN2 GND GND) nch w=(135n) l=246n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

ends ErrorAmplifier Test

// End of subcircuit definition.

// Library name: LDO
// Cell name: buffer OpAmp
// View name: schematic
subckt buffer OpAmp GND VDD Vin Vout
NM3 (net2 net2 GND GND) nch w=(900n) l=246n as=172.8f ad=148.5f
ps=1.464u pd=1.23u nrd=183.333m nrs=213.333m sa=1.56819u
sb=1.56819u m=(1)*(10)

NM2 (net7 net2 GND GND) nch w=(900n) l=1.812u as=172.8f ad=148.5f
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

```
ps=1.464u pd=1.23u nrd=183.333m nrs=213.333m sa=4.48249u
sb=4.48249u m=(1)*(10)
NM1 (Vout Vout net7 0) nch w=(1.8u) l=246n as=540f ad=540f ps=4.2u
pd=4.2u nrd=166.667m nrs=166.667m sa=300n sb=300n m=(1)*(1)
NM0 (net6 Vin net7 0) nch w=(1.8u) l=246n as=540f ad=540f ps=4.2u
pd=4.2u nrd=166.667m nrs=166.667m sa=300n sb=300n m=(1)*(1)
PM1 (net6 net6 VDD VDD) pch w=(900n) l=246n as=172.8f ad=172.8f
ps=1.464u pd=1.464u nrd=213.333m nrs=213.333m sa=922.985n
sb=922.985n m=(1)*(5)
PM0 (Vout net6 VDD VDD) pch w=(900n) l=246n as=172.8f ad=172.8f
ps=1.464u pd=1.464u nrd=213.333m nrs=213.333m sa=922.985n
sb=922.985n m=(1)*(5)
R0 (VDD net2) resistor r=CS res
ends buffer OpAmp
// End of subcircuit definition.
// Library name: LDO
// Cell name: BGR
// View name: schematic
subckt BGR GND VDD Vref
PM8 (VDD v1 VDD VDD) pch w=(135n) l=246n as=47.79f ad=44.145f ps=708n
pd=654n nrd=2.42222 nrs=2.62222 sa=2.92995u sb=2.92995u m=(1)*(20)
PM7 (Vref v1 VDD VDD) pch w=(135n) l=246n as=47.79f ad=44.145f ps=708n
pd=654n nrd=2.42222 nrs=2.62222 sa=2.92995u sb=2.92995u m=(1)*(20)
PM6 (net18 v1 VDD VDD) pch w=(135n) l=246n as=47.79f ad=44.145f
ps=708n pd=654n nrd=2.42222 nrs=2.62222 sa=2.92995u sb=2.92995u
m=(1)*(20)
```
PM4 (net15 net15 VDD VDD) pch w=(135n) l=246n as=47.79f ad=44.145f
ps=708n pd=654n nrd=2.42222 nrs=2.62222 sa=2.92995u sb=2.92995u
m=(1)*(20)
PM3 (v1 net15 VDD VDD) pch w=(135n) l=246n as=47.79f ad=44.145f
ps=708n pd=654n nrd=2.42222 nrs=2.62222 sa=2.92995u sb=2.92995u
m=(1)*(20)
PM2 (net20 v1 VDD VDD) pch w=(135n) l=246n as=47.79f ad=44.145f
ps=708n pd=654n nrd=2.42222 nrs=2.62222 sa=2.92995u sb=2.92995u
m=(1)*(20)
PM1 (net20 net9 v1 VDD) pch w=(135n) l=129n as=51.435f ad=44.145f
ps=762n pd=654n nrd=2.42222 nrs=2.82222 sa=1.47534u sb=1.47534u
m=(1)*(10)
PM0 (net9 v1 VDD VDD) pch w=(135n) l=246n as=47.79f ad=44.145f ps=708n
pd=654n nrd=2.42222 nrs=2.62222 sa=2.92995u sb=2.92995u m=(1)*(20)
NM4 (net15 net18 net16 GND) nch w=(135n) l=246n as=51.435f ad=44.145f
ps=762n pd=654n nrd=2.42222 nrs=2.82222 sa=1.69745u sb=1.69745u
m=(1)*(10)
NM2 (net16 net15 GND GND) nch w=(135n) l=1.182u as=51.435f ad=44.145f
ps=762n pd=654n nrd=2.42222 nrs=2.82222 sa=3.44321u sb=3.44321u
m=(1)*(10)
NM1 (v1 net20 net16 GND) nch w=(135n) l=246n as=51.435f ad=44.145f
ps=762n pd=654n nrd=2.42222 nrs=2.82222 sa=1.69745u sb=1.69745u
m=(1)*(10)
NM0 (net9 net9 GND GND) nch w=(135n) l=11.712u as=51.435f ad=44.145f
ps=762n pd=654n nrd=2.42222 nrs=2.82222 sa=22.8733u sb=22.8733u
m=(1)*(10)
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

R3 (net18 net024) resistor r=244.5K
R0 (Vref GND) resistor r=150K
R4 (net024 GND) resistor r=244.5K
R2 (net028 GND) resistor r=244.5K
R5 (net18 net24) resistor r=52K
R1 (net20 net028) resistor r=244.5K
Q1 (GND GND net24) pnp 2 m=20
Q0 (GND GND net20) pnp 2 m=1
ends BGR
// End of subcircuit definition.

// Library name: PLL
// Cell name: nand2
// View name: schematic

subckt nand2 GND VDD a b z

PM0 (z a VDD VDD) pch w=(135n) l=129n as=80.595f ad=44.145f ps=1.194u
pd=654n nrd=2.42222 nrs=4.42222 sa=485.097n sb=485.097n m=(1)*(2)
PM1 (z b VDD VDD) pch w=(135n) l=129n as=80.595f ad=44.145f ps=1.194u
pd=654n nrd=2.42222 nrs=4.42222 sa=485.097n sb=485.097n m=(1)*(2)
NM1 (net35 b GND GND) nch w=(135n) l=129n as=80.595f ad=44.145f
ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=485.097n sb=485.097n
m=(1)*(2)
NM0 (z a net35 GND GND) nch w=(135n) l=129n as=80.595f ad=44.145f
ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=485.097n sb=485.097n
m=(1)*(2)
ends nand2
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

// End of subcircuit definition.
// Library name: PLL
// Cell name: nand3
// View name: schematic

subckt nand3 GND VDD a b c z
NM2 (net014 c GND GND) nch w=(135n) l=129n as=56.295f ad=56.295f ps=834n pd=834n nrd=3.08889 nrs=3.08889 sa=628.706n sb=628.706n m=(1)*(3)
NM0 (z a net39 GND) nch w=(135n) l=129n as=56.295f ad=56.295f ps=834n pd=834n nrd=3.08889 nrs=3.08889 sa=628.706n sb=628.706n m=(1)*(3)
NM1 (net39 b net014 GND) nch w=(135n) l=129n as=56.295f ad=56.295f ps=834n pd=834n nrd=3.08889 nrs=3.08889 sa=628.706n sb=628.706n m=(1)*(3)
PM2 (z c VDD VDD) pch w=(135n) l=129n as=80.595f ad=44.145f ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=485.097n sb=485.097n m=(1)*2
PM0 (z a VDD VDD) pch w=(135n) l=129n as=80.595f ad=44.145f ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=485.097n sb=485.097n m=(1)*2
PM1 (z b VDD VDD) pch w=(135n) l=129n as=80.595f ad=44.145f ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=485.097n sb=485.097n m=(1)*2
ends nand3
// End of subcircuit definition.

// Library name: PLL
// Cell name: dff
// View name: schematic

subckt dff D GND Q VDD clock reset
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

I1 (GND VDD net16 net20 Q) nand2
I0 (GND VDD net13 net16 net15) nand2
I5 (GND VDD Q net10 reset net20) nand3
I4 (GND VDD net10 D reset net13) nand3
I3 (GND VDD net16 clock net13 net10) nand3
I2 (GND VDD net15 clock reset net16) nand3
ends dff
// End of subcircuit definition.

// Library name: PLL
// Cell name: inv
// View name: schematic
subckt inv GND VDD a z
PM0 (z a VDD VDD) pch w=(135n) l=129n as=80.595f ad=44.145f ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=485.097n sb=485.097n m=(1)*(2)
NM0 (z a GND GND) nch w=(135n) l=129n as=80.595f ad=80.595f ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n m=(1)*(1)
ends inv
// End of subcircuit definition.

// Library name: PLL
// Cell name: pfd
// View name: schematic
subckt pfd GND VDD dclk down rclk up
I5 (VDD GND down VDD dclk net010) dff
I4 (VDD GND up VDD rclk net010) dff
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

I9 (GND VDD up down net11) nand2
I23 (GND VDD net016 net010) inv
I22 (GND VDD net017 net016) inv
I21 (GND VDD net020 net017) inv
I20 (GND VDD net021 net020) inv
I18 (GND VDD net11 net018) inv
I19 (GND VDD net018 net021) inv
ends pfd
// End of subcircuit definition.

// Library name: PLL
// Cell name: dff tg
// View name: schematic

subckt dff tg D GND Q Qb VDD clk
NM3 (Qb clkb net16 GND) nch w=(135n) l=129n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)
NM1 (net12 clk net10 GND) nch w=(135n) l=129n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)
NM2 (net13 clk net16 GND) nch w=(135n) l=129n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)
NM0 (D clkb net10 GND) nch w=(135n) l=129n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

I4 (GND VDD net13 net12) inv
I13 (GND VDD Q Qb) inv
I2 (GND VDD clk clkb) inv
I9 (GND VDD net16 Q) inv
I3 (GND VDD net10 net13) inv

PM3 (net16 clk Qb VDD) pch w=(135n) l=129n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

PM1 (net10 clkb net12 VDD) pch w=(135n) l=129n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

PM2 (net16 clkb net13 VDD) pch w=(135n) l=129n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

PM0 (net10 clk D VDD) pch w=(135n) l=129n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n
m=(1)*(1)

ends dff tg

// End of subcircuit definition.

// Library name: PLL
// Cell name: divider8
// View name: schematic
subckt divider8 GND VDD clkin clkout
I18 (net021 GND f16 net021 VDD net023) dff tg
I19 (net018 GND f32 net018 VDD net021) dff tg
I20 (net028 GND clkout net028 VDD net018) dff tg
I14 (net5 GND f2 net5 VDD clkin) dff tg
I15 (net014 GND f4 net014 VDD net5) dff tg
I16 (net023 GND f8 net023 VDD net014) dff tg
I17 (GND VDD net024 net016) inv
ends divider8
// End of subcircuit definition.

// Library name: PLL
// Cell name: vco inv1v
// View name: schematic
subckt vco inv1v GND VDD in out vn vp
NM2 (net40 vn GND GND) nch w=(1.638u) l=246n as=314.496f ad=314.496f
ps=2.3496u pd=2.3496u nrd=117.216m nrs=117.216m sa=922.985n
sb=922.985n m=(25)*(5)
NM1 (out in net40 GND) nch w=(257.4n) l=246n as=58.4118f ad=58.4118f
ps=762n pd=762n nrd=881.624m nrs=881.624m sa=999.937n sb=999.937n
m=(7)*(5)
PM2 (net41 vp VDD VDD) pch w=(1.17u) l=246n as=224.64f ad=193.05f
ps=1.788u pd=1.5u nrd=141.026m nrs=164.103m sa=1.56819u
sb=1.56819u m=(25)*(10)
PM1 (out in net41 VDD) pch w=(172.8n) l=246n as=53.5896f ad=46.2996f
ps=762n pd=654n nrd=1.55056 nrs=1.7947 sa=1.69745u sb=1.69745u
m=(7)*(10)
ends vco inv1v
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

// End of subcircuit definition.

// Library name: PLL
// Cell name: vco
// View name: schematic

```
subckt vco GND VDD Vcont dclk
PM12 (dclk v VDD VDD) pch w=(135n) l=246n as=45.603f ad=45.603f
ps=675.6n pd=675.6n nrd=2.50222 nrs=2.50222 sa=3.50342u
sb=3.50342u m=(1)*(25)
PM11 (vn vp VDD VDD) pch w=(225n) l=246n as=56.565f ad=56.565f ps=762n
pd=762n nrd=1.11733 nrs=1.11733 sa=999.937n sb=999.937n m=(1)*(5)
PM0 (vp vp VDD VDD) pch w=(225n) l=246n as=85.725f ad=85.725f
ps=1.194u pd=1.194u nrd=1.69333 nrs=1.69333 sa=327n sb=327n
m=(1)*(1)
NM11 (vn vn GND GND) nch w=(225n) l=246n as=85.725f ad=85.725f
ps=1.194u pd=1.194u nrd=1.69333 nrs=1.69333 sa=327n sb=327n
m=(1)*(1)
NM12 (dclk v GND GND) nch w=(135n) l=129n as=51.435f ad=51.435f
ps=762n pd=762n nrd=2.82222 nrs=2.82222 sa=891.417n sb=891.417n
m=(1)*(5)
NM0 (vp Vcont net019 GND) nch w=(2.025u) l=246n as=347.794f
ad=334.125f ps=2.46975u pd=2.355u nrd=81.4815m nrs=84.8148m
sa=4.73704u sb=4.73704u m=(1)*(40)
I35 (GND VDD v net023 vn vp) vco inv1v
I36 (GND VDD net023 net025 vn vp) vco inv1v
I37 (GND VDD net025 v vn vp) vco inv1v
```
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

R0 (net019 GND) resistor r=400
ends vco
// End of subcircuit definition.

// Library name: LDO
// Cell name: ripple cancellation
// View name: schematic
V24 (net0125 0) vsource dc=500.0m type=dc
PM18 (Vout net0103 net106 net106) pch w=(9u) l=9.012u as=1.5336p ad=1.485p
ps=9.7008u pd=9.33u
   nrd=18.3333m nrs=18.9333m sa=76.0381u sb=76.0381u m=(50)*(50)
PM20 (net0103 net0140 net106 net106) pch w=(135n) l=246n as=45.603f ad=45.603f
ps=675.6n pd=675.6n
   nrd=2.50222 nrs=2.50222 sa=3.50342u sb=3.50342u m=(1)*(25)
PM4 (net038 net086 Vout Vout) pch w=(135n) l=246n as=62.37f ad=44.145f ps=924n
pd=654n nrd=2.42222
   nrs=3.42222 sa=847.025n sb=847.025n m=(1)*(4)
PM3 (net086 clkout Vout Vout) pch w=(135n) l=246n as=62.37f ad=44.145f ps=924n
pd=654n nrd=2.42222
   nrs=3.42222 sa=847.025n sb=847.025n m=(1)*(4)
PM6 (net025 refclk Vout Vout) pch w=(135n) l=246n as=62.37f ad=44.145f ps=924n
pd=654n nrd=2.42222
   nrs=3.42222 sa=847.025n sb=847.025n m=(1)*(4)
PM7 (net027 net025 Vout Vout) pch w=(135n) l=246n as=62.37f ad=44.145f ps=924n
pd=654n nrd=2.42222
   nrs=3.42222 sa=847.025n sb=847.025n m=(1)*(4)
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

PM9 (net83 VG vdd! vdd!) pch w=(9u) l=9.012u as=1.5336p ad=1.485p ps=9.7008u
pd=9.33u nrd=18.3333m
nrs=18.9333m sa=76.0381u sb=76.0381u m=(50)*(50)
I89 (0 Vout net037 Vcont Filtered Vcont Filtered) ErrorAmplifier Test
I86 (0 net106 net0102 net0124 net0125) ErrorAmplifier Test
I72 (0 vdd! net0101 Vout amp LDO ref) ErrorAmplifier Test
C7 (net035 Vcont Filtered) capacitor c=22.48p
C6 (net037 0) capacitor c=11.24p
C11 (net093 0) capacitor c=50p
C4 (net83 0) capacitor c=cout
C9 (Vout 0) capacitor c=cout
V11 (net106 0) vsource dc=1 mag=1 type=sine ampl=50m freq=100K
I74 (0 vdd! Vout amp VG) buffer OpAmp
I69 (0 vdd! LDO ref) BGR
R10 (net035 net037) resistor r=100K
R14 (net0102 0) resistor r=5K
R7 (net0101 0) resistor r=5K
R8 (net83 net0101) resistor r=3K
R15 (Vout net0102) resistor r=3K
R9 (net093 net035) resistor r=100K
V2 (refclk 0) vsource type=pulse val0=0 val1=1 period=64/1.5G width=64/3G
I41 (0 Vout dclk down net027 up) pfd
NM9 (net0103 net0103 0 0) nch w=((150n) * 0.9) / (1)) l=246n as=80.595f ad=80.595f
ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n m=(2)*(1)
NM10 (net0140 net0124 0 0) nch w=(135n) l=246n as=80.595f ad=44.145f ps=1.194u
pd=654n nrd=2.42222 nrs=4.42222 sa=515.386n sb=515.386n m=(2)*(2)
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

NM11 (net106 net106 net0140 net106) nch w=(135n) l=246n as=80.595f ad=80.595f ps=1.194u pd=1.194u nrd=4.42222 nrs=4.42222 sa=327n sb=327n m=(1)*(1)

NM4 (net038 net086 0 0) nch w=(135n) l=246n as=80.595f ad=44.145f ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=515.386n sb=515.386n m=(1)*(2)

NM3 (net086 clkout 0 0) nch w=(135n) l=246n as=80.595f ad=44.145f ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=515.386n sb=515.386n m=(1)*(2)

NM1 (net025 refclk 0 0) nch w=(135n) l=246n as=80.595f ad=44.145f ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=515.386n sb=515.386n m=(1)*(2)

NM12 (net095 net095 0 0) nch w=(299.7n) l=246n as=62.937f ad=49.4505f ps=819.6n pd=629.7n nrd=550.551m nrs=700.701m sa=1.05918u sb=1.05918u m=(1)*(6)

NM7 (net096 up net093 0) nch w=(299.7n) l=246n as=62.937f ad=49.4505f ps=819.6n pd=629.7n nrd=550.551m nrs=700.701m sa=1.05918u sb=1.05918u m=(1)*(6)

NM6 (net027 net025 0 0) nch w=(135n) l=246n as=80.595f ad=44.145f ps=1.194u pd=654n nrd=2.42222 nrs=4.42222 sa=515.386n sb=515.386n m=(1)*(2)

NM0 (net093 down net095 0) nch w=(299.7n) l=246n as=62.937f ad=49.4505f ps=819.6n pd=629.7n nrd=550.551m nrs=700.701m sa=1.05918u sb=1.05918u m=(1)*(6)

NM8 (V out V out net096 0) nch w=(299.7n) l=246n as=62.937f ad=49.4505f ps=819.6n pd=629.7n nrd=550.551m nrs=700.701m sa=1.05918u sb=1.05918u m=(1)*(6)

I93 (net081 net078 net080 net079) inv

I40 (0 Vout dcl k divider8

I79 (0 Vout Vcont Filtered clkout) vco

ic I79.v=0 simulatorOptions options retol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27.0 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output"

checklimitdest=psf

tran tran stop=5u errpreset=conservative write="spectre.ic"
APPENDIX A. SPICE NETLIST FOR A LOW JITTER PLL USING ACTIVE LOOP FILTER AND LOW DROPOUT REGULATOR

writefinal="spectre.fc" annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000 annotate=status
dcOpInfo info what=oppoint where=rawfile
ac ac start=1 stop=10G annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=all currents=all