CMOS Low Power Digital and Analog Subthreshold

Temperature Sensor Design

A Thesis Presented

by

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to

The Department of Electrical and Computer Engineering

in partial fulfillment of the requirements

for the degree of

Master of Science

in

Electrical and Computer Engineering

Northeastern University

Boston, Massachusetts

August 2018
To my family.
Contents

List of Figures iv
List of Tables vi
List of Acronyms vii
Acknowledgments viii
Abstract of the Thesis ix

1 Introduction 1
   1.1 Motivation ................................................. 1
   1.2 Organization of Thesis .................................... 4

2 Basic Theory and Prior Arts 5
   2.1 Analog Temperature Sensor .................................. 5
      2.1.1 ADC .................................................... 10
         2.1.1.1 Flash ADC ......................................... 10
         2.1.1.2 Pipeline ADC ..................................... 11
         2.1.1.3 Integrating ADC .................................. 12
         2.1.1.4 Successive Approximation Register (SAR) ADC .... 13
   2.2 Digital Temperature Sensor ................................ 14
      2.2.1 TDC ..................................................... 15
         2.2.1.1 Delay Line TDC .................................... 15
         2.2.1.2 Vernier Delay Line TDC ......................... 16
         2.2.1.3 Cyclic Pulse-Shrinking TDC .................... 17

3 Proposed Digital Temperature Sensor 18
   3.1 Temperature Dependent Delay Cell ......................... 26
      3.1.1 Inverter-Based Buffer .................................. 26
      3.1.2 Interlaced Hysteresis Delay Cell (IHDC) .......... 28
3.1.3 Inverter Interlaced Cascaded Delay Cell (IICDC) .......................... 30
3.1.4 Comparison of delay cells .................................................... 32
3.2 Temperature-to-Pulse Generator ............................................... 35
3.3 Proposed Digital Temperature Sensor Operation ..................... 41

4 Proposed Analog Temperature Sensor ....................................... 43
  4.1 Body Connection ................................................................. 48
  4.2 Proposed Analog Temperature Sensor Operation .................. 51

5 Simulation Results .................................................................. 54
  5.1 Proposed Temperature Sensor .............................................. 54
  5.1.1 Temperature-to-Pulse Generator ......................................... 54
  5.2 Proposed Analog Temperature Sensor ................................. 60

6 Conclusion ............................................................................ 65

Bibliography ............................................................................ 67

A Netlist for A Digital Temperature Sensor ................................ 75

B Netlist for An Analog Temperature Sensor ............................ 91
**List of Figures**

1.1 Traditional temperature sensor design with BJTs ........................................... 3
2.1 npn transistor in CMOS technology ................................................................. 6
2.2 Bandgap Temperature sensor ........................................................................... 6
2.3 Relationship between temperature and voltages in the sensor ......................... 7
2.4 Traditional three-transistor temperature sensor ............................................... 8
2.5 Flash ADC ......................................................................................................... 10
2.6 Pipeline ADC .................................................................................................... 11
2.7 Dual-slope ADC ................................................................................................ 12
2.8 SAR ADC .......................................................................................................... 13
2.9 Temperature sensor with delay line block diagram ........................................... 14
2.10 Delay line TDC .................................................................................................. 15
2.11 Vernier delay line TDC ..................................................................................... 16
2.12 Cyclic pulse-shrinking TDC .............................................................................. 17
3.1 The delay-line based temperature sensor block diagram ................................... 19
3.2 Offset reduction .................................................................................................. 19
3.3 Temperature insensitive delay cell ..................................................................... 21
3.4 Proposed digital temperature diagram ................................................................ 23
3.5 D flip-flop ........................................................................................................... 23
3.6 T flip-flop ............................................................................................................ 24
3.7 Without using extended input signal ................................................................... 25
3.8 Target pulse selection ......................................................................................... 26
3.9 Inverter-based buffer ......................................................................................... 27
3.10 Interlaced hysteretic delay cell (IHDC) ............................................................... 28
3.11 Timing diagram of IHDC .................................................................................. 29
3.12 Inverter interlaced cascaded delay cell (IICDC) .................................................. 31
3.13 Timing diagram of IICDC ................................................................................ 32
3.14 Short-circuit path timing graph in IHDC ............................................................ 33
3.15 Short-circuit path in IHDC ................................................................................ 34
3.16 Proposed temperature-to-pulse generator block diagram .......................................................... 36
3.17 Proposed modified IICDC .......................................................................................................... 37
3.18 D flip-flop based 9 bit counter ................................................................................................. 38
3.19 D flip-flop with reset .............................................................................................................. 38
3.20 SR latch .................................................................................................................................. 39
3.21 Counter output timing diagram ............................................................................................... 40
3.22 Proposed digital temperature sensor ..................................................................................... 41
3.23 Proposed digital temperature sensor timing diagram ............................................................... 42

4.1 Subthreshold temperature sensor front-end ............................................................................ 44
4.2 Subthreshold temperature sensor front-end operation ............................................................. 45
4.3 Proposed subthreshold temperature sensor ........................................................................... 46
4.4 Summing amplifier .................................................................................................................... 47
4.5 Different body connections ..................................................................................................... 50
4.6 Proposed subthreshold temperature sensor ........................................................................... 51
4.7 Proposed subthreshold temperature sensor timing diagram ................................................... 53

5.1 Fast - Fast corner ...................................................................................................................... 56
5.2 Typical - Typical corner ........................................................................................................... 57
5.3 Slow - Slow corner ................................................................................................................... 58
5.4 Digital output code ................................................................................................................. 59
5.5 Fast - Fast corner ...................................................................................................................... 61
5.6 Typical - Typical corner ........................................................................................................... 62
5.7 Slow - Slow corner ................................................................................................................... 63
List of Tables

3.1 Delay cell comparisons .................................................. 34
3.2 Comparisons of IICDC and modified IICDC .......................... 37

4.1 Temperature sensor without summing amplifier ....................... 49
4.2 Proposed temperature sensor ............................................. 49

5.1 Comparison of the digital temperature sensors ....................... 60
5.2 Comparison of the analog temperature sensors ...................... 64
List of Acronyms

ADC  Analog-to-Digital Converter.
BJT  Bipolar Junction Transistor.
CMOS Complementary Metal-Oxide-Transistor.
CTAT Complementary To Absolute Temperature.
DTM  Dynamic Thermal Management.
IHDC Interlaced Hysteresis Delay Cell.
IICDC Inverter Interlaced Cascaded Delay Cell.
MOSFET Metal-Oxide-Transistor Feild-Effect Transistor.
nMOS n-channel Metal-Oxide-Transistor.
pMOS p-channel Metal-Oxide-Transistor.
PTAT Proportional To Absolute Temperature.
SAR Successive Approximation Register.
TDC Time-to-Digital Converter.
VLSI Very Large Scale Integration.
Acknowledgments

This thesis could have written with Dr. Kim who served as my advisor. He encouraged and challenged me throughout my academic program. I learned a great deal about engineering and creative brainstorming from him. I would also like to thank the support of my family and friends.
Sensing temperature for localizing hot spots provides additional observability in modern integrated circuits. First, a digital temperature sensor with modified inverter interlaced cascaded delay cells (IICDCs) is presented. Temperature is sensed by using a temperature-to-pulse generator that produces pulse with an XOR gate and a temperature dependent delay line with the modified IICDCs. A D flip-flop based T flip-flop is implemented to produce a pulse, which is used as the input signal of the delay line, and the inverted input signal is employed to reduce the offset of temperature sensor. The output of the temperature-to-pulse generator is applied to a time-to-digital converter (TDC) to achieve digital codes of the sensed temperature. By using the modified IICDCs, it is possible to consume lower power than the conventional approach using the inverter-based delay lines. The digital temperature sensor is designed with 180 nm CMOS technology and 1.8 V supply voltage. This digital temperature sensor circuit consumes 324 \( \mu \)W at 27\( ^\circ \)C. The temperature sensor monitors
-20°C to 110 °C with a good linearity. Second, an analog subthreshold voltage temperature sensor is presented. In the previous subthreshold voltage temperature sensor topology, a PMOS transistor array is employed to monitor temperature variation. Once the temperature sensor is completely pre-charged, the PMOS transistor array begins discharging. When the PMOS array enters weak inversion, the sampling point is decided. The existing low power subthreshold voltage temperature sensor requires complicated weak inversion current equation to choose the optimal sampling time. To reach the optimal sampling time, it takes approximately 10 µs to 100 µs. In the proposed analog subthreshold temperature sensor, PMOS transistor is employed to monitor temperature variation. When the PMOS enters weak inversion in discharging process, the PMOS stops discharging and the output node voltage becomes stable. It takes around 4 µs. To remove the exponential term in the weak inversion current equation, a summing amplifier is used, and the output node is connected to an analog-to-digital converter (ADC) to change the temperature information to the digital code. The supply voltage of the analog temperature sensor is 1.8V, and the 180 nm CMOS technology is used to design the analog temperature sensor. The total power consumption of the analog temperature sensor circuit is 2.5 mW at 27°C. The front-end of the temperature sensor consumes 11.19 µW. The analog temperature sensor can monitor from -20°C to 130°C shows a very good linearity.
Chapter 1

Introduction

1.1 Motivation

Today, people use computers, cell phones, and other electric devices which have integrated circuit chips. Most of them require thermal monitoring to prevent self-heating of the chip. If they have an inaccurate thermal monitoring system, their chips will be broken by overheating. Therefore, many researchers and companies have been researching temperature sensors.

On-chip temperature sensor design is extremely critical for dynamic thermal management (DTM) in VLSI circuits. On-chip temperature monitoring circuits prevent damage from excessive chip heating to avoid destroying the chip and reducing lifetime.

The temperature sensor needs to be smaller and consume less power. Since the area where on-chip heating is concerned, numerous temperature sensors are placed to monitor
temperature discreetly at the critical points. Therefore, these temperature monitoring circuits must consume small area and low power. As the distance from the temperature sensors to hot spots directly affects the performance of DTM, small and accurate temperature sensors are required [1, 2, 3]. There are lots of temperature sensor architectures which are accurate and consume small area [4, 5, 6, 7]. For instance, multi-core architecture is employed in the microprocessor in many companies because of its energy efficiency and better performance than single-core architecture. However, multi-core architecture has problems with large temperature gradients and hotspots. Hot spots are the main problem in multi-core architecture [8, 9, 10]. To monitor the numerous hot spots with low hardware overhead, sensor footprint needs to be extremely small [1, 2, 11, 12].

Temperature sensors generate output signal which contains temperature information such as a voltage, a current, or a pulse period. The output of the temperature sensors is aimed to achieve a linear relationship with the chip temperature. The temperature dependent principal of p-n junction is widely used for on-chip temperature sensors. Figure 1.1 is the traditional temperature sensor. The difference voltage between base-emitter voltages of two BJT is proportional to the absolute temperature if two different values of currents are applied to each BJT.

The voltage difference between two base-emitter voltages has linear relationship with the absolute temperature [13]. Since the BJT-based temperature sensor can achieve high accuracy, many temperature sensor products and research papers have been using this topology. However, the BJT-based temperature sensors require a large area and consume
CHAPTER 1. INTRODUCTION

Considerable power. Occupying a large area and having high power consumption are critical problems on designing on-chip temperature monitoring circuit. To solve the problems, there are several alternative topologies.

A digital temperature sensor can be a solution to reduce the power consumption. The digital temperature sensor is composed with a temperature-to-pulse generator and a time-to-digital converter (TDC). The temperature-to-pulse generator produces a pulse by using input signal and a delay line. The pulse width varies with temperature variation. The output of the temperature-to-pulse generator is converted to digital codes by the TDC. An analog temperature sensor using a pMOS array which operates in subthreshold voltage region is another way to monitor the temperature variation. The threshold voltage of the pMOS array is measured and converted by an analog-to-digital converter. Since only one pMOS
CHAPTER 1. INTRODUCTION

...transistor is employed to measure temperature, the analog temperature sensor can reduce occupying area and power consumption.

In this research, silicon area and power effective temperature designs are proposed in both digital and analog domain. This research aims a good linearity characteristics and resolution of temperature sensors as well as area and power overhead.

1.2 Organization of Thesis

In this thesis, followings will be described. In Chapter 2, the existing analog and digital temperature sensors are presented with an overview of analog-to-digital converters (ADCs) and time-to-digital converters (TDCs). In Chapter 3, the proposed digital temperature sensor is described. The comparison of temperature dependent delay cells is discussed. Chapter 4 addresses the proposed analog subthreshold voltage temperature sensor. In Chapter 5, the experiments with the proposed analog and digital temperature sensors are described along with simulation results and comparisons, followed by the conclusion in Chapter 6.
Chapter 2

Basic Theory and Prior Arts

2.1 Analog Temperature Sensor

The pn-junction based temperature sensor is commonly used in state-of-the-art microprocessors. The pnp transistors can be formed in standard CMOS technology. A $p^+$ region which is inside an n-well can be the emitter and the n-well can be the base. A p-substrate is able to be the collector and it is connected to the ground. Figure 2.1 shows the pn-junction transistor based temperature sensor.

The most widely used schematic is a bandgap temperature sensor. The bandgap temperature sensors generate a voltage proportional to absolute temperature (PTAT). Two diode-connected pnp transistors produce two different voltages which are $V_{BE}$ and $\Delta V_{BE}$ respectively. These two voltages are used to generate PTAT and a temperature-independent bandgap reference voltage. They are converted to a digital output by an analog-to-digital
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

Figure 2.1: pnp transistor in CMOS technology

The base-emitter voltage $V_{BE}$ of pnp transistor and the difference of base-emitter voltages of two pnp transistors can be written as:
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

\[ V_{\text{Ref}} = V_{BE} + n \cdot \Delta V_{BE} \]

Figure 2.3: Relationship between temperature and voltages in the sensor

\[ V_{BE} = V_T \ln \left( \frac{I}{I_S} \right) \]  \hspace{1cm} (2.1)

\[ \Delta V_{BE} = V_T \ln(\alpha) \] \hspace{1cm} (2.2)

\[ V_T = \frac{kT}{q} \] \hspace{1cm} (2.3)

where \( k \) is Boltzmann’s constant, \( q \) is the electron charge, \( T \) is the absolute temperature, \( I_S \) is saturation current of the transistor, and \( \alpha \) is the ratio of two currents. At room temperature, \( V_T \approx 26mV \).

The bandgap temperature sensor is possible to generate reference voltage of the ADC. The reference voltage is produced by adding PTAT voltage and complementary to absolute temperature (CTAT). \( V_{BE} \) is CTAT voltage and \( \Delta V_{BE} \) is PTAT voltage. \( \Delta V_{BE} \) is amplified by an amplifier to produce the reference voltage [14].
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

In case of the pn-junction transistor based temperature sensor, using bipolar transistors is the critical drawback of area and power consumption. As an alternative method to monitor temperature in analog circuit design, MOSFET-only circuit design can be a good solution [15, 16, 17].

![Diagram of a traditional three-transistor temperature sensor](image)

**Figure 2.4:** Traditional three-transistor temperature sensor

Recently, researches of temperature sensors which are using threshold voltage have progressed [18, 19]. The threshold voltage-based temperature sensors are linear and monitor wide range of temperature. Although, temperature sensors with pn junctions have high linearity, the threshold voltage-based temperature sensors significantly occupy smaller area and consume lower power than the pn-junction-based temperature sensors. A traditional way to design threshold voltage-based temperature sensor is using three transistors which
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

is shown in Figure [2.4][18]. The conventional three transistors temperature sensor uses the temperature dependence of important parameters of the MOS transistor.

\[ \frac{\Delta V_T}{\Delta T} \approx -1.8mV/K \quad (2.4) \]

\[ \frac{1}{\beta} \cdot \frac{\beta}{\Delta T} \approx -0.5%/K \quad (2.5) \]

The pMOS transistors M4, M5, M6, and M7 are employed as current mirror. The current which is flows transistor M1 is mirrored to transistors M2 and M3. The output voltages of the node A and B are

\[ V_A = V_T \times (1 + \frac{X_{45}}{X_{45} - X_{13} - X_{12}}) \quad (2.6) \]

\[ V_B = V_T \times (1 + \frac{X_{13}}{X_{45} - X_{13} - X_{12}}) \quad (2.7) \]

\[ X_{pq} = \sqrt{\frac{W_p/L_p}{W_q/L_q}} \quad (2.8) \]

\( X_{pq} \) is the ratio between the width and length sizes of the transistor pair p and q.

The voltage \( V_A \) at the node A controls the gate of the transistor M9, and the voltage \( V_B \) at the node B controls the gate of the transistor M8. The output current can be written as

\[ I_{OUT} = \beta_8 \times V_T \times \left( \frac{X_{13}}{X_{45} - X_{13} - X_{12}} \right)^2 \quad (2.9) \]

\[ = const \times \beta \times V_T \quad (2.10) \]
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

The temperature dependence of the output current can be written as

\[
\frac{\Delta I_{OUT}}{I_{OUT}} = \left( \frac{1}{\beta} \cdot \frac{d\beta}{dT} + \frac{2}{V_T} \cdot \frac{dV_T}{dT} \right) \times \Delta T
\]  

2.1.1 ADC

2.1.1.1 Flash ADC

A flash ADC is shown in Figure 2.5.

Figure 2.5: Flash ADC
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

The flash ADC which is known as parallel ADC has an advantage of high speed operation. The flash ADC only needs one clock cycle to convert to digital codes. It consists of a resistor string, comparators, and a digital encoder. The $2^N$ resistors which are employed to compose the resistor string produce reference voltages. Each reference voltage is applied to $2^N - 1$ comparators. To achieve one more output bit, the flash ADC requires an additional comparator. The increased number of transistors has disadvantage of the area and power consumption.

2.1.1.2 Pipeline ADC

A pipeline ADC which is shown in Figure 2.6 is a converter with multiple series-connected stages. Each stage consists of a ADC, a sample-and-hold, a digital-to-analog converter (DAC), a summer, and a residue amplifier. The pipeline ADC can achieve the

![Pipeline ADC Diagram]

Figure 2.6: Pipeline ADC

...
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

output from 10 to 13 bits with high speed operation. The advantage of the pipeline ADC is its high throughput with fast conversion and the disadvantage is the initial N clock cycle delay until the first digital output appears [13].

2.1.1.3 Integrating ADC

Single-slope and dual slope ADCs are an integrating ADC. In the single-slope ADC, an input signal is sampled until the value of the input voltage is equal to that of a reference voltage. In case of the dual-slope ADC which is shown in Figure 2.7, an input voltage is applied to the ADC and increased for a specific period. After the period, a reference voltage is applied and the increased voltage is back to zero. The dual-slope ADC cancels irregularities which can affect the accuracy from the single-slope ADC.

![Diagram of Dual-slope ADC](image)

Figure 2.7: Dual-slope ADC
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

2.1.1.4 Successive Approximation Register (SAR) ADC

A SAR ADC which is shown in Figure 2.8 can be used to achieve high resolution from 12 to 18 bits. Because of the SAR ADC has simple architecture, it can operate at high speed with small area and low power. The SAR ADC consists of a DAC, a SAR, and a comparator.

Figure 2.8: SAR ADC

An input voltage is compared with the output of the DAC. A reference voltage is divided half to determine whether the input voltage is bigger or smaller than the half value of the reference voltage. The comparison continues until the divided reference voltage is same to the input voltage. The output of the SAR controls the digital output conversion.
2.2 Digital Temperature Sensor

Temperature sensors with delay lines measure delay which is affected by temperature. The delay changes when temperature changes. The main element of the temperature sensor is a temperature-to-pulse generator which generates temperature dependent pulse as the temperature sensing part. The temperature-to-pulse generator should be designed to produce output pulse which is linearly proportional to temperature. In the temperature sensing part, there is a delay line which is comprised of an even number of inverter-based buffers.

Figure 2.9: Temperature sensor with delay line block diagram

An input signal is delayed by the delay line. To produce the temperature dependent output pulse, an XOR gate is used. The output signal of the delay line which delays the
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

input signal and the input signal produce output pulse at rising edges of the clock pulse. The block diagram of the temperature-to-pulse generator is shown in Figure 2.9. The produced output pulse goes into the time-to-digital converter (TDC). The produced pulse which varies on temperature is converted to digital code by TDC.

2.2.1 TDC

2.2.1.1 Delay Line TDC

A delay line TDC which is shown in Figure 2.10 is the simple converter. The time difference is measured by using a series of D flip-flops, a start pulse and, a clock as a stop pulse. The start pulse is fed to a delay line.

![Delay line TDC](image)

Figure 2.10: Delay line TDC
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

The outputs of the delay cells are the input of the D flip-flops. At the rising edge of the stop pulse, the value of the delay line is maintained. The output thermometer code is determined by the distance of the start and stop pulse. The resolution of the delay line TDC is limited by the buffer delay.

2.2.1.2 Vernier Delay Line TDC

The resolution of the Vernier delay line TDC is limited to a gate delay. In this topology shown in Figure 2.11, there are two different delay lines.

![Vernier Delay Line TDC Diagram](image)

Figure 2.11: Vernier delay line TDC

The way to produce the thermometer code is similar to the delay line TDC. The critical point of the vernier delay TDC is the thermometer code. The thermometer code is determined by two different delay lines which have different amount of delay. The upper delay cell chain
CHAPTER 2. BASIC THEORY AND PRIOR ARTS

has greater delay than the lower delay cell chain. The resolution is the distance between two pulses which are fed to the two delay cell chains. The vernier delay line TDC can achieve the higher resolution than the resolution of the delay line TDC.

2.2.1.3 Cyclic Pulse-Shrinking TDC

The cyclic pulse-shrinking TDC [20] is shown in Figure 2.12.

![Cyclic Pulse-Shrinking TDC Diagram](image)

Figure 2.12: Cyclic pulse-shrinking TDC

The cyclic pulse-shrinking TDC has a delay line which consists of even number of inverter-based buffer. The input pulse goes into the delay line and the input signal is shrunk until it disappears completely. A counter is employed to count the circulation times of the input pulse. In the delay line, all buffers have the same dimension. However, the \( n \)th inverter cell has a larger width than other inverter-based buffers. When the input pulse passes the \( n \)th inverter cell, the pulse shrinking occurs.
Chapter 3

Proposed Digital Temperature Sensor

While the VLSI chips have been changing larger and complicated, the on-chip temperature sensor has become the important component in modern IC designs. In case of a digital temperature sensor design, a delay-line based temperature sensor is proposed [20].

In the proposed digital temperature sensor, new delay cells are used in the delay line. The delay-line based temperature sensor is comprised of a thermal sensing part and the TDC. The thermal sensing part produces a temperature dependent pulse. The pulse width is extended when the temperature increases. The TDC converts the temperature dependent pulse to a digital code. In the thermal sensing part of the prior temperature sensor, there are two different types of delay lines which are a temperature dependent delay line and a temperature insensitive delay line. The temperature dependent delay is made with CMOS logic inverter-based buffer. The block diagram of the delay-line based temperature sensor is shown in Figure 3.1.
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

Temperature dependent delay

\[ W = t_1 - t_2 \]

Temperature insensitive delay

Figure 3.1: The delay-line based temperature sensor block diagram

Figure 3.2: Offset reduction
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

Using the one temperature dependent delay line to generate the temperature dependent pulse, the produced pulse width is wide as much as the delay of the temperature dependent delay line. As the delay has a large offset [20], it is required long time to convert to digital code and more output bits. Therefore, the temperature sensor with the large offset in the temperature-to-pulse generate consumes more power than the temperature sensor with a low offset. To reduce the offset, the temperature insensitive delay line with thermal compensation for temperature sensitivity is employed. Figure 3.2 shows that using two different delay lines can reduce the offset.

The carrier mobility and the threshold voltage of the CMOS transistors are affected when the temperature changes. The carrier mobility decreases when the temperature increases [21]. The equation is written as

\[ \mu = \mu_0 \left( \frac{T}{T_0} \right)^{km} \]  

(3.1)

Where \( km \) is in the range of -1.2 to -2.0, \( T_0 \) is the reference temperature, and \( T \) is the practical absolute temperature. The threshold voltage also decreased when the temperature increases [21].

\[ V_T(T) = V_T(T_0) + \alpha(T - T_0) \]  

(3.2)

Where \( \alpha \) is in the range of -0.5 \( mV/\degree K \) to 3.0 \( mV/\degree K \).

The temperature insensitive delay cell is shown in Figure 3.3 [20]. The diode-connected
transistor M2 is the load of the two diode-connected transistors M1 and M2. The three diode-connected transistors are the main elements of the temperature compensation circuit. Since the three transistors are diode-connected, $|V_{GD,M1}| = |V_{GD,M2}| = V_{GD,M3} = 0 < |V_T|$. Therefore, the three diode-connected transistors work in the saturation region. The bias current of M2 is following.

$$I_{D,M2} = \frac{\mu_0 C_{OX}}{2} \left( \frac{W}{L} \right) (V_{GS,M2} - V_T)^2 (1 + \lambda V_{GS,M2})$$ (3.3)

By substituting the threshold voltage equation, the equation can be written as

$$I_{D,M2} = \frac{\mu_0 C_{OX}}{2} \left( \frac{W}{L} \right) \left( \frac{T}{T_0} \right)^{Km}[V_{GS,M2} - V_T(T_0) - \alpha(T - T_0)]^2 (1 + \lambda V_{GS,M2})$$ (3.4)
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

Since the transistor M2 is diode-connected, \( V_{DS} \) is equal to \( V_{GS} \). To get the minimum thermal sensitivity, let \( \frac{\partial I_{D,M2}}{\partial T} = 0 \) \[20\]. The equation is following.

\[
\frac{\mu_0 C_{OX} k_m}{2T_0} \left( \frac{W}{L} \right) \left( \frac{T}{T_0} \right)^{k_m - 1} [V_{GS,M2} - V_T(T_0) - \alpha(T - T_0)]^2 (1 + \lambda V_{GS,M2})
\]

As a result, it is possible to get the simplified equation.

\[
V_{GS,M2} = V_T(T_0) + \alpha(T - T_0) + 2 \frac{\alpha T}{k_m}
\]

By substituting the \( V_{GS,M2} \) equation to the bias current equation, the equation can be written as

\[
I_{D,M2} = \frac{\mu_0 C_{OX}}{2} \left( \frac{W}{L} \right) \left( \frac{T}{T_0} \right)^{k_m} \left( \frac{2 \alpha T}{k_m} \right)^2 (1 + \lambda V_{GS,M2})
\]

When \( k_m = -2 \), the bias current becomes temperature insensitive.

\[
I_{D,M2} = \frac{\mu_0 C_{OX}}{2} \left( \frac{W}{L} \right) (\alpha T_0)^2 (1 + \lambda V_{GS,M2})
\]

In the proposed temperature-to-pulse generator which is the main part of the proposed digital temperature sensor, the input pulse signal is employed instead of using the temperature insensitive delay cells. In case of the temperature insensitive delay cell, big transistors are required in the current mirror to compensate temperature sensitivity. To resolve the problem,
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

the input signal which is not affected by temperature variation can be applied. The proposed
digital temperature sensor block diagram is shown in Figure 3.4.

![Figure 3.4: Proposed digital temperature diagram](image)

At the beginning, the input signal is divided by a T flip-flop. The T flip-flop is comprised
of a conventional D flip-flop which is shown in Figure 3.5.

![Figure 3.5: D flip-flop](image)

It consists of \( \overline{S}R \) NAND latches. \( \overline{S} \) and \( \overline{R} \) are complementary of set and reset, respec-
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

tively. When the $S$ is low and $R$ is high, the output $Q$ is high. When the $S$ is high and $R$ is low, the output $Q$ is low. When both $S$ and $R$ are high, the output is not changed and follows the previous value. In case of the D flip-flop, the output value is same as the input value at rising edge. At non-rising edge, the output value is same to the previous value.

![Figure 3.6: T flip-flop](image)

When the input node of the D flip-flop is connected to the complementary of the output, it works as the T flip-flop. In the proposed temperature-to-pulse generator, a D flip-flop based T flip-flop is employed. Figure 3.6 shows the timing diagram of the D flip-flop based T flip-flop. The input signal is divided by two. When a 500 kHz pulse signal is applied to the proposed temperature dependent delay line as the input signal, the output pulse signal of the XOR gate has an undesired pulse range. Since the rising edge and falling edge delay are different amounts, the rising edge and falling edge pulse range fall within the same 500 kHz pulse width. In the fast-fast corner temperature-to-pulse generator’s temperature monitoring
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

range, the XOR gate produces the pulse range of the falling edge as well. To remove the pulse range of the falling edge, a 250 kHz pulse is applied to the temperature dependent delay line and the 500 kHz pulse picks the target pulse range. The undesired pulse signal without using the extended input signal in the fast-fast corner is shown in Figure 3.7.

Therefore, the D flip-flop based T flip-flop is implemented to generate the 250 kHz pulse signal as the input signal of the temperature dependent delay line. The 250 kHz pulse is delayed by the temperature dependent delay line. Since the proposed digital temperature sensor only need the rising edge of the delay pulse signal, the XOR gate and an AND gate is employed. To choose the target pulse which is delayed from the rising edge of the input signal, the AND gate is required. The input signal passes the inverter and the inverted input signal picks the target pulse from the delayed signal with the AND gate. The target pulse selection is shown in Figure 3.8.
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

![Diagram of target pulse selection](image)

Figure 3.8: Target pulse selection

3.1 Temperature Dependent Delay Cell

3.1.1 Inverter-Based Buffer

The inverter-based buffer which is shown in Figure 3.9 is the simplest and basic buffer.

The low-to-high and high-to-low propagation delay of a CMOS logic inverter can be expressed as [22]

\[
\begin{align*}
    t_{PHL} &= \frac{2C_LV_{TN}}{k_N(V_{DD} - V_{TN})^2} + \frac{C_L}{k_N(V_{DD} - V_{TN})} \times \ln\left(\frac{1.5V_{DD} - 2V_{TN}}{0.5V_{DD}}\right) \\
    t_{PLH} &= \frac{-2C_LV_{TP}}{k_P(V_{DD} - V_{TP})^2} + \frac{C_L}{k_P(V_{DD} - V_{TP})} \times \ln\left(\frac{1.5V_{DD} - 2V_{TP}}{0.5V_{DD}}\right)
\end{align*}
\]

(3.10)  (3.11)
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

Figure 3.9: Inverter-based buffer

\[ k_N = \mu_N C_{OX} \left( \frac{W}{N} \right)_N \]  \hspace{1cm} (3.12)

\[ k_P = \mu_P C_{OX} \left( \frac{W}{N} \right)_P \]  \hspace{1cm} (3.13)

where \( k_N, k_P \) and \( C_L \) are the transconductance parameters and effective load capacitance of the CMOS logic inverter respectively. As a result, the propagation delay can be written as

\[ t_p = \frac{t_{PHL} + t_{PLH}}{2} \]  \hspace{1cm} (3.14)

\[ = \frac{C_L}{\mu C_{OX} \left( \frac{W}{L} \right)(V_{DD} - V_T)} \ln \left( \frac{1.5V_{DD} - 2V_T}{0.5V_{DD}} \right) \]  \hspace{1cm} (3.15)
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

3.1.2 Interlaced Hysteresis Delay Cell (IHDC)

To produce a large delay with low power, an interlaced hysteresis delay cell (IHDC) which is shown in Figure 3.10 is proposed in [23]. The IHDC consists of two cascaded cells.

![Figure 3.10: Interlaced hysteresis delay cell (IHDC)](image)

The nodes which are labeled with the same name are connected. The two series of transistors are main delay elements and M17 - M28 are used to charge or discharge each node. M17 - M28 do not affect the delay time. Those transistors (M17 - M28) help the floating nodes to reach a stable state.

In this structure, pMOS and nMOS are turned on and off simultaneously. Therefore, the significant short-circuit path does not exist. The power consumption is greatly increased.
Figure 3.11: Timing diagram of IHDC
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

by the short-circuit current. The power consumption of the IHDC is lower than that of the conventional inverter-based delay cells. When the IN signal goes low to high, pMOS M1 is turned off and nMOS M8 is turned on. The node M is pre-charged before the IN signal changes and the node A is low. Since M8 is turned on, the node H is discharged and M9 is turned on. Since the node F is charged, M7 and M17 are turned on. The node I and M are discharged, and M16 is turned off. Since the node A is already low, M2 is turned on and M22 is turned on. Therefore, the node I is low, and M10 and M28 are turned on. The node E is charged, and M6 and M18 are turned on. After the node J is discharged, M11 and M27 are turned on. The node D is charged, and M5 and M19 are turned on. Lastly, the node G is discharged, and M12 and M25 are turned on and the node C is charged. Therefore, the output changes low to high. In Figure 3.11, the operating timing diagram of the internal nodes of the IHDC is shown.

3.1.3 Inverter Interlaced Cascaded Delay Cell (IICDC)

An inverter interlaced cascaded delay cell (IICDC)\[24\] is shown in Figure 3.12. The IICDC has similar structure to the IHDC and produces a large delay with low power. The main delay elements which are the two series of cascade pMOS and nMOS transistors can achieve the delay. The nodes which are labeled with same name are connected. Unlike the IHDC, the connection nodes of the IICDC have clear status. In the IHDC, the extra transistors, which are not the main delay element, charge or discharge each node.
When the input signal goes from low to high, nMOS M8 is turned on and the node A is discharged. Since the node A is discharged, pMOS M9 is turned on and the node B is charged. The node B turns M7 on and the node C is discharged. Next, M10 is turned on and the node D is charged. The charged node D turns M6 on, and the node E is discharged and M11 is turned on. The node F is charged and M5 is tuned on. Lastly, the node G is discharged and M12 is turned on. Therefore, the output goes low to high. At the rising edge, the input signal affects M8, M9, M7, M10, M6, M11, M5, and M12. In other words, the rising edge of the input signal passes through M5, M6, M7, M8, M9, M10, M11 and M12 to the output node. Since the drain node of M1 is connected to the drain node of M8, the weakly driven status can be avoided [24]. In the IICDC, pMOS is turned on and nMOS is
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

turned off, or vice versa. Therefore, there is no short-circuit path from the power supply to the ground. As a result, the IICDC consumes lower power than other delay cells. Figure 3.13 shows the timing diagram of the IICDC.

3.1.4 Comparison of delay cells

In the IHDC, there is a short-circuit path from the power supply to the ground. Figure 3.14 shows that M15, M28 and M22 are turned on at the rising edge of the input signal for 623.89 ps simultaneously.
As shown in Figure 3.15, the current flows through M9, M23 and M16. When the input goes low to high, the node $H$ is discharged and M9 is turned on. Since M9 is turned on, the node $F$ is charged. The node $F$ turns M7 on and the node $I$ becomes discharged. At this point, M9 is still working. Next, the node $I$ turns M28 on. Before the input goes low to high, the node $M$ is pre-charged and M16 remains turned on. Since the node L is previously charged, M23 also remains turned on. Therefore, the current flows from the power supply to the ground for short time until the node $M$ is discharged below 50% of the power supply level. Although the short-circuit path from the power supply to the ground exists for a small amount of time, it can be a critical drawback for the low power circuit design. An alternative solution for the short-circuit path problem is using the IICDC.
In Table 3.1, three different delay cells are compared with 500 kHz input signal. The IHDC can produce the same amount of delay with lower power than the inverter-based buffer. The inverter-based buffer can delay the input signal 6.939 ns with 90 series buffer cells and consumes 15.925 µW. In case of the IHDC, it can make a 7.019 ns delay with 5 cells and consumes 14.799 µW. The IHDC delay cell chain is possible to make the similar delay to
the inverter-based buffer chain with lower power and less transistors. As aforementioned, the IHDC has the short-circuit current path from the power supply to the ground. By using the IICDC, the short-circuit path problem can be solved. The IICDC produces 6.99 ns delay with 8 delay cells and consumes 9.514 $\mu$W. The IICDC is a good solution for the low power delay cell.

3.2 Temperature-to-Pulse Generator

The temperature-to-pulse generator is the main part of the digital temperature sensor. In case of the conventional temperature-to-pulse generator, the temperature dependent delay line and the temperature insensitive delay line are employed. To reduce the offset, big size transistors are required for a current mirror which is the one part of the temperature insensitive cell. Instead of using the temperature insensitive cell, the input signal is used to reduce the offset. The proposed temperature-to-pulse generator is shown in Figure 3.16.

In the proposed temperature-to-pulse generator, the 500 kHz input signal is required. As aforementioned, the D flip-flop based T flip-flop generates the 250 kHz pulse signal with the input signal to avoid the undesired pulse range which is generated by the XOR gate with the fast-fast process corner falling edge of the temperature dependent delay line. The delayed input signal goes through the temperature dependent delay line. The output of the temperature dependent delay line and the inverted input signal enter the XOR gate to generate the pulse. Therefore, the pulse is produced after subtracting the offset. In the
temperature dependent delay line, the modified IICDC is employed. The IICDC is suitable for the low power digital temperature sensor. To extend the delay, the inverter-based buffers are added to each path between the first cascaded delay cell and the second cascaded delay cell. When the temperature increases, the modified IICDC can create more delay than the IICDC. The modified IICDC is shown in Figure 3.17.

When the input signal goes low to high, the source node of M1 goes low. In this case, the gate node of M9 turns on when the status of the source node of M1 passes through the inverter-based buffer. In the modified IICDC, each status of the source nodes of the first cascaded pMOS part is delayed to the status of the gate nodes of the second cascaded pMOS part. Similarly, each status of the source nodes of the second cascaded nMOS part is delayed to the status of the gate nodes of the first cascaded nMOS part. The IICDC and the modified
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

IICDC are compared in Table 3.2.

<table>
<thead>
<tr>
<th></th>
<th>Delay (ns)</th>
<th>Power (µW)</th>
<th>Delay Cell Number</th>
<th>Transistor Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>IICDC</td>
<td>6.99</td>
<td>9.514</td>
<td>8</td>
<td>128</td>
</tr>
<tr>
<td>Modified IICDC</td>
<td>6.987</td>
<td>7.576</td>
<td>1</td>
<td>40</td>
</tr>
</tbody>
</table>

In the temperature-to-pulse generator, the output pulse is generated with the modified IICDC chain and the inverted input signal. The produced output pulse is converted to the digital code by using the TDC which consists of asynchronous up counters. The reference clock signal is applied to the counter-based TDC. The counters which consists of the D flip-flops count a stream of reference pulse applied to the counters clock input. The output
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

is a binary value and the least significant bit can be determined by the number of pulses received at the clock input. The output pulse of the temperature-to-pulse generator is counted by the reference clock pulse and the first D flip-flop divides the reference pulse by two. Other D flip-flops divide previous pulses which is applied to the clock input of each D flip-flop. Figure 3.18 shows the 9 bit counter. The D flip-flop with reset is shown in Figure 3.19.

Figure 3.18: D flip-flop based 9 bit counter

Figure 3.19: D flip-flop with reset
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

To maintain the output value as high or low, SR latches which is shown in Figure 3.20 are used.

![SR latch diagram](image.png)

Figure 3.20: SR latch

The output pulse of the temperature-to-pulse generator is applied to the SR latches as the clock signal. If the SR latches are not used, each output pulse of the D flip-flops becomes low when the output pulse of the temperature-to-pulse generator goes low. In the SR latch, the output value is not changed when the clock of SR latch is low. The output value is same as the value of the S when the clock is high. The output nodes of the D flip-flops in the counter are connected to the nodes of each node of S. To avoid the case which the values of S and R are same, the inverter is placed between the nodes of S and R. When the clock is high, the output is not changed if both S and R are low and the output value is undefined if both S and R are high. Therefore, the output value can be monitored with binary digital codes by using SR latches. The output value is high when the reference pulse is high at the half value of the temperature-to-pulse generators output pulse. In opposite case, output value is low when the reference pulse is low at the half value of the temperature-to-pulse generators output pulse. Figure 3.21 shows the timing diagram of the counter with and without SR latches.
(a) With SR latches

(b) Without SR latches

Figure 3.21: Counter output timing diagram
CHAPTER 3. PROPOSED DIGITAL TEMPERATURE SENSOR

3.3 Proposed Digital Temperature Sensor Operation

The proposed digital temperature sensor is shown in Figure 3.22. The D flip-flop based T flip-flop produces the input signal of the temperature dependent delay line. The input signal is inverted and applied to the XOR gate. The delayed signal A and the inverted input signal B enter the XOR gate. The output signal of the XOR gate which is $P_{OUT}$ and the output signal of the T flip-flop which is $D_{OUT}$ are applied to the AND gate to eliminate redundant signal. The output signal of the AND gate is applied to the counter. The $Clk_{ref}$ is used to determine the input signal of the counter depending on the temperature. The $Clk_{ref}$ is 1 GHz. As using the SR latch, the output signal of the counter is maintained. The proposed digital temperature sensor operation timing diagram is shown in Figure 3.23.

Figure 3.22: Proposed digital temperature sensor
Figure 3.23: Proposed digital temperature sensor timing diagram
Chapter 4

Proposed Analog Temperature Sensor

The on-chip temperature sensors have been becoming smaller and more accurate. To monitor more accurate temperature of the chips, the smaller area and lower power consumption on-chip temperature sensor is desired. The small area temperature sensors are required to have high accuracy to maximize performance of DTM techniques because the hot spots need to be monitored with an appropriate number of temperature sensors. In aspect of accuracy, BJT based temperature sensors are the optimum solution. However, the BJT based temperature sensors occupy large area and consume large amount of power. In the previous temperature sensor designs, they can achieve high accuracy [25, 26, 27]. To satisfy the demand of small area, low power, and accuracy temperature sensor, a temperature sensor using the subthreshold voltage is proposed [28]. The subthreshold voltage temperature sensor which is shown in Figure 4.1 consists of a single sensing PMOS device. The subthreshold temperature sensor can achieve high accuracy with small area.
The subthreshold voltage has linear relationship of temperature. The equation can be written as [29]

\[ V_{TH}(T) = V_{TH}(T_O) + K_{V_{TH}}(T - T_O) \]  \hspace{1cm} (4.1)

where \( T \) is temperature, \( T_O \) is reference temperature which is 300K, and \( K_{V_{TH}} \) is \( \partial V_T / \partial T \) which is the temperature coefficient. The temperature coefficient \( (K_{V_{TH}}) \) is a negative constant.

To measure subthreshold voltage of the temperature sensing part, the discharging characteristic of pMOS transistor is employed. The discharging behavior of the pMOS array shows threshold voltage drop. The pre-charging pMOS transistor charges the source node of the pMOS transistor array. After the source is fully charged, the pre-charging pMOS transistor
CHAPTER 4. PROPOSED ANALOG TEMPERATURE SENSOR

is turned off. The pMOS transistor array is turned on and begins discharging. The pMOS transistor array discharges rapidly in the strong inversion region. When the pMOS transistor array reaches the weak inversion region, the discharging speed is greatly reduced. The source node of the pMOS transistor array discharges slowly like the threshold voltage drop. The subthreshold temperature sensor operation is shown in Figure 4.2. In the subthreshold temperature sensor design, the appropriate sampling time is the most important component. In [28], the optimal sampling time range is considered with several standards which are good linearity, robustness against leakage current, process variation, and pre-charged level variation.

![Subthreshold temperature sensor front-end operation](image)

**Figure 4.2**: Subthreshold temperature sensor front-end operation

The leakage current is exponentially related with $V_{TH}$ of the pMOS transistor array or temperature. If the temperature sensor samples the node voltage too late, the linearity will be affected. With faster sampling time, moreover, the discharging rate increases exponentially.
CHAPTER 4. PROPOSED ANALOG TEMPERATURE SENSOR

The weak inversion current equation is written as

\[ I_{\text{weak}} = I_O \cdot \frac{W}{L} \cdot e^{\left(\frac{V_{GS} - V_{TH}(T)}{nV_T}\right)} \]  

(4.2)

where \( V_T \) is the thermal voltage which is \( kT/q \). The weak inversion current is affected by the value of \( V_{GS} - V_{TH}(T) \). To simplify the design process, the exponential part of the weak inversion current equation needs to be removed. The proposed subthreshold voltage temperature sensor consists of the temperature sensing part and a summing amplifier. Figure 4.3 shows the proposed subthreshold voltage temperature sensor.

![Proposed subthreshold temperature sensor](image)

Figure 4.3: Proposed subthreshold temperature sensor

To charge the pMOS M1, the pre-charging switch is turned on. During the pre-charging process, other switches for pMOS M4 and M5 are turned off. Once the Vsense node is
CHAPTER 4. PROPOSED ANALOG TEMPERATURE SENSOR

pre-charged, the switches of M4 and M5 are turned on to start discharging. At the same
time, the pre-charging switch is turned off. The pMOS M2 starts discharging and reaches
a weak inversion region. To reduce sampling time and simplify the design, the value of
$V_{GS} - V_{TH}(T)$ should be removed. The summing amplifier which is shown in Figure 4.4
can eliminate the exponential part in the weak inversion current equation.

![Summing Amplifier Diagram]

Figure 4.4: Summing amplifier

$$V_{out} = \frac{R_3}{R_1}(V_C - V_A) + \frac{R_3}{R_2}(V_D - V_B) \quad (4.3)$$

where,

- $V_A =$ Supply Voltage ($V_{DD}$)
- $V_B =$ Ground (0V)
- $V_C =$ $V_{node}$ (Output node)
- $V_D =$ $V_{drain}$ ($V_{DD} - |V_{THP}|$)
CHAPTER 4. PROPOSED ANALOG TEMPERATURE SENSOR

To remove the value of \( V_{GS} - V_{TH}(T) \) in the exponential term, the gate value of the pMOS M2 is equal to \( V_S - V_{TH}(T) \).

\[
V_{GS} - V_{TH}(T) = 0 \tag{4.4}
\]

\[
V_G - V_S = V_{TH} \tag{4.5}
\]

\[
V_G = V_{node} - |V_{THP}| \tag{4.6}
\]

All of the resistors have the same amount of resistance. \( V_C \) is \( V_{node} \) and \( V_D \) is the drain voltage of the pMOS transistor. Since the value of the \( V_{THP} \) is required, the drain voltage of the pMOS transistor is subtracted by the supply voltage. Therefore, \( V_A \) is the supply voltage and \( V_B \) is the zero voltage which is the ground connection. The output value of the summing amplifier is \( V_{node} - |V_{THP}| \). The output value of the summing amplifier is applied to the gate of the pMOS M2.

4.1 Body Connection

The proposed temperature sensor circuit and the temperature sensor circuit without the summing amplifier are compared with different body connections. Table 4.1 shows the comparison of the temperature sensor circuit without the summing amplifier with the different body connections. Table 4.2 shows the comparison of the proposed temperature sensor circuit with the different body connections.
CHAPTER 4. PROPOSED ANALOG TEMPERATURE SENSOR

Table 4.1: Temperature sensor without summing amplifier

<table>
<thead>
<tr>
<th>Body connection</th>
<th>Settling time</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>$\approx 100\mu s$</td>
<td>1.193 mV/$^\circ$C</td>
</tr>
<tr>
<td>Ground</td>
<td>$\approx 10\mu s$</td>
<td>1.15 mV/$^\circ$C</td>
</tr>
<tr>
<td>$V_{source}$</td>
<td>$\approx 10\mu s$</td>
<td>1.34 mV/$^\circ$C</td>
</tr>
</tbody>
</table>

Table 4.2: Proposed temperature sensor

<table>
<thead>
<tr>
<th>Body connection</th>
<th>Settling time</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>$\approx 4\mu s$</td>
<td>1.397 mV/$^\circ$C</td>
</tr>
<tr>
<td>Ground</td>
<td>$\approx 7\mu s$</td>
<td>1.134 mV/$^\circ$C</td>
</tr>
<tr>
<td>$V_{source}$</td>
<td>$\approx 4\mu s$</td>
<td>1.03 mV/$^\circ$C</td>
</tr>
</tbody>
</table>

When the temperature sensor circuit without the summing amplifier has the body connection with the power supply voltage, the optimal sampling time is around $100\mu s$ and the resolution is 1.193 mV/$^\circ$C. If the temperature sensor circuit has the body connection with the ground, the optimal sampling time is around $10\mu s$ and the resolution is 1.15 mV/$^\circ$C. Lastly, the temperature sensor circuit has the body connection with the source node, the optimal sampling time is around $10\mu s$ and the resolution is 1.34 mV/$^\circ$C.

When the proposed temperature sensor has the body connection with the $V_{DD}$, the output voltage is stable around $4\mu s$ and the resolution is 1.397 mV/$^\circ$C. If the proposed temperature sensor has the body connection with the ground, the output voltage is stable around $7\mu s$ and the resolution is 1.134 mV/$^\circ$C. Lastly, the proposed temperature sensor has the body connection with the source node, the output voltage is stable around $4\mu s$ and the resolution is 1.03 mV/$^\circ$C.

The temperature sensor without the summing amplifier is required to calculate a complicated equation to determine the optimal sampling time. Since the exponential term is removed in the proposed temperature sensor, the complicated calculation is not required.
CHAPTER 4. PROPOSED ANALOG TEMPERATURE SENSOR

and the settling time is faster than the temperature sensor without the summing amplifier. Moreover, the proposed temperature sensor which has the body connection with the $V_{DD}$ can achieve the best accuracy.

Figure 4.5 shows different body connections with the power supply voltage, the ground, and the source node of the sensing pMOS transistor.
CHAPTER 4. PROPOSED ANALOG TEMPERATURE SENSOR

4.2 Proposed Analog Temperature Sensor Operation

The proposed analog subthreshold voltage temperature sensor is shown in Figure 4.6. Since the output of the analog subthreshold temperature sensor is stable because of the summing amplifier, a sample and hold circuit is not required.

![Diagram of proposed analog temperature sensor]

Figure 4.6: Proposed subthreshold temperature sensor

At the beginning, the analog temperature output node, V_{sense}, is pre-charged and starts discharging after the pre-charging pMOS transistor is turned off. The switching pulse is high when the pre-charge pulse becomes low. When the rest pulse is high, the input node voltage of the comparator, V_{out}, charges with the same amount of the value as V_{ref}. The
CHAPTER 4. PROPOSED ANALOG TEMPERATURE SENSOR

node voltage $V_{\text{out}}$ decreases while the sample pulse is high. When the reference pulse is high, the node voltage $V_{\text{out}}$ increases. The comparator compares the node voltage $V_{\text{out}}$ and $V_{\text{comp}}$. The $V_{\text{comp}}$ is 275 mV with the typical-typical corner condition. With the fast-fast corner, the $V_{\text{comp}}$ is 325 mV. Lastly, the $V_{\text{comp}}$ is 240 mV with the slow-slow corner. To produce a pulse which is transferred to the digital code, a 3-input AND gate is employed. The output pulse signal of the comparator, reference pulse signal, and 400 MHz pulse signal enter the 3-input AND gate. The output pulse signal of the 3-input AND gate is used as the input signal of the counter to be transferred to the digital code.

At the lowest temperature among the monitoring range, the discharging node voltage, $V_{\text{sense}}$, is highest. Since the decreasing rate is negative, the counter input pulse width is at its narrowest at the lowest temperature.

$$V_{\text{out \ decreasing rate}} = -\frac{V_{\text{sense}}}{R_7 \cdot C} \quad (4.7)$$

$$V_{\text{out \ increasing rate}} = \frac{V_{\text{comp}}}{R_7 \cdot C} \quad (4.8)$$
CHAPTER 4. PROPOSED ANALOG TEMPERATURE SENSOR

Figure 4.7: Proposed subthreshold temperature sensor timing diagram
Chapter 5

Simulation Results

The proposed digital and analog temperature sensor is simulated with 180 nm CMOS process and 1.8 V power supply.

5.1 Proposed Temperature Sensor

5.1.1 Temperature-to-Pulse Generator

The temperature-to-pulse generator consists of the temperature dependent delay line, the D flip-flop based T flip-flop, and the XOR gate. The input pulse signal is applied to the D flip-flop based T flip-flop and the inverter cell which produces the inverted pulse signal to be applied to the XOR gate. The output pulse signal of the T flip-flop is reduced to half as much frequency as the input pulse signal. It passes through the temperature dependent delay line which consists of 52 modified IICDCs. The modified IICDC chain generates about
1.329 $\mu W$ at 27°C. Since the proposed digital temperature sensor only uses the pulse which is delayed from the rising edge, the output pulse of the XOR gate at rising edge requires monitoring and the output pulse of the XOR gate at falling edge needs to be removed. To eliminate the output pulse signal at the falling edge, another pulse signal is employed. In the proposed digital sensor, the input signal is used instead of using the temperature insensitive cells. The linear range of the fast-fast process corner starts near 1 $\mu s$. Therefore, the pulse signal, which is employed to reduce the offset, has to rise at 1 $\mu s$. As a result, the 500 kHz pulse signal is applied as the input signal. Moreover, the 250 kHz pulse signal is used to remove the pulse signal which is produced at the falling edge to cover the slow-slow and the fast-fast process corners. Figure 5.1 shows the fast-fast corner result, Figure 5.2 shows the typical-typical corner result, and Figure 5.3 shows the slow-slow corner result.

In the proposed digital temperature sensor, the power consumption is 323.64 $\mu W$ at 27°C. Since the lower frequency is applied as the input signal, the power consumption is reduced. The power consumption equation is following [31].

$$P \approx C_L \cdot V_{DD}^2 \cdot f \quad (5.1)$$

where $C_L$ is the load capacitance, $V_{DD}$ is the power supply, and $f$ is the frequency. By choosing the lowest frequency, each corner interference can be avoided which improves the design of the low power digital temperature sensor.

The digital output codes can be acquired with the temperature dependent pulse signal by using TDC. Figure 5.4 shows the digital output code with different process corners.
CHAPTER 5. SIMULATION RESULTS

(a) Pulse signal

(b) Pulse width

Figure 5.1: Fast - Fast corner
CHAPTER 5. SIMULATION RESULTS

Figure 5.2: Typical - Typical corner

(a) Pulse signal

(b) Pulse width
CHAPTER 5. SIMULATION RESULTS

(a) Pulse signal

(b) Pulse width

Figure 5.3: Slow - Slow corner
Figure 5.4: Digital output code
CHAPTER 5. SIMULATION RESULTS

According to the digital output code, the resolution of the digital temperature sensor is 0.52°C in the linear region, which ranges from -20°C to 110°C. Table 5.1 shows the comparison of the digital temperature sensors.

Table 5.1: Comparison of the digital temperature sensors

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[25]</th>
<th>[32]</th>
<th>[33]</th>
<th>[34]</th>
<th>[35]</th>
<th>[36]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature range</td>
<td>0-110</td>
<td>-45-85</td>
<td>0-100</td>
<td>0-100</td>
<td>0-100</td>
<td>0-100</td>
<td>-20-110</td>
</tr>
<tr>
<td>Resolution (°C)</td>
<td>0.18</td>
<td>0.42</td>
<td>0.66</td>
<td>NA</td>
<td>0.5</td>
<td>0.78</td>
<td>0.52</td>
</tr>
<tr>
<td>Power consumption (µW)</td>
<td>500</td>
<td>478</td>
<td>1200</td>
<td>360</td>
<td>1111.2</td>
<td>1200</td>
<td>323.64</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>1.0</td>
<td>-</td>
<td>1.2</td>
<td>0.6-1</td>
<td>1.35</td>
<td>1.2</td>
<td>1.8</td>
</tr>
<tr>
<td>Technology</td>
<td>65 nm</td>
<td>180 nm</td>
<td>130 nm</td>
<td>65 nm</td>
<td>14 nm</td>
<td>130 nm</td>
<td>180 nm</td>
</tr>
</tbody>
</table>

5.2 Proposed Analog Temperature Sensor

The proposed analog subthreshold temperature sensor consists of the pre-charging pMOS, the temperature sensing pMOS, the summing amplifier, and the ADC. To reduce the power consumption, two pMOS switches are employed. While the pre-charging pMOS is turned on, the switches block the current flowing through the next blocks. After the pre-charging process is completed, the pre-charging pMOS is turned off and the switches are turned on to begin discharging. The analog temperature sensor front-end consumes 11.19 µW. In the ADC, the comparator generates the pulse, which varies according to temperature. The 3-input AND gate is employed to produce the input signal of the counter. The reference pulse, the comparator output, and 400 MHz ADC reference pulse enter the 3-input AND gate. The fast-fast corner result is shown in Figure 5.5. The typical-typical corner result is shown in Figure 5.6. Figure 5.7 describes the slow-slow corner result.
CHAPTER 5. SIMULATION RESULTS

(a) Vsense output voltage

(b) Aalog temperature sensor digital output code

Figure 5.5: Fast - Fast corner
CHAPTER 5. SIMULATION RESULTS

![Graph](image)

(a) Vsense output voltage

(b) Analog temperature sensor digital output code

Figure 5.6: Typical - Typical corner
CHAPTER 5. SIMULATION RESULTS

(a) Vsense output voltage

(b) Aalog temperature sensor digital output code

Figure 5.7: Slow - Slow corner
CHAPTER 5. SIMULATION RESULTS

As shown in the Vsense graph, the temperature coefficient of the analog temperature sensor front-end is $1.38 \text{mV} / ^\circ C$. The resolution of the analog temperature sensor is $0.75 ^\circ C$. Moreover, the analog subthreshold temperature sensor can monitor the temperature linearly from $-20 ^\circ C$ to $130 ^\circ C$. Table 5.2 shows the comparison of the digital temperature sensors.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[37]</th>
<th>[38]</th>
<th>[39]</th>
<th>[40]</th>
<th>[41]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature range</td>
<td>−10-125</td>
<td>20-100</td>
<td>−40-125</td>
<td>−55-125</td>
<td>−40-125</td>
<td>−20-130</td>
</tr>
<tr>
<td>Resolution ($^\circ C$)</td>
<td>0.6</td>
<td>0.19</td>
<td>0.21</td>
<td>N/A</td>
<td>0.36</td>
<td>0.75</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>3.6</td>
<td>3.78</td>
<td>3.1</td>
<td>7.8</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>1.35</td>
<td>1.4-1.8</td>
<td>1</td>
<td>1.35</td>
<td>0.9-1.2</td>
<td>1.8</td>
</tr>
<tr>
<td>Technology</td>
<td>160 nm</td>
<td>32 nm</td>
<td>160 nm</td>
<td>14 nm</td>
<td>40 nm</td>
<td>180 nm</td>
</tr>
</tbody>
</table>
Chapter 6

Conclusion

This thesis presents the low power consumption digital and analog temperature sensor. The digital temperature sensor is proposed with the modified IICDCs. The proposed temperature sensor monitors from $-20^\circ C$ to $110^\circ C$. The proposed temperature-to-pulse generator by using the modified IICDC can produce the pulse width with a lower power consumption than the conventional approach using other delay cells. Since the input signal is used to reduce the offset, the temperature sensor does not require using temperature independent delay cells and consumes lower power. The resolution is $0.52^\circ C$ and the total digital temperature sensor consumes $323.64 \mu W$ at the $27^\circ C$. The proposed analog subthreshold temperature sensor consists of the pre-charge pMOS transistor, the temperature sensing pMOS transistor, the summing amplifier, and the ADC. Once the temperature sensing pMOS transistor enters the weak inversion, the discharging begins. The summing amplifier can remove the exponential term in the weak inversion current equation. The
CHAPTER 6. CONCLUSION

output voltage becomes stable after approximately 4 µs. The resolution of the analog temperature sensor is 0.75°C. The power consumption of the temperature sensor front-end is 11.19 µW. The digital temperature sensor with the dual-slope ADC consumes 2.5 mW at 27°C. The proposed digital and analog temperature sensor is designed using 180 nm standard CMOS technology with 1.8 V power supply. The proposed temperature sensors turn out to be cost and overhead effective, and they will be a very useful references for the future on-chip temperature sensor designs.
Bibliography


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Appendix A

Netlist for A Digital Temperature Sensor

// Generated for: spectre
// Generated on: Mar 2 14:24:31 2018
// Design library name: Temp_sensor
// Design cell name: TB_2_21
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
parameters ref=1n F=0.5M
include ”/home/centos/workspaces/HL18G-SL3.7/SPECTRE/corner_HL18G.scs” section=ttt

// Library name: Temp_sensor
// Cell name: NAND
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

// View name: schematic

subckt NAND A B Gnd Out Vdd

NM1 (net16 B Gnd Gnd) nch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1) NM0 (Out A net16 Gnd) nch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1) PM1 (Out B Vdd Vdd) pch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1) PM0 (Out A Vdd Vdd) pch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1)

ends NAND

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: XOR

// View name: schematic

subckt XOR A B Gnd Out Vdd

I3 (net11 net12 Gnd Out Vdd) NAND

I2 (A B Gnd net9 Vdd) NAND

I1 (net9 B Gnd net12 Vdd) NAND

I0 (A net9 Gnd net11 Vdd) NAND
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

ends XOR
// End of subcircuit definition.

// Library name: Temp_sensor
// Cell name: inverter
// View name: schematic
subckt inverter IN OUT VDD gnd
NM2 (OUT IN gnd gnd) nch_tn w=(1u) l=180n ad=480f as=480f pd=2.96u
ps=2.96u nrd=480m nrs=480m m=(1)*(1)
PM2 (OUT IN VDD VDD) pch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u
ps=4.96u nrd=240m nrs=240m m=(1)*(1)
ends inverter
// End of subcircuit definition.

// Library name: Temp_sensor
// Cell name: 3NAND
// View name: schematic
subckt Temp_sensor_3NAND_schematic A B C Gnd Out Vdd
PM2 (Out A Vdd Vdd) pch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u
ps=4.96u nrd=240m nrs=240m m=(1)*(1)
PM1 (Out C Vdd Vdd) pch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

\[ \text{ps} = 4.96u \text{ nrd}=240m \text{ nrs}=240m \text{ m}=(1)^*(1) \]

PM0 (Out B Vdd Vdd) pch \_tn \ w=(2u) \ l=180n \ ad=960f \ as=960f \ pd=4.96u

\[ \text{ps} = 4.96u \text{ nrd}=240m \text{ nrs}=240m \text{ m}=(1)^*(1) \]

NM2 (net21 C Gnd Gnd) nch \_tn \ w=(3u) \ l=180n \ ad=1.44p \ as=1.44p \ pd=6.96u

\[ \text{ps} = 6.96u \text{ nrd}=160m \text{ nrs}=160m \text{ m}=(1)^*(1) \]

NM1 (net22 B net21 Gnd) nch \_tn \ w=(3u) \ l=180n \ ad=1.44p \ as=1.44p \ pd=6.96u

\[ \text{ps} = 6.96u \text{ nrd}=160m \text{ nrs}=160m \text{ m}=(1)^*(1) \]

NM0 (Out A net22 Gnd) nch \_tn \ w=(3u) \ l=180n \ ad=1.44p \ as=1.44p \ pd=6.96u

\[ \text{ps} = 6.96u \text{ nrd}=160m \text{ nrs}=160m \text{ m}=(1)^*(1) \]

ends Temp\_sensor\_3NAND\_schematic

// End of subcircuit definition.

// Library name: Temp\_sensor

// Cell name: DFF\_nores

// View name: schematic

subckt DFF\_nores Clk D Gnd Q Qb Vdd

I15 (net9 Clk net10 Gnd net3 Vdd) Temp\_sensor\_3NAND\_schematic

I13 (net10 net9 Gnd net8 Vdd) NAND

I19 (net8 Clk Gnd net9 Vdd) NAND

I20 (Q net3 Gnd Qb Vdd) NAND

I18 (net9 Qb Gnd Q Vdd) NAND
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

I21 (net3 D Gnd net10 Vdd) NAND
ends DFF_nores

// End of subcircuit definition.

// Library name: Temp_sensor
// Cell name: buffer_body1
// View name: schematic

subckt buffer_body1 IN NB OUT PB VDD gnd

NM2 (net10 IN gnd NB) nch tn w=(220n) l=2u ad=198.4f as=198.4f
pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)

NM3 (OUT net10 gnd NB) nch tn w=(220n) l=2u ad=198.4f as=198.4f
pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)

PM2 (net10 IN VDD PB) pch tn w=(440n) l=2u ad=211.2f as=211.2f
pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)

PM3 (OUT net10 VDD PB) pch tn w=(440n) l=2u ad=211.2f as=211.2f
pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)
ends buffer_body1

// End of subcircuit definition.

// Library name: Temp_sensor
// Cell name: IICDC4_test2
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

// View name: schematic

subckt IICDC4_test2 Gnd In Nb Out Pb Vdd

NM26 (net9 net05 net039 Nb) nch_tn w=(220n) l=1u ad=198.4f as=198.4f
pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)

NM29 (net27 net17 net028 Nb) nch_tn w=(220n) l=1u ad=198.4f as=198.4f
pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)

NM24 (net10 net06 net9 Nb) nch_tn w=(220n) l=1u ad=198.4f as=198.4f
pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)

NM25 (net7 In Gnd Nb) nch_tn w=(220n) l=1u ad=198.4f as=198.4f
pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)

NM23 (net039 net045 net7 Nb) nch_tn w=(220n) l=1u ad=198.4f as=198.4f
pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)

NM27 (Out net10 net27 Nb) nch_tn w=(220n) l=1u ad=198.4f as=198.4f
pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)

PM53 (net25 net20 Vdd Pb) pch_tn w=(440n) l=1u ad=211.2f as=211.2f
pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)

PM41 (net7 In Vdd Pb) pch_tn w=(440n) l=1u ad=211.2f as=211.2f
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)
PM40 (net10 net06 net9 Pb) pch_tn w=(440n) l=1u ad=211.2f as=211.2f
pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)
PM52 (net028 net19 net25 Pb) pch_tn w=(440n) l=1u ad=211.2f as=211.2f
pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)
PM42 (net039 net045 net7 Pb) pch_tn w=(440n) l=1u ad=211.2f as=211.2f
pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)
PM39 (net9 net05 net039 Pb) pch_tn w=(440n) l=1u ad=211.2f as=211.2f
pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)
PM54 (net27 net17 net028 Pb) pch_tn w=(440n) l=1u ad=211.2f as=211.2f
pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)
PM55 (Out net10 net27 Pb) pch_tn w=(440n) l=1u ad=211.2f as=211.2f
pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)
I33 (net7 Gnd net20 Vdd Vdd Gnd) buffer_body1
I41 (net27 Gnd net06 Vdd Vdd Gnd) buffer_body1
I39 (net9 Gnd net17 Vdd Vdd Gnd) buffer_body1
I40 (net028 Gnd net05 Vdd Vdd Gnd) buffer_body1
I38 (net039 Gnd net19 Vdd Vdd Gnd) buffer_body1
I37 (net25 Gnd net045 Vdd Vdd Gnd) buffer_body1
ends IICDC4_test2

// End of subcircuit definition.
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

// Library name: Temp_sensor

// Cell name: pulse_gen_2_16

// View name: schematic

subckt pulse_gen_2_16 Gnd In Out Vdd

I94 (net0114 IICDC Gnd net118 Vdd) XOR

I3921 (net137 Out Vdd Gnd) inverter

I4106 (In net0114 Vdd Gnd) inverter

I3990 (In net114 Gnd in2 net114 Vdd) DFF_nores

I4052 (Gnd in2 Gnd net0148 Vdd Vdd) IICDC4_test2

I4078 (Gnd net0144 Gnd net0143 Vdd Vdd) IICDC4_test2

I4094 (Gnd net0127 Gnd net0126 Vdd Vdd) IICDC4_test2

I4087 (Gnd net0157 Gnd net0125 Vdd Vdd) IICDC4_test2

I4084 (Gnd net0150 Gnd net0120 Vdd Vdd) IICDC4_test2

I4058 (Gnd net0117 Gnd net0158 Vdd Vdd) IICDC4_test2

I4100 (Gnd net0163 Gnd net0131 Vdd Vdd) IICDC4_test2

I4085 (Gnd net0120 Gnd net0153 Vdd Vdd) IICDC4_test2

I4096 (Gnd net0121 Gnd net0149 Vdd Vdd) IICDC4_test2

I4092 (Gnd net0151 Gnd net02 Vdd Vdd) IICDC4_test2

I4075 (Gnd net0118 Gnd net0154 Vdd Vdd) IICDC4_test2

I4066 (Gnd net0132 Gnd net0159 Vdd Vdd) IICDC4_test2
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

I4057 (Gnd net0158 Gnd net0129 Vdd Vdd) IICDC4_test2
I4093 (Gnd net0126 Gnd net0151 Vdd Vdd) IICDC4_test2
I4059 (Gnd net0152 Gnd net0117 Vdd Vdd) IICDC4_test2
I4105 (Gnd net0182 Gnd IICDC Vdd Vdd) IICDC4_test2
I4055 (Gnd net0161 Gnd net0152 Vdd Vdd) IICDC4_test2
I4062 (Gnd net0139 Gnd net0134 Vdd Vdd) IICDC4_test2
I4063 (Gnd net0134 Gnd net5 Vdd Vdd) IICDC4_test2
I4083 (Gnd net0156 Gnd net0150 Vdd Vdd) IICDC4_test2
I4069 (Gnd net0138 Gnd net0133 Vdd Vdd) IICDC4_test2
I4076 (Gnd net0119 Gnd net0118 Vdd Vdd) IICDC4_test2
I4091 (Gnd net0145 Gnd net3 Vdd Vdd) IICDC4_test2
I4099 (Gnd net0131 Gnd net0130 Vdd Vdd) IICDC4_test2
I4082 (Gnd net4 Gnd net0156 Vdd Vdd) IICDC4_test2
I4060 (Gnd net0140 Gnd net6 Vdd Vdd) IICDC4_test2
I4053 (Gnd net0148 Gnd net0147 Vdd Vdd) IICDC4_test2
I4095 (Gnd net0149 Gnd net0127 Vdd Vdd) IICDC4_test2
I4070 (Gnd net0155 Gnd net0138 Vdd Vdd) IICDC4_test2
I4061 (Gnd net0128 Gnd net0140 Vdd Vdd) IICDC4_test2
I4071 (Gnd net6 Gnd net0155 Vdd Vdd) IICDC4_test2
I4072 (Gnd net0123 Gnd net4 Vdd Vdd) IICDC4_test2
I4064 (Gnd net0141 Gnd net0139 Vdd Vdd) IICDC4_test2
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

I4089 (Gnd net0135 Gnd net0146 Vdd Vdd) IICDC4_test2
I4090 (Gnd net0146 Gnd net0145 Vdd Vdd) IICDC4_test2
I4104 (Gnd net02 Gnd net0182 Vdd Vdd) IICDC4_test2
I4086 (Gnd net0153 Gnd net0157 Vdd Vdd) IICDC4_test2
I4097 (Gnd net0122 Gnd net0121 Vdd Vdd) IICDC4_test2
I4101 (Gnd net3 Gnd net0163 Vdd Vdd) IICDC4_test2
I4088 (Gnd net0125 Gnd net0135 Vdd Vdd) IICDC4_test2
I4054 (Gnd net0147 Gnd net0161 Vdd Vdd) IICDC4_test2
I4098 (Gnd net0130 Gnd net0121 Vdd Vdd) IICDC4_test2
I4065 (Gnd net0137 Gnd net0141 Vdd Vdd) IICDC4_test2
I4079 (Gnd net0162 Gnd net0144 Vdd Vdd) IICDC4_test2
I4077 (Gnd net0143 Gnd net0119 Vdd Vdd) IICDC4_test2
I4056 (Gnd net0129 Gnd net0128 Vdd Vdd) IICDC4_test2
I4081 (Gnd net5 Gnd net0160 Vdd Vdd) IICDC4_test2
I4068 (Gnd net0133 Gnd net0132 Vdd Vdd) IICDC4_test2
I4074 (Gnd net0154 Gnd net0124 Vdd Vdd) IICDC4_test2
I4073 (Gnd net0124 Gnd net0123 Vdd Vdd) IICDC4_test2
I4067 (Gnd net0159 Gnd net0137 Vdd Vdd) IICDC4_test2
I4080 (Gnd net0160 Gnd net0162 Vdd Vdd) IICDC4_test2
I18 (net118 in2 Gnd net137 Vdd) NAND

ends pulse_gen_2_16
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

// End of subcircuit definition.

// Library name: Temp_sensor
// Cell name: SRLatch
// View name: schematic
subckt SRLatch En Gnd Q Qb R S Vdd
I12 (net17 Qb Gnd Q Vdd) NAND
I13 (Q net16 Gnd Qb Vdd) NAND
I1 (S En Gnd net17 Vdd) NAND
I0 (En R Gnd net16 Vdd) NAND
ends SRLatch

// End of subcircuit definition.

// Library name: Temp_sensor
// Cell name: Digital_Code1
// View name: schematic
subckt Digital_Code1 En Gnd Q1 Q10 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 S1 S10 S2 S3 S4 S5 S6 S7 S8 S9 Vdd q1 q10 q2 q3 q4 q5 q6 q7 q8 q9
I43 (S10 net026 Vdd Gnd) inverter
I83 (S4 net15 Vdd Gnd) inverter
I87 (S3 net16 Vdd Gnd) inverter
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

I81 (S2 net17 Vdd Gnd) inverter
I120 (S5 net14 Vdd Gnd) inverter
I35 (S6 net016 Vdd Gnd) inverter
I37 (S7 net017 Vdd Gnd) inverter
I76 (S1 net18 Vdd Gnd) inverter
I41 (S9 net023 Vdd Gnd) inverter
I40 (S8 net020 Vdd Gnd) inverter
I44 (En Gnd Q10 q10 net026 S10 Vdd) SR_latch
I63 (En Gnd Q4 q4 net15 S4 Vdd) SR_latch
I42 (En Gnd Q9 q9 net023 S9 Vdd) SR_latch
I39 (En Gnd Q8 q8 net020 S8 Vdd) SR_latch
I114 (En Gnd Q5 q5 net14 S5 Vdd) SR_latch
I38 (En Gnd Q7 q7 net017 S7 Vdd) SR_latch
I36 (En Gnd Q6 q6 net016 S6 Vdd) SR_latch
I75 (En Gnd Q3 q3 net16 S3 Vdd) SR_latch
I0 (En Gnd Q2 q2 net17 S2 Vdd) SR_latch
I59 (En Gnd Q1 q1 net18 S1 Vdd) SR_latch
ends Digital_Code1

// End of subcircuit definition.

// Library name: Temp_sensor
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

// Cell name: DFF

// View name: schematic

subckt DFF Clk D Gnd Q Qb Reset Vdd

I14 (net8 Clk Reset Gnd net9 Vdd) Temp_sensor_3NAND_schematic
I17 (Q net3 Reset Gnd Qb Vdd) Temp_sensor_3NAND_schematic
I16 (net3 D Reset Gnd net10 Vdd) Temp_sensor_3NAND_schematic
I15 (net9 Clk net10 Gnd net3 Vdd) Temp_sensor_3NAND_schematic
I13 (net10 net9 Gnd net8 Vdd) NAND
I18 (net9 Qb Gnd Q Vdd) NAND

ends DFF

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: Counter1

// View name: schematic

subckt Counter1 En Gnd Q1 Q10 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Vdd reset

I305 (net018 net020 Gnd Q10 net020 reset Vdd) DFF
I304 (net7 net9 Gnd Q5 net9 reset Vdd) DFF
I284 (net10 net12 Gnd Q3 net12 reset Vdd) DFF
I302 (net014 net016 Gnd Q8 net016 reset Vdd) DFF
I33 (En net8 Gnd Q1 net8 reset Vdd) DFF
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

I300 (net9 net011 Gnd Q6 net011 reset Vdd) DFF
I281 (net8 net10 Gnd Q2 net10 reset Vdd) DFF
I303 (net016 net018 Gnd Q9 net018 reset Vdd) DFF
I287 (net12 net7 Gnd Q4 net7 reset Vdd) DFF
I301 (net011 net014 Gnd Q7 net014 reset Vdd) DFF

ends Counter1

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: TB_2_21

// View name: schematic

V5 (net036 0) vsource dc=0 mag=1 type=pulse val0=0 val1=1.8 period=ref
V2 (In 0) vsource dc=0 mag=1 type=pulse val0=0 val1=1.8 period=1/F
NM27 (net041 Temptopulse 0 0) nch_txn w=(1u) l=180n ad=480f as=480f
   pd=2.96u ps=2.96u nrd=480m nrs=480m m=(1)*(1)
NM23 (TDC_in net041 0 0) nchtxn w=(2u) l=180n ad=960f as=960f pd=4.96u
   ps=4.96u nrd=240m nrs=240m m=(1)*(1)
I457 (0 In Temptopulse vdd!) pulse_gen_2_16
PM27 (net041 Temptopulse vdd! vdd!) pch_txn w=(2u) l=180n ad=960f
   as=960f pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1)
PM23 (TDC_in net041 vdd! vdd!) pch_txn w=(4u) l=180n ad=1.92p as=1.92p
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

pd=8.96u ps=8.96u nrd=120m nrs=120m m=(1)*(1)
I456 (Temptopulse 0 1 10 2 3 4 5 6 7 8 9 net25 net035 net24 net23
net22 net21 net20 net19 net031 net033 vdd! q1 q10 q2 q3 q4 q5 q6
q7 q8 q9) Digital_Code1
V0 (vdd! 0) vsource dc=1.8 type=dc
I451 (net036 0 net25 net035 net24 net23 net22 net21 net20 net19 net031
net033 vdd! TDC_in) Counter1
ic 10=0 I457.in2=0 7=0 8=0 9=0 2=0 6=0 1=0 4=0 3=0 5=0
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=-20.0
tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5
digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output"
checklimitdest=psf
tran tran stop=1.8u errpreset=conservative write="spectre.ic"
writefinal="spectre.fc" annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
APPENDIX A. NETLIST FOR A DIGITAL TEMPERATURE SENSOR

save 1 2 3 4 5 6 7 Temtopulse

saveOptions options save=all currents=all
Appendix B

Netlist for An Analog Temperature Sensor

// Generated for: spectre

// Generated on: Jun 3 11:57:36 2018

// Design library name: Temp_sensor

// Design cell name: ADC_TB2

// Design view name: schematic

simulator lang=spectre

global 0 vdd!

parameters comp=275m period=2.5n res=3u sample=4u ref=5u

include ”/home/centos/workspaces/HL18G-SL3.7/SPECTRE/corner_HL18G.scs” section=ttt
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

// Library name: MPDK_HL18G
// Cell name: rhpo_ns
// View name: schematic
subckt rhpo_ns_pcell_0 MINUS PLUS
parameters segW=2u segL=10u nMcMode=1 mult_top=(1)
R0 (PLUS MINUS) rhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
ends rhpo_ns_pcell_0
// End of subcircuit definition.

// Library name: Temp_sensor
// Cell name: OP_1_1
// View name: schematic
subckt OP_1_1 Gnd Out VI\+ VI\- Vdd ibias
NM2 (Out net022 Gnd Gnd) nch_tn w=(22.2u) l=540n ad=10.656p as=10.656p
pd=45.36u ps=45.36u nrd=21.6216m nrs=21.6216m m=(1)*(1)
NM1 (net14 net14 Gnd Gnd) nch_tn w=(2u) l=540n ad=960f as=960f
pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1)
NM0 (net022 net14 Gnd Gnd) nch_tn w=(2u) l=540n ad=960f as=960f
pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1)
PM8 (ibias ibias Vdd Vdd) pch_tn w=(1.08u) l=540n ad=518.4f as=518.4f
pd=3.12u ps=3.12u nrd=444.444m nrs=444.444m m=(1)*(1)
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

PM4 (Out ibias Vdd Vdd) pch_tn w=(5u) l=540n ad=2.4p as=2.4p pd=10.96u ps=10.96u nrd=96m nrs=96m m=(1)*1

PM3 (net022 VI+ net16 Vdd) pch_tn w=(3.24u) l=540n ad=1.5552p as=1.5552p pd=7.44u ps=7.44u nrd=148.148m nrs=148.148m m=(1)*1

PM2 (net14 VI net16 Vdd) pch_tn w=(3.24u) l=540n ad=1.5552p as=1.5552p pd=7.44u ps=7.44u nrd=148.148m nrs=148.148m m=(1)*1

PM6 (net16 ibias Vdd Vdd) pch_tn w=(1.08u) l=540n ad=518.4f as=518.4f pd=3.12u ps=3.12u nrd=444.444m nrs=444.444m m=(1)*1

C2 (net023 Out) cmim1p1 w=21.445u l=21.445u area=459.888p peri=85.78u entrymode=1 mcmode=1 m=1 mult=1

R0 (net022 net023) rhpo_ns_pcell_0 m=1 segW=2u segL=20u nMcMode=1 mult_top=(1)

ends OP_amp1_1

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: Comparator

// View name: schematic

subckt Comparator GND Ibias Out V+ V- VDD

NM2 (Out net16 GND GND) nch_tn w=(20u) l=180n ad=9.6p as=9.6p pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*1

93
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

NM0 (net16 net11 GND GND) nch_tn w=(8u) l=180n ad=3.84p as=3.84p
pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)

PM4 (net11 net11 GND GND) nch_tn w=(8u) l=180n ad=3.84p as=3.84p
pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)

PM5 (Out net20 VDD VDD) pch_tn w=(8u) l=180n ad=3.84p as=3.84p
pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)

PM3 (net16 V+/ net13 VDD) pch_tn w=(8u) l=180n ad=3.84p as=3.84p
pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)

PM2 (net11 V-/ net13 VDD) pch_tn w=(8u) l=180n ad=3.84p as=3.84p
pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)

PM1 (net13 net20 VDD VDD) pch_tn w=(8u) l=180n ad=3.84p as=3.84p
pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)

NM1 (Ibias net20 VDD VDD) pch_tn w=(8u) l=180n ad=3.84p as=3.84p
pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)

ends Comparator

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: 3NAND

// View name: schematic

subckt Temp_sensor_3NAND_schematic A B C Gnd Out Vdd
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

PM2 (Out A Vdd Vdd) pch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u
ps=4.96u nrd=240m nrs=240m m=(1)*(1)

PM1 (Out C Vdd Vdd) pch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u
ps=4.96u nrd=240m nrs=240m m=(1)*(1)

PM0 (Out B Vdd Vdd) pch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u
ps=4.96u nrd=240m nrs=240m m=(1)*(1)

NM2 (net21 C Gnd Gnd) nch_tn w=(3u) l=180n ad=1.44p as=1.44p pd=6.96u
ps=6.96u nrd=160m nrs=160m m=(1)*(1)

NM1 (net22 B net21 Gnd) nch_tn w=(3u) l=180n ad=1.44p as=1.44p
pd=6.96u ps=6.96u nrd=160m nrs=160m m=(1)*(1)

NM0 (Out A net22 Gnd) nch_tn w=(3u) l=180n ad=1.44p as=1.44p
pd=6.96u ps=6.96u nrd=160m nrs=160m m=(1)*(1)

ends Temp_sensor_3NAND_schematic

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: inverter

// View name: schematic

subckt inverter IN OUT VDD gnd

NM2 (OUT IN gnd gnd) nch_tn w=(220n) l=180n ad=198.4f as=198.4f
pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

PM2 (OUT IN VDD VDD) pch_tn w=(440n) l=180n ad=211.2f as=211.2f
dp=1.8u ps=1.8u nrd=1.09091 nrs=1.09091 m=(1)*(1)

ends inverter

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: Temp_array_5_17

// View name: schematic

subckt Temp_array_5_17 Body Gnd Vdd Vsense

PM2 (Gnd Vsense Vdd Body) pch_tn w=(5u) l=185n ad=1.35p as=1.56p

dp=5.54u ps=6.624u nrd=54m nrs=62.4m m=(1)*(10)

ends Temp_array_5_17

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: NAND

// View name: schematic

subckt NAND A B Gnd Out Vdd

NM1 (net16 B Gnd Gnd) nch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u

ps=4.96u nrd=240m nrs=240m m=(1)*(1)

NM0 (Out A net16 Gnd) nch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

ps=4.96u nrd=240m nrs=240m m=(1)*(1)

PM1 (Out B Vdd Vdd) pch tn w=(2u) l=180n ad=960f as=960f pd=4.96u
ps=4.96u nrd=240m nrs=240m m=(1)*(1)

PM0 (Out A Vdd Vdd) pch tn w=(2u) l=180n ad=960f as=960f pd=4.96u
ps=4.96u nrd=240m nrs=240m m=(1)*(1)

ends NAND

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: DFF

// View name: schematic

subckt DFF Clk D Gnd Q Qb Reset Vdd
I14 (net8 Clk Reset Gnd net9 Vdd) Temp_sensor_3NAND_schematic
I17 (Q net3 Reset Gnd Qb Vdd) Temp_sensor_3NAND_schematic
I16 (net3 D Reset Gnd net10 Vdd) Temp_sensor_3NAND_schematic
I15 (net9 Clk net10 Gnd net3 Vdd) Temp_sensor_3NAND_schematic
I13 (net10 net9 Gnd net8 Vdd) NAND
I18 (net9 Qb Gnd Q Vdd) NAND
ends DFF

// End of subcircuit definition.
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

// Library name: Temp_sensor

// Cell name: Counter1

// View name: schematic

subckt Counter1 En Gnd Q1 Q10 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Vdd reset
I284 (net10 net12 Gnd Q3 net12 reset Vdd) DFF
I302 (net014 net016 Gnd Q8 net016 reset Vdd) DFF
I33 (En net8 Gnd Q1 net8 reset Vdd) DFF
I300 (net9 net011 Gnd Q6 net011 reset Vdd) DFF
I281 (net8 net10 Gnd Q2 net10 reset Vdd) DFF
I303 (net016 net018 Gnd Q9 net018 reset Vdd) DFF
I287 (net12 net7 Gnd Q4 net7 reset Vdd) DFF
I304 (net7 net9 Gnd Q5 net9 reset Vdd) DFF
I305 (net018 net020 Gnd Q10 net020 reset Vdd) DFF
I301 (net011 net014 Gnd Q7 net014 reset Vdd) DFF
ends Counter1

// End of subcircuit definition.

// Library name: Temp_sensor

// Cell name: ADC_TB2

// View name: schematic

I178 (0 out net081 net4 vdd! net15) OP_amp1_1
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

V31 (0 net048) vsource dc=6 type=dc
V32 (net083 0) vsource dc=6 type=dc
V13 (net033 0) vsource dc=comp type=dc
V44 (net081 0) vsource dc=400m type=dc
V21 (vdd! 0) vsource dc=1.8 type=dc
I190 (net019 0) isource dc=2u type=dc
I106 (net15 0) isource dc=2u type=dc
C11 (Vsensor1 0) capacitor c=1p
C0 (net4 out) capacitor c=1p
R44 (net012 Vsense1) resistor r=120K
R40 (net014 0) resistor r=120K
R41 (V net014) resistor r=120K
R39 (net082 net014) resistor r=120K
R43 (vdd! net012) resistor r=120K
R42 (0 net012) resistor r=120K
R0 (net060 net4) resistor r=1.7M
NM2 (net4 res out 0) nch_tn w=(6u) l=180n ad=2.88p as=2.88p pd=12.96u
ps=12.96u nrd=80m nrs=80m m=(1)*{(1)
NM1 (Vsensor1 sample net060 0) nch_tn w=(6u) l=180n ad=2.88p as=2.88p
pd=12.96u ps=12.96u nrd=80m nrs=80m m=(1)*{(1)
NM0 (net060 ref 0 0) nch_tn w=(6u) l=180n ad=2.88p as=2.88p pd=12.96u
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

ps=12.96u nrd=80m nrs=80m m=(1)*(1)
V35 (net053 0) vsource dc=0 type=pulse val0=1.8 val1=0 period=10u delay=1u
V33 (net057 0) vsource dc=0 type=pulse val0=1.8 val1=0 period=10u delay=1u
V34 (net024 0) vsource dc=0 type=pulse val0=1.8 val1=0 period=10u width=1u
V6 (net028 0) vsource dc=0 mag=1 type=pulse val0=0 val1=1.8 period=period
V10 (res 0) vsource type=pulse val0=0 val1=1.8 period=100u delay=res width=1u
V0 (sample 0) vsource type=pulse val0=0 val1=1.8 period=100u delay=sample width=1u
V39 (ref 0) vsource type=pulse val0=0 val1=1.8 period=100u delay=ref width=1u
I239 (0 net019 Comp out net033 vdd!) Comparator
I245 (Comp ref net028 0 net055 vdd!) Temp_sensor_3NAND_schematic
I211 (net055 test vdd! 0) inverter
I199 (res net056 vdd! 0) inverter
I216 (vdd! 0 V1 Vsense1) Temp_array_5_17
I271 (test 0 1 10 2 3 4 5 6 7 8 9 vdd! net056) Counter1
PM30 (net082 net082 vdd! vdd!) pch_tn w=(880n) l=180n ad=422.4f as=422.4f pd=2.72u ps=2.72u nrd=545.455m nrs=545.455m m=(1)*1
PM31 (V net053 V1 vdd!) pch_tn w=(6u) l=180n ad=2.88p as=2.88p pd=12.96u ps=12.96u nrd=80m nrs=80m m=(1)*1
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

PM29 (Vsensor1 net024 vdd! vdd!) pch_tn w=(700n) l=180n ad=336f as=336f pd=2.36u ps=2.36u nrd=685.714m nrs=685.714m m=(1)*1

PM28 (V1 net057 Vsensor1 vdd!) pch_tn w=(6u) l=180n ad=2.88p as=2.88p pd=12.96u ps=12.96u nrd=80m nrs=80m m=(1)*1

I226 (Vsense1 0 net014 net012 net083 net048) opamp gain=1.5M freq_unitygain=8M rin=10M vin_offset=0 ibias=10u rout=5

ic 1=0 2=0 3=0 4=0 5=0 6=0 7=0 8=0
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=130.0 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output"
checklimitdest=psf
tran tran stop=9u errpreset=conservative write="spectre.ic"
writefinal="spectre.fc" annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000 annotate=status
dcOpInfo info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
APPENDIX B. NETLIST FOR AN ANALOG TEMPERATURE SENSOR

subckts info what=subckts where=rawfile

saveOptions options save=allpub currents=all

ahdl_include ”/tools/cadence/IC615/tools/dfII/samples/artist/ahdlLib/opamp/veriloga/veriloga.va”