CLOCK DISTRIBUTION ON STANDING WAVE WITH CMOS ACTIVE INDUCTOR LOADING

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Abstract

Global clock distribution design is becoming an increasingly challenge task for multi GHz microprocessors. Clock skew and jitter requirement are becoming more and more stringent as clock frequency increases. For traditional clock distributions, skew and jitter are proportional to latency, which is dominated by a series of resistive-capacitance delay and does not scale with clock period. Moreover, the resistive-capacitance wire-load consumes a significant amount of power.

As an alternative, resonant clock is applied to reduce dynamic power and achieve better control of clock skew and jitter. There are three approaches to create resonant clocks, standing wave, traveling wave, and L-C tank resonance. Among these approaches, standing wave clock scheme forms an energy efficient tank that dissipates power only at the parasitic resistance of the network. Furthermore, standing wave resonance has uniform phase across the entire clock network, which yields almost zero skew in global clock distribution. But its voltage and current vary spatially. To overcome the position-dependent amplitude variation and low output swing issue, passive inductive loading is proposed, where uniform phase and almost uniform amplitude standing wave is realized.

In this thesis, we extend the idea of clock distribution with inductive loading further by applying CMOS active inductor as inductive loading.
Compared to passive inductor design, active inductor can potentially achieve tunable design with reduced area overhead and high Q value. Moreover, it is compatible with CMOS technology process and easily integrated into chip-sets. The thesis first presents a global clock distribution design by generating standing wave oscillations along inductively loaded micro-strip lines. Transmission line modeling is setting up and analyzed. An improved X-tree clock topology is employed and cross-coupled pair (CCP) is used to reduce loss on transmission line. Then standing wave clock distribution with active inductor loading is presented. Three types of active inductor loading on a standing wave resonant global clock distribution network are proposed. In the first case, we design a CMOS single cascoded active inductor with tuned capacitor to increase Q value. The design with a 0.6 nH active inductance achieves Q of 4630. Applying the active inductor to the entire clock network, the clock jitter introduced by the active inductor is 0.39 ps. Clock skew is 0.39 ps. In the second case, a novel CMOS differential active inductor with CCP compensation is proposed. The design has 1.2 nH inductance and Q of 327. The clock jitter introduced by active inductor loading is 1ps. Clock skew is 0.52 ps. In the last case, a improved CMOS differential cascoded active inductor with 1nH inductance and Q 344 is designed. The clock jitter introduced by active inductor loading is 0.16 ps. Clock skew is 1.95 ps. All the schemes are based on an improved X-tree clock topology and simulated in CMOS 28nm technology. The proposed clock distribution schemes greatly reduce clock skew, jitter, power consumption and chip area.
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1 Introduction

1.1 Motivations

Clock distribution design in multi-GHz systems is becoming more and more challenging. To achieve the desired time margin in synchronous systems, both clock skew and jitter need to be reduced proportionally to the clock period. However, for conventional clock distribution, which is typically buffered clock-tree, the clock skew and jitter are proportional to latency. Regulating skew and jitter to be less than 10% of the total clock cycle is very difficult when clock frequency is above 10GHz.

Furthermore, conventional clock distribution contains a large number of buffers to balance clock paths and reduce clock skew, the highly toggling active elements consume a large amount of the total power, as much as 30% - 50% [1] and in extreme cases, up to 70% [2]. High power consumption would impose more stringent requirements on power supply and heat dissipation. Ultimately it affects the reliability of the systems.

As an alternative solution, resonant clock distribution is applied to have better control on clock skew/jitter and reduce the overall power consumption. Electrical resonance occurs when imaginary parts of impedance cancel out at a particular frequency known as resonant frequency. Meanwhile the recycling energy are restored in the on-chip inductors and save the power. According to this concept, there are three approaches to create resonant clocks: standing wave [3–9], traveling wave [10–14], and L-C tank resonant [15–21].
Standing wave occurs if two harmonic waves of the same frequency and amplitude travel in opposite direction. If the wire length is properly designed at integer of quarter wave length [4], the input signal can be delivered along the line with identical phase but spacial various amplitude. One classic example of standing wave resonance is by shorting both ends of a half wave length transmission line. The standing wave amplitude gets its peak at the center of the line and diminishes to zero at the end of the line. Therefore, auxiliary circuits such as sense amplifiers are needed to convert it to full swing, which leads to more power consumption and susceptible to noise.

The low output swing can be improved by using lumped spiral inductor load instead of shorting the end by wire [7]. The inductor load provides phase shift and acts as a replacement to part of the transmission line. As a result, transmission line positions with relatively large standing wave amplitude are retained, which makes the clock output uniform phase and almost uniform amplitude.

1.2 Summary of Contributions

In this thesis, we extend the idea of clock distribution with inductive loading further by applying CMOS active inductor as inductive loading. Compared to passive inductor design, active inductor can potentially achieve tunable design with reduced area overhead and high Q value. Moreover, it is compatible with CMOS technology process and easily integrated into chip-sets. To get an optimized design, both single-ended and differential active
inductor designs are explored with significant efforts to enhance the quality factor. Issues like transmission loss compensation on clock network when span is comparable to wave length are discussed. For clock distribution topologies, most existing standing wave resonant schemes use grid structure, which is a way to reduce skew, but consume more power and cost large area overhead. Moreover, the mutual inductance from the grid will be an interference source to the entire chip. In this thesis, an improved X-tree clock distribution typology is used, along with the proposed active inductor loading. Detailed designs of 10GHz clock distribution network are presented.

In summary, the purpose of the study is to establish a clock distribution network that transfers clock signals with a minimum skew and jitter while consumes less energy and takes up less chip area. The key contributions of this thesis are:

1. Designed CMOS negative transconductance circuits to compensate transmission line loss for generating standing wave on lossy line

2. Proposed and designed three CMOS active inductor schemes, used as active inductive load to enhance the standing wave amplitude on transmission line

3. Designed global clock distribution scheme with the proposed active inductor loading to minimize skew, jitter and power consumption
1.3 Outline of Thesis

This thesis is organized as follows: Chapter 2 reviews literature of alternative clock distribution technique and topologies, lists figure-of-merit and recent trends in designing global clock. Chapter 3 first explains the transmission line theory basis and the RLGC model. then presents the extracted RLGC matrices using Cadence transmission line model generator. Chapter 4 focuses on how to generate standing wave reliably on lossy transmission lines. A improved CMOS cross-coupled pair is proposed to compensate the on-chip interconnect loss. A 10GHz standing-wave clock distribution design example with cross-coupled pair compensation is presented. To overcome the spatial variation in the clock amplitude, Chapter 5 presents the use of active inductor as load on both ends of the microstrip. Several improved CMOS active inductor circuit schemes have been proposed, including singled-ended and differential active inductors. Chapter 6 reports the entire global clock distribution network, an improved X-tree clock distribution scheme is proposed with detailed simulation results. Chapter 7 summarizes work presented in this thesis and points out potential areas for further studies.
2 Clock Distribution System

2.1 Figure of Merit

Most of the digital systems in nowadays, e.g. high-performance microprocessor, employ synchronous clocking design. High-speed clocks exceeding GHz are required to globally distributed across the chip. The clock distribution network are mainly characterized by two aspects: time uncertainty and power consumption. Clock skew (spatial variation of clock arrival time) and jitter (clock period from nominal) are two major concern of time uncertainty. Power usually categorizes into static power and dynamic power.

2.1.1 Clock Skew

Clock skew is the time difference between arrival at different positions, as shown in Figure 1. For synchronous design, it means arrival variation in the clock pin of the flip-flops. Clock skew is generally caused by the following:

- mismatch of interconnect length (wire delay)
- buffers on the clock path
- loading variations
- PVT variations

Clock skew can be corrected by carefully pre-layout design and post-layout simulation. Buffering, symmetric structure and redundant connections
are commonly used to minimize clock skew [22–26].

2.1.2 Clock Jitter

Jitter is defined as period variations at different clock cycles on a clock node, as shown as in Figure 2. There are two types of jitter: deterministic and random. Deterministic jitter is caused by interference signals such as power supply noise, gate switching etc. Random jitter is usually caused by PVT variations and can be characterized statistically.

In the past, jitter was dominated by the clock source, which is usually made of an on-chip phase-locked loop (PLL) that multiplies the off-chip clock reference to the core clock frequency. However, PLL jitter has been scaled well with technology while the jitter in the clock distribution has not. As a result, the dominant source of clock jitter for today’s high-performance microprocessors is the clock distribution.
2.1.3 Power Consumption

Power consumption can be categorized into static power and dynamic power. Static power consumption refers to the power when there is no circuit activity, e.g. the leakage from transistors. Dynamic power is power consumed while the inputs are active, e.g. power consumed when charging and discharging a capacitive output load. Dynamic power is the main contribution to the overall system power. But as technology scaled to nano meter design, static power is playing a more and more important role.

The dynamic power $P_{\text{dyn}}$ of digital systems can be expressed as

$$P_{\text{dyn}} = \alpha C_L V^2 f$$

(1)

where $\alpha$ is switching rate, $C_L$ is load capacitance, $V$ is the voltage swing and $f$ is the clock frequency. For a clock distribution network, the major
power consumption comes from the loading on the leaf of the clock network, which usually is capacitance of the flip-flop clock pins, the loading from the buffer and wiring capacitance. For modern high speed design, the power consumption of the clock distribution network can be around 30% to 50% \cite{1} and in extreme cases can be up to 70\% \cite{2} of the entire digital system.

2.2 Conventional Clock Distribution

Conventional clock distribution uses a hierarchical approach to deliver the clock signal across the entire chip. The global clock distribution network takes the clock reference and drives the local distribution network with low skew clocks copies. Typically the global clock topologies can be tree, grid or hybrid of tree and grid. The local distribution network would contain buffers to match the loading and equalize the delay from the clock source to the clock pin of the flip-flops.

2.2.1 Tree

Figure 3 shows some example of global clock distribution using tree topology, including binary tree and H-tree scheme. The main idea is to balance the delays of various path by splitting the clock source symmetrically at each stage. Therefore, multiple clock copies are created. H-tree clock distribution (Figure 3b) is constructed from perpendicular line segments and the repeating pattern resembles the letter ”H”. It requires relatively regular floorplan. In contrast, binary tree (Figure 3a) has less stringent floorplan
requirement. The buffer along the tree can be placed closely. Both H-tree and binary tree provide the flexibility to individually tune the skew along each path through sizing of the buffers. Additionally, fine-grained clock gating can be easily achieved by inserting clock gating cells on individual clock branches. However, due to the various number of flip-flops to be driven at each clock nodes, it is difficult to balance the path delays and gain closed to zero skews, especially under various PVT from on chip variation (OCV).

Figure 3: Clock tree for global clock distribution

2.2.2 Grid

Clock grid is popular in high performance high speed microprocessors using custom methodologies, as shown in Figure 4. In the clock grid architec-
ture, multiple copies of the root clock signal are injected into various nodes a metal mesh. The metal mesh provides paths down to the clock sinks via its regular mesh routing structure. Due to the cross-linking between the clock nodes, clock grid is less susceptible to loading variations and has better control on skew and jitter. On the other hand, clock grids has large capacitive loads, and hence higher power dissipation and wire usage.

Figure 4: Clock grid for global clock distribution

2.2.3 Hybrid

As addressed before, clock grid provides a load-independent method of clock delivering but takes more wiring and routing resources, which results in high power and area overhead. Clock tree, on the contrary, has relatively low routing overhead but are sensitive to PVT OCV and hard to balance between clock nodes. Hybrid clock scheme is a mixture of clock grid and clock tree to take benefits from each scheme. Various hybrid clock scheme has been proposed. Figure 5a shows an example when a mesh is used to
distribute clocks from a global clock source and the local trees distribute the clock to local regions. Figure 5b is a clock scheme that trees feed the global clock source to local mesh at each leaf. Other hybrid mesh-style structures are also possible.

Figure 5: Hybrid clock scheme for global clock distribution [27]

Many commercial micro-processors employed the hybrid clock distribution approach [38–45]. The designs consist of multilevel trees and grids and achieve clock skew in ps range. It also reports the clock distribution network contributed to a significant amount of the total power [38–45].

2.3 Resonant Clock Distribution

As clock frequency continues to increase and is approaching 10GHz, more and more buffer levels are inserted into conventional clock distribution to achieve the desired edge rates and cover the increasing die size. This, in turn, results in higher latency relative to the clock period and higher skew and jitter.
In recent years, significant research has been focused on improving the existing clock distribution architecture to allow further process scaling and reduction of clock period. Additionally, alternative topologies, such as traveling-wave distribution, standing-wave distribution and coupled arrays of oscillators, are proposed to replace the conventional clock distribution architecture. All these new schemes utilize the resonant behavior on the transmission line and can be classified as resonant clock distribution. This section gives a brief summary of the research in these areas and leads to the proposed global clock distribution scheme in the following chapter.

2.3.1 Traveling Wave Resonant

Traveling wave resonant utilizes transmission line to convey the global clock source by means of traveling wave. One form of traveling wave resonant is a rotary clock that an inner and outer transmission line form a closed parallel loop [10, 12]. If there is no loss on transmission line, the signal applied to the loop could travel indefinitely.

For rotary clock, the swing of all positions are the same while the phase varies with position. Since clock sinks may be attached to different positions on the loop, the position-dependent phase variation would bring extra work in clock timing and synchronization. For lossy transmission line, negative impedance devices are needed to overcome the signal attenuation and maintain traveling wave along the transmission line.
2.3.2 Standing Wave Resonant

A standing wave is formed when two harmonic waves of the same frequency and amplitude propagate in opposite directions. A simple method to generate a standing wave is to send a wave signal along a transmission line and reflect it back at the end of the line. Figure 7 shows the example implementation.

In standing wave clocks, the phases of all points are the same which achieves very low clock skews. Transmission line loss causes amplitude attenuation along the line. Therefore, amplitude of the reflected wave does not match incident wave, which results in residual traveling wave and causes clock skew. Distributed negative impedance devices are introduced to compensate for signal attenuation [4]. Another practical issue of standing wave
2.3.3 LC Tank Resonant

LC tank resonant clock is extension of conventional clock scheme with additional spiral inductors at leaf nodes. Ideally, LC tank resonant clock has constant phase, constant magnitude and topology similar to non-resonant...
clock described previously. Compared to standing wave and rotary clock, it has less restrictions on physical implementation, i.e. no requirement on a fully symmetric and balanced structure.

Figure 8: Resonant LC tank clock network, with H-tree and grid, inductor, decoupling cap and gain elements are attached to the leaf of the tree [17]

Figure 8 shows an LC tank and H-tree combined clock architecture with inductors, decoupling capacitors and negative transconductance. H-tree is used as the global clock distribution network. Spiral inductors are connected at certain branches of the H-tree in series with the decoupling capacitors. The decoupling capacitors are sufficiently large that the spiral inductor and the decoupling capacitor forms a serial LC tank. When the clock frequency equals to the LC tank resonant frequency, the LC tank is in resonant mode and the energy is recycling inside the LC tank and results in large power savings.
2.3.4 Oscillator Array

Another resonant clock distribution scheme is oscillator array, where distributed multiple clock generators are used instead of a single root clock source. This scheme reduces the skews from clock generator to the load. The distributed oscillator arrays are coupled. Its phase is averaged between oscillators and this would reduce clock skew and jitter.

![Distributed phase locked loops (PLLs) array](image)

Figure 9: Distributed phase locked loops (PLLs) array

Two forms of oscillator array are proposed: distributed phase locked loops (PLLs) [28–31] and distributed VCO arrays [32–36]. In distributed PLL array, the loops are duplicated to each clocks, as shown in Figure 9. Therefore all the oscillators are in phase. The clock skew is mostly caused by mismatch of buffers and phase detectors. Jitter also gets reduced because all PLLs are localized. However, distributed PLL array is expensive to implement and has relatively high power consumption.
Distributed VCO clock array is similar to distributed PLL clock array, except that a single control loop is used for multiple VCOs. Figure 10 shows one design example from [32]. A single set of phase detector, charge pump and low pass filter are used in the loop. All the VCOs are coupled together to oscillate at the same frequency and reduce jitter and skew. Clearly the solution is more cost effective compared to distributed PLL array scheme. In reality, the routing and device mismatch will inevitably worsen the clock skew and jitter. An test-chip of 264 17-stage ring oscillators at 0.25\(\mu\)m CMOS technology is reported in [32]. The measured jitter between oscillator 1 and 65 is 17ps at 434MHz.
3 Transmission Line and Modeling

3.1 Background

In low frequency clock distribution, the interconnect wiring is usually analyzed as simple lumped $RC$ or $RLC$ models and provides a convenient way for delay calculation. As clock frequency keeps increasing and the wire length increases due to bigger die size, the lumped $RC/RLC$ model is no longer sufficient to provide enough accuracy and hence distributed $RLC$ mode like transmission line model needs to be employed (Figure 11).

![Figure 11: Transmission line RLGC model](image)

Assuming for transmission line, $R$ is series resistance per unit length in $\Omega/m$, $L$ is series inductance per unit length in $H/m$, $G$ is shunt conductance per unit length in $S/m$ and $C$ is shunt capacitance per unit length in $F/m$, from the well-known Telegrapher Equation [70],

\[
\frac{\partial v(z,t)}{\partial z} = -(R + j\omega L)i(z,t) \quad (2)
\]

\[
\frac{\partial i(z,t)}{\partial z} = -(G + j\omega C)v(z,t) \quad (3)
\]

For calculation convenience, $v(z,t)$ and $i(z,t)$ can be replaced by its
phasor version $V(z)$ and $I(z)$. Define $\gamma, \alpha, \beta$ as propagation constant, loss constant and phase constant respectively,

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

There are,

$$\frac{d^2V(z)}{dz^2} - \gamma^2V(z) = 0$$
$$\frac{d^2I(z)}{dz^2} - \gamma^2I(z) = 0$$

The voltage and current on the transmission line can be expressed as two waves travel superimposed in opposite direction, while the forward phasor voltage $V_0^+$ and reverse phasor voltage $V_0^-$ depend on boundary conditions and the initial condition.

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}$$
$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}$$

The characteristic impedance of the transmission line $Z_0$ is defined as the impedance of the forward phasor voltage over its current, or the reverse phasor voltage over its current,

$$Z_0 = \frac{V_0^+}{I_0^+} = -\frac{V_0^-}{I_0^-} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$
If the line is lossless, \( \alpha = R = G = 0 \), and we have

\[
\gamma = j\beta = j\omega\sqrt{LC} \quad (10)
\]

\[
Z_0 = \sqrt{\frac{L}{C}} \quad (11)
\]

In case the line loss is small enough that satisfies \( R \ll \omega L, G \ll \omega C \), then, \( RG \ll \omega^2 LC \), and Equation 16 can be simplified to

\[
\gamma \approx j\omega\sqrt{LC} \sqrt{1 - j\left(\frac{R}{\omega L} + \frac{G}{\omega C}\right)} \quad (12)
\]

Furthermore, expand Equation 12 with Taylor series using \( \sqrt{1+x} \approx 1 + x/2 + ... \), we get,

\[
\gamma \approx j\omega\sqrt{LC} \left[1 - \frac{j}{2}\left(\frac{R}{\omega L} + \frac{G}{\omega C}\right)\right] = \alpha + j\beta \quad (13)
\]

\[
\alpha \approx \frac{1}{2}\left(R\sqrt{\frac{C}{L}} + G\sqrt{\frac{L}{C}}\right) = \frac{R}{2Z_0} + \frac{GZ_0}{2} \quad (14)
\]

\[
\beta \approx \omega\sqrt{LC} \quad (15)
\]

\[
\lambda = \frac{2\pi}{\beta} = \frac{1}{f\sqrt{LC}} \quad (16)
\]

Now assume the infinite length transmission line is terminated at one end by a \( Z_L \) loading, as shown in Figure 12. In this case, the forward wave with voltage of \( V_0^+ \) got reflected at the right end of the transmission line. The reflected wave is with voltage of \( V_0^- \) and subjected to the constraint that it needs to satisfy Ohm’s law on the lumped component \( Z_L \). It can be derived
that for lossless transmission line,

\[
V(z) = V_0^+(e^{-j\beta z} + \Gamma e^{j\beta z})
\]  
(17)

\[
I(z) = \frac{V_0^+}{Z_0}(e^{-j\beta z} - \Gamma e^{j\beta z})
\]  
(18)

where \( \Gamma \) is the voltage reflection coefficient

\[
\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0}
\]  
(19)

There are three special cases of line terminations where the reflected wave has the same amplitude as the forward wave,

- Short circuit, \( Z_L = 0 \), \( \Gamma = -1 \)
- Open circuit, \( Z_L = \infty \), \( \Gamma = 1 \)
- Reactance load, \( Z_L = j\omega L \), \( |\Gamma| = 1 \)
Let $\Gamma = e^{j\theta}$, then

$$V(z) = V_0^+ (e^{-j\beta z} + \Gamma e^{j\beta z})$$

$$= V_0^+ (e^{-j\beta z} + e^{j\theta} e^{j\beta z})$$

$$= V_0^+ e^{j\theta/2} 2\cos(\beta z + \theta/2) \quad (20)$$

Clearly, for $|\Gamma| = 1$, standing wave is formed with its amplitude depends on the position, $|V_0^+|\cos(\beta z + \theta/2)$. As an example, for the short circuit, the voltage and current becomes

$$V(z) = V_0^+ (e^{-j\beta z} - e^{j\beta z}) = -2j V_0^+ \sin\beta z \quad (21)$$

$$I(z) = V_0^+ (e^{-j\beta z} + e^{j\beta z})/Z_o = 2V_0^+ \cos\beta z/Z_o \quad (22)$$

The voltage along the transmission line has the same phase with its amplitude varies based on its position ($\sin\beta z$). Standing wave is formed along the line.

For loossy transmission line, the forward and reflected wave can be expressed as,

$$V(z) = V_0^+ (e^{-\gamma z} + \Gamma e^{\gamma z}) \quad (23)$$

$$I(z) = \frac{V_0^+}{Z_o} (e^{-\gamma z} - \Gamma e^{\gamma z}) \quad (24)$$
Take the short end transmission line as an example, the voltage becomes,

\[ V(z) = V_0^+(e^{-\gamma z} - e^{\gamma z}) \]

\[ = V_0^+(e^{-\alpha z - \beta z} - e^{\alpha z + \beta z}) \]

\[ = V_0^+e^{-\alpha z}(e^{-j\beta z} + e^{j\beta z}) - V_0^+(e^{\alpha z} + e^{-\alpha z})e^{j\beta z} \]  

\[ = V_0^+2e^{-\alpha z}\cos(\beta z) - V_0^+(e^{\alpha z} + e^{-\alpha z})e^{j\beta z} \]  

From Equation 26, the first part represents a standing wave attenuated with amplitude \(2e^{-\alpha z}\cos(\beta z)\), the second part is a traveling wave with amplitude of \((e^{\alpha z} + e^{-\alpha z})\) and phase \(\beta z\). Traveling wave does not have uniform phase across the transmission line. As a result, skew is introduced. To reduce the traveling wave, the loss constant \(\alpha\) needs to be minimized. To demonstrate the effect of the line loss, modeling and simulation of lossless and lossy transmission line with \(\lambda\) length is run. Assume the lossy transmission line has attenuation of 2dB on \(\lambda\) length. Figure 13a shows the waveform from 12 evenly divided sample positions on a lossless transmission line. All the waveforms are with the same phases and its amplitude depends on position. Figure 13b shows the waveform from 12 evenly divided sample positions on a lossy transmission line. Clearly all the waveforms are attenuated and not line up any more and large skew is observed.
Coupled microstrip lines contain two strips, a substrate and an insulating layer in between. This thesis is using TSMC 180nm [48] and 28nm [49] technology for micro-strip lines. Figure 14 shows the cross section of metal layers and the electric properties of the 28nm process. The coupled strips are made up by the top metal layer in case for low resistance, thus low loss. The substrate of this research is made up by M2, which gives a height if insulating layer $4.28 \mu m$. A more precise result comes from using an electromagnetic (EM) simulator. Recently, a simple LMG parameter generator has been developed and embedded in the most recent version of Cadence Virtuoso, where people can easily reach for simple geometric transmission line RLGC values. Table 1 lists geometry and per unit length transmission line RLGC parameters through Cadence LMG generator.
Table 1: Design parameters of a coupled microstrip transmission line

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line width ($\mu m$)</td>
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</tr>
<tr>
<td>Line space ($\mu m$)</td>
<td>14</td>
</tr>
<tr>
<td>Line height ($\mu m$)</td>
<td>2.8</td>
</tr>
<tr>
<td>Insulating layer height ($\mu m$)</td>
<td>4.28</td>
</tr>
<tr>
<td>$R$($\Omega/mm$)</td>
<td>7.56</td>
</tr>
<tr>
<td>$L$($nH/mm$)</td>
<td>215.5</td>
</tr>
<tr>
<td>$G$($mS/mm$)</td>
<td>0</td>
</tr>
<tr>
<td>$C$($fF/mm$)</td>
<td>211</td>
</tr>
</tbody>
</table>
4 Standing Wave Clock Distribution on Lossy Transmission Line

4.1 Introduction

As mentioned in previous chapters, one of the key issue in generating standing wave on transmission line is to ensure the incident wave and reflected wave have the same amplitude. Otherwise residual traveling wave is formed and will impact on clock skew. The unequal amplitude of incident wave and reflected wave are mostly due to transmission line loss. According to [25], CPW with 5-10 metal layers fabricated in an emulated silicon CMOS technologies has the lowest reported wire loss to 0.14 dB/mm at 10GHz. Consider a 15mm wavelength, the loss is normalized as 2.1 dB/λ, corresponding to a skew of 7% clock cycle. Therefore, for design with large die size and high frequency, loss compensation is needed. One approach is to use distributed negative resistances for the compensation.

This chapter first summarizes the existing negative resistive circuits, then presents an alternative voltage controlled cross-coupled pair design, which compensates the wire loss in an adjustable approach. Design example of an improved X-tree clock topology with 10GHz and cross-coupled pair compensation is presented. To overcome the position dependent standing wave output issue, standing wave clock distribution on transmission line with passive loading is discussed.
4.2 Negative Resistance Circuit

4.2.1 Literature Reviews

Various types of negative resistance circuits have been used in transmission loss compensation. In [37], common-gate FETs were distributed along the transmission lines with a broadband negative resistance. In [10], cross-coupled inverters were used as negative resistance. But the highly nonlinear digital inverters tend to cause distortion when working with large signal swing. Additionally, it is hard to dynamically control the negative resistance except adjusting the supply voltage. In [4], cross-coupled pair (CCP) is used to generate a differential negative resistance for the transmission line loss.

A simple cross-coupled pair is shown in Figure 15(a). The circuit offers \(-g_m/2\) negative conductance, where \(g_m\) is the transconductance of the...
transistor. Furthermore, it allows tuning of the negative resistance through control of the current source.

Figure 15(b) is used to further increase the negative resistance as it consists a PMOS cross-coupled pair and an NMOS cross-coupled pair. By carefully designed W/L ratio, negative resistance can be doubled compared to Figure 15(a). However, this structure can operate at lower frequency since PMOS devices have lower $\omega_T$ than NMOS devices.

To solve this, Figure 15(c) is introduced. It composes of NMOS cross-coupled pair and a pair of diode-connected PMOS pair with a large resistor as load. The bias current $I_1$ controls $g_m$ of the devices. The load sets the common mode voltage at the terminals to be one diode-drop from supply voltage while isolate the gate capacitance from the terminals at high frequencies [4]. However, the circuit requires large resistors, which cost lots of area and hard to be designed with CMOS process technology.

Figure 15(d) is another option to induce negative resistance. It makes up of a standard NMOS cross-coupled pair with a pair of PMOS diode load. The PMOS is biased by a separate biasing voltage $V_{bias}$, this eliminate the requirement of large resistors between gate and drain of PMOS transistors, thus saving the chip area. The disadvantage is, this structure sets up the common-mode voltage by the drain-to-source resistance of the PMOS load and the drain current of NMOS transistors, which may varies a lot with the PVT variations.
4.2.2 Modified Negative Resistance Circuit

Figure 16 introduces a modified CCP structure. It is formed by standard NMOS and PMOS cross-coupled pairs and a pair of diode-connected PMOS transistors. The negative resistance can be controlled by biasing voltage $V_B$.

![Figure 16: Modified CMOS negative resistance](image)

The small signal model is shown in Figure 17.

Assume $M_1$ and $M_2$, $M_3$ and $M_6$, $M_4$ and $M_5$ match respectively, ignore the parasitic capacitance, the resistance in $V_a$ or $V_b$ can be derived as,

$$ g = -g_{m2} - g_{m4} + g_{ds2} + g_{ds4} + g_{ds3} + g_{m3} $$

$$ = -g_{m1} - g_{m5} + g_{ds1} + g_{ds5} + g_{ds6} + g_{m6} $$  \hspace{1cm} (27)

where $g_{m1} - g_{m6}$ are the transconductance of $M_1$ to $M_6$ respectively.
Figure 17: Small signal model for the proposed CMOS negative resistance

Define the voltage between $V_a$ and $V_b$ as $V_{out}$

$$V_{out} = V_a - V_b$$  \hspace{1cm} (28)

And the corresponding output resistance from the circuit is given by

$$R_{out} = \frac{V_{out}}{I_{out}}$$

$$= \frac{2}{-g_{m2} - g_{m4} + g_{ds2} + g_{ds4} + g_{ds3} + g_{m3}}$$  \hspace{1cm} (29)

$$\approx -\frac{2}{g_{m2} + g_{m4} - g_{m3}}$$  \hspace{1cm} (30)

The negative resistance can be tuned by adjusting $V_B$ and the biasing current source $I_1$. 

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4.3 Standing Wave Clocking with Short Ended Load

As mentioned previously, a short ended transmission line with multiple quarter wave length can generate standing wave clocks. Figure 18 shows the schematic of a single standing wave oscillator which consists short ended coupled microstrip lines and voltage controlled cross-coupled pairs.

Figure 18: Standing wave oscillator with 5 cross-coupled pairs

The transmission line is a microstrip line using TSMC 0.18µm CMOS technology. Metal 6, the top metal layer, is used as the coupled strips. Metal 4 is used for conducting layer at the bottom of the interconnect. Dielectric layers between metal 6 and metal 4 are used as insulating layers.

Table 2 lists parameters of standing wave oscillator shown in Figure 18. Five cross-coupled pairs are equally distributed along transmission lines. The
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line width</td>
<td>4 µm</td>
</tr>
<tr>
<td>Line space</td>
<td>14 µm</td>
</tr>
<tr>
<td>Line height</td>
<td>2.34 µm</td>
</tr>
<tr>
<td>Insulating layer height</td>
<td>3.5 µm</td>
</tr>
<tr>
<td>SWO length $l$</td>
<td>2500 µm</td>
</tr>
<tr>
<td>$R(\Omega/mm)$</td>
<td>3.95</td>
</tr>
<tr>
<td>$L(\mu H/mm)$</td>
<td>207</td>
</tr>
<tr>
<td>$C(fF/mm)$</td>
<td>184</td>
</tr>
<tr>
<td>$G(mS/mm)$</td>
<td>0</td>
</tr>
<tr>
<td>$V_{cc}$</td>
<td>0.8 V</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>1.8 V</td>
</tr>
<tr>
<td>$(W/L)_p$</td>
<td>4µm/0.18µm</td>
</tr>
<tr>
<td>$(W/L)_n$</td>
<td>2µm/0.18µm</td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td>5 mA</td>
</tr>
<tr>
<td>$g_d$</td>
<td>1.25 mS/ccp</td>
</tr>
<tr>
<td>$c_d$</td>
<td>17 fF/ccp</td>
</tr>
</tbody>
</table>

Table 2: Design parameters of SWO with 5 cross-coupled pairs

Loss constant $\alpha$ and phase constant $\beta$ can be expressed as:

$$
\alpha \approx \frac{1}{2} \left( R \sqrt{\frac{C + C_d}{L}} + (G - G_d) \sqrt{\frac{L}{C + C_d}} \right) \\
= \frac{R}{2Z_0} + \frac{(G - G_d)Z_0}{2} \\
(31)
$$

$$
\beta \approx \omega \sqrt{L(C + C_d)} \\
(32)
$$

To make sure the transmission line is a low loss line, loss constant $\alpha < 0$ should be guaranteed, which gives

$$
\frac{R}{2Z_0} - \frac{Z_0(G - G_d)}{2} < 0 \\
(33)
$$
that is

\[ G_d > \frac{R(C + C_d)}{L} \] (34)

For a given transmission line, RLCG values are fixed, as listed in table 2. It can be derived \( G_d \gtrsim 4mS \), which is \( g_d \gtrsim 0.8mS/ccp \). For the cross-coupled pair structure, the NMOS and PMOS transistor size is \((W/L)_n = 2\mu m/0.18\mu m\), \((W/L)_p = 4\mu m/0.18\mu m\) respectively. Then

\[
\begin{align*}
g_{m8} &= 975\mu S \\
g_{m5} &= 1.83mS \\
g_{m1} &= 1.74mS \\
g_{d1} &= g_{m5} - g_{m8} \\
g_{d2} &\approx g_{m1}/2 \\
g_d &= g_{d1} + g_{d2} \approx 1.25mS/ccp
\end{align*}
\]

Transient simulation result is shown in Figure 19. The diagram plots the time-domain waveform from the five positions evenly distributed across the transmission line. Only four clock cycles are plotted for brevity. Clearly all the waveform are line up together with almost no clock skew. The amplitude is varied by its position and follows the sinusoid amplitude distribution. Standing wave is formed in this case.

A complete clock distribution network based on X-tree structure with
the proposed cross-couple pair compensation is also designed and simulated. Figure 20(a) shows the detailed clock tree structure. All the ends of the branches are short ended. CMOS cross-coupled pairs are evenly spaced to compensate for the transmission loss. The clock distribution network is built with coupled microstrip lines using metal 6 and metal 4 layers of TSMC 0.18µm technology. Details design parameters are listed in Table 3.

Figure 21 shows the output voltages of different nodes, the amplitude of the output signal is from 64 mV to 700mV. The clock distribution network consumes an average power of 195 mW.

Figure 22 is the eye diagram of clock skew from clock node next to the shorted end. The skew is about 0.4477 ps.
Figure 20: Standing wave clock distribution with short ended load and CCP compensation

Figure 21: Output voltages of various clock nodes
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line width</td>
<td>4 $\mu$m</td>
</tr>
<tr>
<td>Line space</td>
<td>14 $\mu$m</td>
</tr>
<tr>
<td>Line height</td>
<td>2.34 $\mu$m</td>
</tr>
<tr>
<td>Insulating layer height</td>
<td>3.5 $\mu$m</td>
</tr>
<tr>
<td>Effective dielectric constant</td>
<td>3.7</td>
</tr>
<tr>
<td>Network dimensions</td>
<td>$7.5 \times 7.5mm^2$</td>
</tr>
<tr>
<td>R</td>
<td>3.95 $\Omega/mm$</td>
</tr>
<tr>
<td>L</td>
<td>207 $pF/mm$</td>
</tr>
<tr>
<td>C</td>
<td>184 $fF/mm$</td>
</tr>
<tr>
<td>G</td>
<td>0 $mS/mm$</td>
</tr>
<tr>
<td>$V_{cc}$</td>
<td>0.9 V</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>1.8 V</td>
</tr>
<tr>
<td>$(W/L)_p$</td>
<td>2$\mu$m/0.18$\mu$m</td>
</tr>
<tr>
<td>$(W/L)_n$</td>
<td>2$\mu$m/0.18$\mu$m</td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td>1 mA</td>
</tr>
<tr>
<td>$g_d(mS/ccp)$</td>
<td>1.25</td>
</tr>
<tr>
<td>$c_d(fF/ccp)$</td>
<td>17</td>
</tr>
</tbody>
</table>

Table 3: Design parameters of the short ended clock distribution in Figure 20

Figure 22: Eye-diagram of the clock node next to the short end
4.4 Passive Inductor Loading

In conventional standing-wave clock distribution scheme, the output amplitude varies with its position in the transmission line and becomes zero at the end of the line. To overcome this issue, inductive loading is proposed [7–9]. The idea is to use inductor as termination to maintain the reflection with the same phase/amplitude at the position accordingly, while effectively shorten the transmission line. Figure 23 shows both short-ended loading and inductive loading transmission line for standing wave resonance. Assume \( l \) is the length of short-ended transmission line length, \( l' \) is the length of inductive loaded transmission line.

\[
\Gamma = \frac{-1}{\frac{j\omega L - Z_0}{j\omega L + Z_0}}
\]

Figure 23: Standing wave oscillator on short-ended and inductive loading transmission line
At the inductor loading point, the reflection coefficient $\Gamma$ can be expressed as:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{j\omega L - Z_0}{j\omega L + Z_0}$$

$$\angle \Gamma = \pi - 2\tan^{-1}\frac{\omega L}{Z_0}$$

Equation 36 denotes incident wave and reflected wave differs $\angle \Gamma$ in phase at the inductor loading point, but with same amplitude. Given the same incident wave, the phase of the reflected wave should be equal in both cases as in Figure 23

$$\pi - 2\beta\left(\frac{l - l'}{2}\right) = \angle \Gamma$$

(37)

Where $\beta$ is phase velocity, which can be expressed as $2\pi/\lambda$ ($\lambda$ is electrical wave length). From Equation 37, assume $l = n\lambda/4$, $n=1,2,3,4...$, length $l'$ can be expressed in term of length $l$ as:

$$l' = \frac{n\lambda}{4} - \frac{\lambda}{\pi}\tan^{-1}\frac{\omega L}{Z_0}$$

(38)

The standing wave amplitude at the inductor load point is the same as the $l'$ position in short-ended transmission line. Therefore, by controlling the length and inductance, a larger voltage swing is obtained at the expense of a shorter transmission line. Figure 24 shows a comparison of the standing wave amplitude on a short ended and an inductive loading transmission line.
The transmission line is set to half wave-length in the short ended case for illustration. Obviously the inductive loading transmission line removes the low swing region in the short ended transmission line. The amplitude variation can be controlled by selecting the length of the line and the inductor loading accordingly. The larger the inductor, the shorter the transmission line and more uniform of the amplitude.

![Standing wave amplitude on short ended and inductive loading transmission line](image)

Figure 24: Standing wave amplitude on short ended and inductive loading transmission line

Figure 25 shows a standing wave oscillator structure with passive inductive loading. The schematic is almost the same as structure shown in Figure 18, except the former one has inductive loading, the latter has shorted ends. As described before, both can generate standing wave if satisfied certain conditions. The advantage of using inductive loading is the output signal amplitude gets increased. On the other hand, the length of the transmission line needs to be shrink in order to achieve the same resonant frequency due to the inductance in the load point.
In this case, \((W/L)_n = (W/L)_p = 2\mu m/0.18\mu m\), and \(V_{cc} = 0.9V\). Figure 26 shows the simulation results of output voltages at every node that has a cross-coupled pair. The furthest point of the swo is the loading point, which is zero at the short ended schematic, and is 0.5V with inductive load.

Figure 27 shows a X-tree global clock distribution using on-chip spiral inductors loading. The loaded inductor is 904 \(pH\). The dimensions of the inductor are 6\(\mu m\) for inductor width, 2\(\mu m\) for inductor space, 89\(\mu m\) for inner radius and 1.25 turns. This increases the output amplitude of the resonant clock, the disadvantages of this loading are: first, the available clock network sizes are shorten; Second, the chip inductor has lower Q factors and occupies large areas.

NMOS cross-coupled pairs are used in this typology to compensate the transmission loss. Figure 28 shows the output voltages from the clock signal.
Figure 26: Transient waveform of various nodes on SWO with inductive loading

Figure 27: Standing wave clock distribution with inductive load and cross-coupled pair
to the very far end of an X-tree branch, and the voltage amplitude is 1.19 V at the end of the X-tree branch. The entire clock distribution network consumes an average power of 51.75 mW.

Figure 28: Output voltages from node closed to the inductor loading

Monte Carlo simulation results are listed below in Table 4. In the simulation, supply voltage varies from 1.1V to 1.3V, biasing current of the cross-coupled pairs varies from 1.1mA to 1.9mA and the process corners includes FF, MC, SS and TT. Since there is no PMOS transistors in the whole clock networking schematic, FS and SF corners are ignored. Figure 29 shows the clock delays between the clock output nodes and the clock source. The clock skew for inductive loading clock distribution networking is between -0.1ps and +0.1ps. Figure 30 is the eye-diagram for the standing wave clock distribution with passive inductor loading, which indicates clock jitters of 1.8574 ps together for all corners.
<table>
<thead>
<tr>
<th>corners</th>
<th>FF</th>
<th>MC</th>
<th>TT</th>
<th>SS</th>
</tr>
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<tbody>
<tr>
<td>skew (fs)</td>
<td>±0.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>jitter (fs)</td>
<td>768.31</td>
<td>999.18</td>
<td>761.29</td>
<td>746.24</td>
</tr>
<tr>
<td>power (mW)</td>
<td>48</td>
<td>56</td>
<td>54</td>
<td>60</td>
</tr>
</tbody>
</table>

Table 4: Monte Carlo simulation results for passive inductor loading clock distribution

Figure 29: Skew for the standing wave clock distribution with passive inductor loading

Figure 30: Jitter for the standing wave clock distribution with passive inductor loading
5 Active Inductor Loading for Transmission Line

5.1 Introduction

As mentioned in Chapter 4, standing wave clock scheme has uniform phase across the entire clock network, which yields almost zero skew in global clock distribution. But its voltage and current vary spatially. Furthermore, voltage swing at the loading point (the end of a transmission line) usually reduces to zero.

To overcome the position-dependent amplitude variation and low output swing issue, passive inductive loading is proposed [7–9], where uniform phase and almost uniform amplitude standing wave is realized. The detailed analysis of standing wave clock distribution using inductor loading is addressed in Chapter 4. Spiral inductor is usually used as lumped passive inductor in CMOS process. Drawbacks of implement spiral inductor are: fist, it takes up large chip area, second, it has low Q value, below 20 for 28nm CMOS technology (By using special design, such as using much wider winding, single turn, it may reach up to 40, but then, it will consume even more chip area). In this chapter, we extend the idea of inductive loading further by applying CMOS active inductor instead of its passive counterpart.

Compare with spiral inductors, first, CMOS active inductor is made up by MOSFET, thus is area saving, second, it is inductively tunable, by tuning
biasing voltage/current and device parameter, inductance can be tuned. For low power design, dynamic frequency scaling is widely used. By applying inductance tunable active inductor, which fits wider frequency range will benefit from the above mentioned low power design. Third, active inductor can achieve high quality factor, mostly more than 100. Moreover, active inductor is composed by MOSFET, which makes it compatible with CMOS technology process. Due to these advantages, CMOS active inductors are applied with lots of RF components nowadays.

For the rest of the chapter, we investigate both single-ended and differential active inductor design. Three active inductor schemes are proposed: single-ended cascoded, differential active inductor with cross-coupled pair compensation and differential cascoded active inductor. All of the circuits achieve more than one hundred Q value and some tunability. The proposed schemes are employed in an improved X-tree clock distribution network to distribute low skew, low jitter clocks across the chip.

5.2 Single-Ended Active Inductor

5.2.1 General Active Inductor Structure

CMOS active inductor is constructed by gyrator-C structure, as shown in Figure 31. A gyrator-C structure is made up by two back-to-back connected OTAs. $g_{m1}$ and $g_{m2}$ are transconductance of OTA- and OTA+ respectively. OTA-, loading capacitor $C$ and OTA+ provide a $v \rightarrow i \rightarrow v \rightarrow i$ conversion.
OTA- provides 180° phase shift and the capacitor $C$ makes -90° phase shift. Both together gain a 90° phase shift between voltage and current. As a result, an active inductor is formed with the inductance of

$$L_{eq} = \frac{C}{g_{m1}g_{m2}}$$  \hspace{1cm} (39)$$

Ideal OTA with infinite input and output impedance can achieve perfect Q value. In reality, circuit implementation with single transistor amplifier suffers from low input or output impedance and affects quality factor value. Non-ideal OTA can be modeled as ideal OTA with limited output conductance and capacitance. Figure 32 shows a non-ideal (lossy) gyrator-C active inductor model. The conductance of lossy gyrator-C active inductor can be expressed as

$$Y = \frac{I_A}{V_A} = \frac{g_{m1}g_{m2}}{g_1 + sc} + sC_2 + g_2$$  \hspace{1cm} (40)$$
The RLGC parameter of lossy gyrator-C active inductor can be expressed as

\[ L = \frac{C}{g_{m1} g_{m2}} \]  
\[ R_s = \frac{g_1}{g_{m1} g_{m2}} \]  
\[ R_p = \frac{1}{g_2} \]  
\[ C_p = C_2 \]

The equivalent RLGC model is shown in Figure 33.

Unlike lossless active inductor, which performs inductive character across the entire frequency spectrum, a lossy active inductor is inductive effective only within certain frequency range, which can be determined by its poles and zeros. From the RLC equivalent circuit in Figure 33, the impedance of
the RLGC equivalent circuit is,

\[
Z(s) = \frac{1}{C_p} \frac{s + \frac{R_s}{L}}{s^2 + s\left(\frac{1}{R_p C_p} + \frac{R_s}{L}\right) + \frac{R_p + R_s}{R_p C_p L}}
\]

(45)

Therefore Z has one zero and two poles and can be expressed as,

\[
Z(s) = \frac{R_s R_p}{R_s + R_p} \frac{(1 - \frac{s}{\zeta})}{(1 - \frac{s}{p_1})(1 - \frac{s}{p_2})}
\]

(46)
where

\[ z = -\frac{R_s}{L} \]  

(47)

\[ p_1 \approx -\left(\frac{1}{R_p C_p} + \frac{R_s}{L}\right)/2 + j\sqrt{\frac{R_p + R_s}{R_p C_p L}} \]  

(48)

\[ p_2 \approx -\left(\frac{1}{R_p C_p} + \frac{R_s}{L}\right)/2 - j\sqrt{\frac{R_p + R_s}{R_p C_p L}} \]  

(49)

All the zero and poles are located in the left plane. The two poles are complex conjugate and mirrored to X-axis. When the operating frequency is close to DC, \( Z \approx \frac{R_s R_p}{R_s + R_p} \). To further analyze the impedance change along various frequency, plug in the design parameters of the lossy gyration-C active inductor, assume \( g_{m1} \gg g_1, g_{m2} \gg g_2 \), we get,

\[ z = -\frac{g_1}{C} \]  

(50)

\[ p_1 \approx -(\frac{g_1}{C} + \frac{g_2}{C_2^2})/2 + j\sqrt{\frac{g_{m1} g_{m2}}{C C_2^2}} \]  

(51)

\[ p_2 \approx -(\frac{g_1}{C} + \frac{g_2}{C_2^2})/2 - j\sqrt{\frac{g_{m1} g_{m2}}{C C_2^2}} \]  

(52)

The root locus plot is shown in Figure 34,

Typically \( g_{m1} \) and \( g_{m2} \) is comparable, \( C \) and \( C_2 \) is comparable, \( \frac{g_{m1}}{C} \gg \frac{g_{m2}}{C_2} \gg \frac{g_1}{C} \gg \frac{g_2}{C_2^2} \) and \( \sqrt{\frac{g_{m1} g_{m2}}{C C_2^2}} \gg \frac{g_1}{C} + \frac{g_2}{C_2^2} \), so \( p_1 \approx j\sqrt{\frac{g_{m1} g_{m2}}{C C_2^2}} \).
Figure 34: Root locus of the lossy gyrator-C active inductor

\[ p_2 \approx -j \sqrt{\frac{g_m g_{m2}}{C C_2}} \]

Define \( \omega_z = \frac{g_1}{C} \) as the frequency of the zero, \( \omega_p = \sqrt{\frac{g_m g_{m2}}{C C_2}} \) as the frequency on the imaginary axis of the poles (ignore its real part since it’s much smaller than its imaginary part). For \( \omega \ll \omega_z \), the phase contribution from the zero is closed to \( 0^\circ \) while contributions from the poles canceled out each other, the circuit behaves like a resistor with resistance of \( \frac{R_s R_p}{R_s + R_p} \), as shown in Figure 34a. If \( \omega_z < \omega < \omega_p \), the phase contribution from the zero is closed to \( 90^\circ \) while contributions from the poles canceled out each other, the circuit acts as an inductor of \( L = \frac{C}{g_m g_{m2}} \), as shown in Figure 34b. For \( \omega \gg \omega_p \), the phase contribution from two poles add up.
together closed to -180° and the contribution from zero is closed to 90°. The total phase closes to -90°, the circuit is capacitive, as shown in Figure 34c. The phase of the lossy gyrator-C active inductor versus frequency is plot in Figure 35.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{figure35.png}
\caption{Phase characteristics of the lossy gyrator-C active inductor}
\end{figure}

The quality factor $Q$ of an inductor can be expressed as ratio of the recycling energy versus the resistive power dissipation:

$$Q = \frac{\text{Im}(Z)}{\text{Re}(Z)}$$

$$= \left( \frac{\omega L}{R_s} \right) \frac{R_p}{R_p + R_s \left[ 1 + \left( \frac{\omega L}{R_s} \right)^2 \right]} \left[ 1 - \frac{R^2 C_p}{L} - \omega^2 L C_p \right]$$

(53)

Clearly, the more the phase of $Z(j\omega)$ approaches to 90°, the better the quality factor. When the phase of $Z$ is 90° for a particular frequency, $Q$ equals to infinity. Additional, to achieve a wide tuning range, i.e. the circuit remains inductive, $\omega_z$ and $\omega_p$ needs to be separated as much as possible.
Given that $\omega_p \approx \sqrt{\frac{g_m g_{m2}}{C C_2}}$, for single transistor amplifier, $\frac{g_m}{c}$ is usually the transit frequency of the transistor, reducing $\omega_z$ to zero is desired and $g_1$ should be minimized.

From Equation 53, $Q$ is a function of frequency $\omega$. For low frequency, $\omega L \ll R_p$ and closed to $R_s$, $Q$ will be dominated by the value of $R_s$ and can be simplified to,

$$Q \approx Q_s = \frac{\omega L}{R_s} \quad (54)$$

When frequency goes higher that $\omega L \gg R_s$, $Q$ will be dominated by the value of $R_p$ and can be simplified to,

$$Q \approx Q_p = \frac{R_p}{\omega L} \quad (55)$$

When frequency reaches sufficiently high that $1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p = 0$, i.e. $\omega \approx 1/\sqrt{LC_p}$, $Q$ becomes zero and turns to negative. The active inductor is no longer inductive and becomes capacitive.

5.2.2 Circuit Examples

Various active inductor circuits have been proposed using the gyrator-C structure [51–58]. Figure 36a is a simple active inductor with common-source, common-drain (CS-CD) gyrator-C structure by [51]. The circuit
exploits the parasitic capacitance of $M_1$ and $M_2$ and is inductive up to the $f_T$ of the transistor. As shown later, the equivalent OTA topology is slight different from the gyrator-C structure addressed before in that one end of the capacitor $C$ is connected to the output of the gyrator instead of the ground. This topology creates undesired feedback from the gyrator output and limits the Q factor that can be achieved.

Figure 36: Gyrator-C active inductor circuit examples

Figure 36b is a common-source, common-gate (CS-CG) active inductor structure proposed by [55], the bias current of $M_1$ and $M_2$ is shared and reused, thus lower the power consumption. The circuit has limited Q value due to the low output impedance of the common gate stage. Figure 36c is a single transistor active inductor proposed by [56] with minimum number of transistor. However, the circuit requires a large $R$ value to achieve high Q value. There’s many other variations existing, which is mostly derived from combinations of basic amplifiers, i.e. common-source, common-drain,
In the following, the common-source, common-drain (CS-CD) gyrator-C structure in Figure 36a is analyzed as an example to show its merit and limitations. If we only consider $g_{ds}$ and $C_{gs}$ and ignore other parasitics of the transistors, the small signal model is shown in Figure 37.

![Figure 37: Small signal model for CS-CD active inductor](image)

Admittance is expressed in Equation 56,

$$Y = sC_{gs1} + g_{m1} + g_{ds1} + g_{ds2} + \frac{g_{m1}g_{m2} + g_{ds1}(g_{m2} - g_{m1} - g_{ds1})}{sC_{gs2} + g_{ds1}}$$

(56)
All parasitic can be expressed as Equation 57.

\[
L = \frac{C_{gs2}}{g_{m1}g_{m2} + g_{ds1}(g_{m2} - g_{m1} - g_{ds1})}
\]

\[
R_s = \frac{g_{ds1}}{g_{m1}g_{m2} + g_{ds1}(g_{m2} - g_{m1} - g_{ds1})}
\]

\[
R_p = \frac{1}{g_{m1} + g_{ds1} + g_{ds2}}
\]

\[
C_p = C_{gs1}
\]

(57)

Since \( g_{m1} \gg g_{ds1} \) and \( g_{m2} \gg g_{ds2} \), Equation 57 can be simplified as:

\[
L = \frac{C_{gs2}}{g_{m1}g_{m2}}
\]

\[
R_s = \frac{g_{ds1}}{g_{m1}g_{m2}}
\]

\[
R_p = \frac{1}{g_{m1}}
\]

\[
C_p = C_{gs1}
\]

(58)

\( Q_p \) and \( Q_s \) are:

\[
Q_s \approx \frac{\omega L}{R_s} = \frac{\omega C_{gs2}}{g_{ds1}} \approx \frac{\omega}{f_T} \frac{g_{m2}}{g_{ds1}}
\]

(59)

\[
Q_p \approx \frac{R_p}{\omega L} = \frac{g_{m2}}{\omega C_{gs2}} = \frac{f_T}{\omega}
\]

(60)

\( Q \) is determined by \( Q_p \) or \( Q_s \), whichever is dominant. To maximize \( Q_s \), \( R_s \) needs to be minimized. If we re-visit the circuit from an equivalent but simplified OTA model by ignoring all the parasitic, as shown in Figure 38.
Figure 38: Simplified OTA model for CS-CD active inductor

The admittance looking into node A and the equivalent RL network are:

\[
Y = g_{m1} + \frac{1}{s \frac{C_{gs2}}{g_{m1}g_{m2}}} \\
L = \frac{C_{gs2}}{g_{m1}g_{m2}} \\
R_p = \frac{1}{g_{m1}} \\
R_s = 0 \\
C_p = 0
\]  \(61\)

Compared to Figure 31, the feedback path of \(C_{gs2}\) in Figure 38 introduced a parallel conductance of \(g_{m1}\), therefore, for circuit like Figure 36a, the upper bound of \(Q\) is limited as shown in Equation (62). \(Q_p\) is limited by transit frequency \(f_T\). To increase \(Q\), \(R_p\) need to be maximized, which
requires a different circuit topology.

\[ Q = \frac{g_{m2}}{\omega C_{gs2}} = \frac{\omega_T}{\omega} \]  

(62)

### 5.2.3 Improved Single-Ended Active Inductor

Figure 39 shows an alternative design [57], \( M_2, M_3 \) and \( M_4 \) act as OTA+ while \( M_1 \) as OTA-. The equivalent OTA model is shown in Figure 31. Compared to Figure 38, the feedback from the input of OTA+ to its output by \( C_{gs2} \) is removed, a larger \( R_p \) is achieved. The small signal model is shown in Figure 40.

![Simplified schematic of Uyanik-Tarim active inductor](image)

Figure 39: Simplified schematic of Uyanik-Tarim active inductor
Figure 40: Small signal model of Uyanik-Tarim active inductor

Admittance and equivalent $L, R_s, R_p, C_p$ are listed in Equation 63,

\[
Y = sC_{gs1} + g_{ds4} + \frac{g_{m1}g_{m2}g_{m4}}{(g_{m3} + g_{ds2} + g_{ds3} + sC_{gs3} + sC_{gs4})(g_{ds1} + sC_{gs2})} \\
L = \frac{(g_{m3} + g_{ds2} + g_{ds3})C_{gs2} + (C_{gs3} + C_{gs4})g_{ds1}}{g_{m1}g_{m2}g_{m4}} \\
R_s = \frac{-\omega^2C_{gs2}(C_{gs3} + C_{gs4}) + (g_{ds2} + g_{ds3} + g_{m3})g_{ds1}}{g_{m1}g_{m2}g_{m4}} \\
R_p = \frac{1}{g_{ds4}} \\
C_p = C_{gs1} \tag{63}
\]

Q expressions are listed in Equation 64.

\[
Q_s \approx \frac{\omega L}{R_s} = \frac{\omega C_{gs2}g_{m3}}{-\omega^2C_{gs2}(C_{gs3} + C_{gs4}) + (g_{ds2} + g_{ds3} + g_{m3})g_{ds1}} \\
Q_p \approx \frac{R_p}{\omega L} = \frac{1}{g_{ds4}} \frac{g_{m1}g_{m2}g_{m4}}{g_{ms}(g_{m3} + g_{ds2} + g_{ds3})C_{gs2} + (C_{gs3} + C_{gs4})g_{ds1}} \tag{64}
\]

The circuit shown in Figure 39 can be improved to have tunable in-
ductance and $Q_s$ value by introducing capacitors connected to the gate of $M_2$ and $M_3$ respectively. Figure 41 is the designed circuit, the inductance is tuned by $C_L$, as shown in Equation (65). $Q_s$ can be tuned independently by lowering $R_s$. From Equation 67, by tuning $C_Q, C_{gs2}, C_{gs3}, C_{gs4}, g_{m3}$ and $g_{ds1}, R_s$ can reach close to zero. $Q_p$ becomes dominant in this case.

$$L = \frac{(g_{m3} + g_{ds2} + g_{ds3})(C_{gs2} + C_L) + (C_{gs3} + C_{gs4} + C_Q)g_{ds1}}{g_{m1}g_{m2}g_{m4}}$$  \hspace{1cm} (65)$$

$$Q_s \approx \frac{\omega L}{R_s} = \frac{\omega (C_{gs2} + C_L)g_{m3}}{-\omega^2 C_{gs2}(C_{gs3} + C_{gs4} + C_Q) + (g_{ds2} + g_{ds3} + g_{m3})g_{ds1}}$$  \hspace{1cm} (66)$$

$$Q_p \approx \frac{R_p}{\omega L} = \frac{1}{g_{ds4} (g_{m3} + g_{ds2} + g_{ds3})(C_{gs2} + C_L) + (C_{gs3} + C_{gs4} + C_Q)g_{ds1}}$$  \hspace{1cm} (67)$$

To verify the active inductor circuit, an active inductor of 500pH and 10GHz operating frequency is designed and simulated with TSMC 28nm
technology. The designed active inductor is intended to use as the active loading of standing wave clock distribution network. The detailed design parameters are listed in Table 5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>1.8 V</td>
</tr>
<tr>
<td>$(W/L)_1$</td>
<td>2.4μm/60nm</td>
</tr>
<tr>
<td>$(W/L)_2$</td>
<td>9.6μm/60nm</td>
</tr>
<tr>
<td>$(W/L)_{3,4}$</td>
<td>2.4μm/60nm</td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td>1.6mA</td>
</tr>
<tr>
<td>$C_L$</td>
<td>0nF</td>
</tr>
<tr>
<td>$C_Q$</td>
<td>0fF</td>
</tr>
</tbody>
</table>

Table 5: L and Q tunable CMOS active inductor design data, Figure 41

Figure 42 shows simulation results, at 10 GHz frequency, we can obtain a $\sim 500$ pH inductor with Q larger than 3700.

Figure 42: Simulation result of Uyanik-Tarim active inductor
To further improve $Q_p$, we need to increase $R_p$, i.e. $1/g_{ds4}$. The proposed circuit schematic is shown in Figure 43. $M_5$ and $M_6$ cascaded on current mirror $M_3$ and $M_4$, increasing the output resistance from $1/g_{ds4}$ to $g_{m5}/(g_{ds4}g_{ds5})$. Capacitor $C_L$ in parallel with $C_{gs2}$ to control inductance. Capacitor $C_Q$ is used to control $Q_s$.

![Figure 43: Proposed schematic of single-ended active inductor](image)

Table 6 shows the detailed design parameters at TSMC 28nm technology.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>1.8 V</td>
</tr>
<tr>
<td>$(W/L)_1$</td>
<td>2.4$\mu m$/60nm</td>
</tr>
<tr>
<td>$(W/L)_2$</td>
<td>4$\mu m$/60nm</td>
</tr>
<tr>
<td>$(W/L)_{3-6}$</td>
<td>4.8$\mu m$/60nm</td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td>1.6mA</td>
</tr>
<tr>
<td>$C_L$</td>
<td>100aF</td>
</tr>
<tr>
<td>$C_Q$</td>
<td>1.3fF</td>
</tr>
</tbody>
</table>

Table 6: Design parameters of proposed cascoded single-ended active inductor

75
Figure 44 shows the simulation result that at 10 GHz, we can obtain a $\sim 600 \, \mu H$ inductor which $Q$ is around 4630.

Figure 44: Simulation result of the proposed single-ended cascoded active inductor

5.3 Differential Active Inductor

5.3.1 Introduction

Differential active inductor compared with its single counterparts has two attractive advantages: rejection of common-mode disturbances due to differential configuration, and double of voltage swing. Conventional differential active inductor is made up of two differential OTAs or two single-ended active inductors [59–65]. Figure 45a shows the back-to-back connected differential OTA topology and Figure 45b shows the differential OTA composed
by two single-ended OTAs.

Figure 45: Differential active inductor using differential OTAs

The principle between differential active inductor is the same as single-ended active inductor addressed previously, where the back-to-back connected OTA+ and OTA- provides 180° phase shift while the parasitic capacitor offers a -90° phase shift, both together gain a 90° phase shift between voltage and current and form an active inductor. Some circuit examples are shown in Figure 46 for the above mentioned topologies.

In Figure 46a, the differential active inductor [60] is constructed by using two basic differential OTAs. Negative resistors are connected across the OTA output to cancel out the OTA output parasitic resistances and achieve better Q. A \( Q = 600 \) (at 2GHz) differential inductor is reported in [60] in 0.18um technology.

Figure 46b shows the differential active inductor based on two single-ended common-source common-gate (CS-CG) active inductor. The PMOS common-source stage (M2,M3) is cascoded to have larger output resistance.
A cross-couple pair is inserted to cancel out the parasitic output resistance too. A 70nH Active inductor with Q exceeds 100 is reported [59] from 0.83GHz to 1.33GHz. Various circuits have been proposed to further improve the active inductor quality factors and tuning range, examples includes using feedback resistor, etc.

![Active Inductor Circuit Examples](image)

**Figure 46: Differential active inductor circuit examples**

### 5.3.2 Improved Topology

Compared to single-ended active inductor, differential structure have inputs(outputs) of opposite phases, this feature enables flexibility of OTA choices for active inductor, e.g. an active inductor can be composed by two OTA-. Figure 47 below shows the proposed structure.
Its equivalent circuit topology is shown in Figure 48. It is made up of a differential pair and two single OTA-. Each employed the common-source single stage amplifier with high input and output impedance. Equivalent circuit and small signal model are listed in Figure 49 and Figure 50.
The input admittance of the active inductor is given by:

\[
Y = s2C_{gs2} + 2g_{ds4} + \frac{2g_{m1}g_{m4}}{sC_{gs4} + g_{ds1}}
\]

\[
L = \frac{2C_{gs4}}{g_{m1} g_{m4}}
\]

\[
R_s = \frac{2g_{ds1}}{g_{m1} g_{m4}}
\]

\[
Q = \frac{C_{gs4}}{g_{ds1}}
\]

From Equation 68, \( R_s \) is determined by \( g_{ds1}, g_{m1} \) and \( g_{m4} \), roughly,
\( g_{m1} \approx 10g_{ds1}, \) \( R_s \approx 2/10g_{m4}, \) therefore \( R_s \) is limited by the gain of \( M1 \) stage \((g_{m1}/g_{ds1})\) and can not be too small. For a 1nH differential active inductor we would like to apply in global clock distribution network, \( Q \approx \omega L/R_s, \) with fixed \( L \) value, and a relative high \( R_s, \) \( Q \) can not reach a high value. To decrease \( R_s, \) we need to increase \( g_{ds1}. \) There are two ways to improve \( g_{ds1}: \) to add a cross-coupled pair as a negative resistor to reduce \( g_{ds1} \) or to cascode differential pair to reduce conductance.

\textbf{5.3.3 Differential Active Inductor with Cross-Coupled Pair Compensation}

A Cross-Coupled pair can offer \(-g_m/2\) transconductance to reduce \( R_s \) value thus improve quality factor. Figure 51 shows the circuit schematic. And Figure 52 and Figure 53 are half equivalent circuit model and its corresponding small signal model. Transistor \( M_5 \) and \( M_6 \) are cross-coupled pair, which equals to a negative \(-2/g_{m5}\) shunt resistor to compensate \( R_s. \) Transistor \( M_7 \) forms a transmission gate and is used to control \( M_5, M_6 \) compensation, make sure the negative resistor introduced by \( M_5 \) and \( M_6 \) does not over-compensate \( R_s \) that leads to oscillation. The resistance of the transmission gate can be tuned by \( V_{bias}. \)
Figure 51: Schematic of differential active inductor with CCP

Figure 52: Half circuit equivalent model of differential active inductor with CCP

Figure 53: Small signal model of differential active inductor with CCP
The equivalent $L$ and $R_s$ of the differential active inductor with CCP can be expressed as following, where $g_{\text{trans}}$ is the equivalent resistance of the transmission gate $M_7$.

\[
L = \frac{2C_{gs4}}{g_{m1} g_{m4}} \\
R_s = \frac{2(g_{ds1} - g_{m5}) + g_{\text{trans}}}{g_{m1} g_{m4}} \\
Q = \frac{C_{gs4}}{(g_{ds1} - g_{m5}) + g_{\text{trans}}/2}
\] (69)

By adjusting $g_{\text{trans}}$ with $V_{\text{bias}}$, $R_s$ can be closed to zero and a large $Q$ is achieved. To verify the active inductor circuit, a differential active inductor around 1nH and 10 GHz operating frequency is designed and simulated with TSMC 28nm technology. The designed active inductor is intended to use as the active loading of standing wave clock distribution network. The detailed design parameters are listed in Table 7.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>1.8 V</td>
</tr>
<tr>
<td>$(W/L)_{1-4}$</td>
<td>$2.4\mu m/60nm$</td>
</tr>
<tr>
<td>$(W/L)_{5,6}$</td>
<td>$1.44\mu m/60nm$</td>
</tr>
<tr>
<td>$I_{bias_1}$</td>
<td>$940\mu A$</td>
</tr>
<tr>
<td>$I_{bias_2}$</td>
<td>$1.655mA$</td>
</tr>
<tr>
<td>$V_{casd}$</td>
<td>1.58 V</td>
</tr>
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</table>

Table 7: Design parameters of differential active inductor with CCP
Circuit simulation result is shown in Figure 54. At 10 GHz, inductance is about 1.2 nH with Q value around 327.

Figure 54: Simulation results of differential active inductor with CCP

Figure 55 shows the tuning range of the proposed differential active inductor with CCP. The circuit can operated in frequency between 6GHz to 15GHz with Q more than 100.

Figure 55: Tuning range of differential active inductor with CCP
To verify the voltage swing range that can be applied to the differential active inductor, total harmonic distortion (THD) is measured on various input amplitude. The results are shown in Figure 56. The inductor has 1% THD when input amplitude is 10mV and 10% THD when input amplitude is about 60mV. Therefore the differential active inductor with CCP is quite sensitive to its DC operating point and voltage swing, which is also common for other active inductor designs too [51].

5.3.4 Cascoded Differential Active Inductor

Another method to reduce $R_s$ is cascoding. By cascoding $M_1$ and $M_2$ with $M_5$ and $M_6$ in differential pair, output conductance is lowered to $g_{ds1}g_{ds5}/g_{m5}$ compared with original $g_{ds1}$. Figure 57 is the circuit schematic of cascoded differential active inductor.
Figure 57: Schematic model of cascoded differential active inductor

Figure 58: Equivalent model of cascoded differential active inductor
Figure 58 and Figure 59 are the corresponding equivalent circuit model and small signal analysis. The equivalent $L$ and $R_s$ of the cascoded differential active inductor can be expressed as following,

$$
L = \frac{2C_{gs4}}{g_{m1} g_{m4}} \\
R_s = \frac{2(g_{ds1} g_{ds5} / g_{m5})}{g_{m1} g_{m4}} \\
Q = \frac{C_{gs4}}{g_{ds1} g_{ds5} / g_{m5}}
$$

(70)

It can be seen that $Q$ is improved by $g_{m5} / g_{ds5}$ times. To verify the active inductor circuit, a differential active inductor around 1nH and 10 GHz operating frequency is designed and simulated with TSMC 28nm technology. The designed active inductor is intended to use as the active loading of standing wave clock distribution network. The detailed design parameters are listed in Table 8.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
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<td>$(W/L)_{3,4}$</td>
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</tr>
<tr>
<td>$(W/L)_{5-7}$</td>
<td>$90\text{nm}/60\text{nm}$</td>
</tr>
<tr>
<td>$I_{bias1}$</td>
<td>$700\mu A$</td>
</tr>
<tr>
<td>$I_{bias2}$</td>
<td>$881.6\mu A$</td>
</tr>
<tr>
<td>$V_{bias}$</td>
<td>1.4 V</td>
</tr>
</tbody>
</table>

Table 8: Design parameters of cascoded differential active inductor for Figure 57.

Figure 60 shows simulation results of the cascoded differential active inductor. The inductance is about 1 nH at 10GHz with Q around 344.

![Simulation results of cascoded differential active inductor](image)

Figure 60: Simulation results of cascoded differential active inductor.
Figure 61 shows tuning range of the cascoded differential active inductor. The circuit has Q above 10 at frequency from 8.25GHz to 10.07GHz. The operating frequency range is roughly 1.8GHz.

Total harmonic distortion (THD) is measured on various input amplitude. The results are shown in Figure 62. The inductor has 1% THD when input amplitude is 25mV and 10% THD when input amplitude is about 450mV. Therefore the voltage swing range of differential cascoded active inductor is larger than the differential active inductor with CCP before.
Figure 62: THD of cascoded differential active inductor
6 Standing Wave Clock Distribution with Active Inductor Loading

6.1 Introduction

In this chapter, active inductors proposed previously is applied to an X-tree clock distribution network. The design example is intended to deliver 10GHz clock globally with minimum skew and jitter on 28nm technology. Standing wave clocking with various active inductor loading are compared. The proposed scheme is compared with implementations in the existing literature too.

6.2 Standing Wave Clock Distribution with Single-Ended Active Inductor

![Figure 63: Standing wave on transmission line with active inductor loading](image)

Figure 63: Standing wave on transmission line with active inductor loading
Figure 63 shows the circuit schematic of applying proposed single-ended cascaded active inductor on a transmission line to generate standing wave. To drive the differential transmission line, two single-ended active inductors are used to act as a differential active inductor. By applying active inductor on both sides of the transmission line, the output voltage amplitude is improved. Figure 64 is the eye diagram and its zoomed in. From Figure 64, clock jitter is about 189 fs.

Figure 64: Eye diagram of standing wave on transmission line with active inductor loading
Figure 65: Global clock distribution with active inductor loading circuit schematic

Figure 65 is the circuit schematic of applying proposed active inductor on global clock distribution network. The size of the clock network is 4.96mm × 4.96mm. Parameters are listed in Table 9. Figure 66 is the transient simulation result. Figure 67 is the eye diagram and its zoomed in. The reported clock skew is 1.59 ps and clock jitter is about 0.39ps.
Table 9: Design parameters of global clock distribution with single-ended cascoded active inductor loading

<table>
<thead>
<tr>
<th>Item</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>60nm/2.4µm</td>
</tr>
<tr>
<td>$M_2$</td>
<td>60nm/9.6µm</td>
</tr>
<tr>
<td>$M_3 \sim M_6$</td>
<td>60nm/2.4µm</td>
</tr>
<tr>
<td>$C_L$</td>
<td>250aF</td>
</tr>
<tr>
<td>$C_Q$</td>
<td>1.05fF</td>
</tr>
<tr>
<td>$I_{bias}$</td>
<td>1.6mA</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.8V</td>
</tr>
<tr>
<td>length per segment clock</td>
<td>1.8mm</td>
</tr>
<tr>
<td>network size</td>
<td>4.96mm × 4.96mm</td>
</tr>
</tbody>
</table>

Figure 66: Transient simulation results for global clock distribution with single-ended cascoded active inductor loading
Figure 67: Eye diagram of global clock distribution with active inductor loading
6.3 Standing Wave Clock Distribution with Differential Active Inductor (CCP)

Figure 68 shows the schematic of applying differential active inductor with cross-coupled pair into an X-tree clock distribution network. Figure 69 shows simulation result and Figure 70 shows eye diagram respectively. The reported clock skew is 0.521ps and clock jitter is about 1ps.

Figure 68: Global clock distribution with differential active inductor loading and cross-coupled pairs
Figure 69: Simulation result of global clock distribution with differential active inductor loading and CCP

(a) Full eye diagram
(b) Zoom in of the first eye crossing
(c) Zoom in of the second eye crossing

Figure 70: Eye diagram of clock distribution with CCP active inductor
6.4 Standing Wave Clock Distribution with Cascoded Differential Active Inductor

Figure 71: Global clock distribution with cascoded differential active inductor loading

Figure 71 shows the schematics of applying differential active inductor with cascoded differential active inductor into an X-tree global clock distribution network. Figure 72 shows simulation result and Figure 73 show eye diagram respectively. The reported clock skew is about 1.95ps and jitter is about 0.16ps.
Figure 72: Simulation result of global clock distribution with cascoded differential active inductor

(a) Full eye diagram

(b) Zoom in of the first eye crossing

(c) Zoom in of the second eye crossing

Figure 73: Eye diagram of global clock distribution with cascoded differential active inductor
6.5 Comparison of Various Standing Wave Clock Distribution

Various clock distribution schemes have been proposed in recent years. As a comparison, Table 10 summarizes the detailed results from existing literature and this thesis. It should be noted that most of the results from literature are based on 180nm and 90nm technology nodes. Since the technology nodes are evolved in recent year, this thesis uses 28nm process as it is more likely to be used for digital systems of 10GHz clocks or beyond.
<table>
<thead>
<tr>
<th>Design</th>
<th>Tech CMOS</th>
<th>Power(mW)</th>
<th>Freq(GHz)</th>
<th>Jitter(ps)</th>
<th>Skew(ps)</th>
<th>Topology</th>
<th>Area(mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sasaki [8]</td>
<td>180nm 6Al</td>
<td>80</td>
<td>11.5</td>
<td>4.7</td>
<td>8</td>
<td>SWO mesh grid</td>
<td>5x5</td>
</tr>
<tr>
<td>Sasaki [9]</td>
<td>180nm 6Al</td>
<td>81</td>
<td>9.5</td>
<td>5.2</td>
<td>0.8</td>
<td>SWO ring curve</td>
<td>2.2x2.2</td>
</tr>
<tr>
<td>Frank O’Mahony [4]</td>
<td>180nm 6AlCu</td>
<td>460</td>
<td>10</td>
<td>5</td>
<td>1.5</td>
<td>SWO grid</td>
<td>3.6x3.6</td>
</tr>
<tr>
<td>Codero [5]</td>
<td>90nm 8metal</td>
<td>8.2</td>
<td>9.8</td>
<td>3.1</td>
<td></td>
<td>SWO mobius ring</td>
<td>0.39x0.39</td>
</tr>
<tr>
<td>SC.Chan [17]</td>
<td>180nm 6Al</td>
<td>168</td>
<td>1</td>
<td>22</td>
<td></td>
<td>LC tank, H-tree</td>
<td>5x5</td>
</tr>
<tr>
<td>This work</td>
<td>180nm 6Al</td>
<td>109.8</td>
<td>10</td>
<td>0.14</td>
<td>1.6</td>
<td>SWO X-tree</td>
<td>7.5x7.5</td>
</tr>
<tr>
<td>This work (single-ended AI)</td>
<td>28nm 11Al</td>
<td>98.79</td>
<td>10</td>
<td>0.39</td>
<td>1.59</td>
<td>SWO X-tree</td>
<td>4.96x4.96</td>
</tr>
<tr>
<td>This work (DAI CCP)</td>
<td>28nm 11Al</td>
<td>38.67</td>
<td>10</td>
<td>1</td>
<td>0.52</td>
<td>SWO X-tree</td>
<td>4.96x4.96</td>
</tr>
<tr>
<td>This work (cascode DAI)</td>
<td>28nm 11Al</td>
<td>55.49</td>
<td>10</td>
<td>0.16</td>
<td>1.95</td>
<td>SWO X-tree</td>
<td>4.96x4.96</td>
</tr>
</tbody>
</table>

Table 10: Comparison of different loading on standing wave clock distribution network
7 Conclusion and Future Research

7.1 Conclusions

The continuous demand for high-speed high performance microprocessors has constantly driven tremendous research efforts for decades. As CMOS technology scaling from generation to generation, the clock frequency of microprocessors will be soon approaching and beyond 10 GHz. Recently, there has been more and more focuses on low power design for better energy conserved and relaxing the heat dissipation requirement. Majority of modern digital design are synchronous systems that requires synchronous clocks to be delivered throughout the entire chip. Traditional clock distribution often consumes as much as 30%-50% of the total power. Many research efforts have been spent to explore alternative approaches for better clock skew, jitter control and lower power consumption. Resonant clock distribution is one of the promising techniques in that it can recycle the energy through the distributed wire inductance and capacitance.

In this thesis, we try to address some of the topics and open problems in the standing wave clock distribution, which is one of the resonant clock distribution schemes. The thesis starts from a literature overview of existing clock distribution techniques, including traditional clock tree, grid, hybrid and more recently resonant clock distribution schemes. A brief summary of transmission line theory is presented to provide enough background for the discussion later. RLG C model for TSMC 28nm technology is explained.
The thesis approaches the practical issues of standing wave clock distribution by analyzing a 10GHz X-tree global clock distribution design with both short-end loading and passive spiral inductor loading. One cross-coupled pairs structure is proposed to compensate the transmission line loss when it is closed or beyond half of wave length. Detailed simulation results are presented. The key benefit of using passive spiral inductor loading is that it can provide almost uniform amplitude output. This greatly relaxes the buffer requirement as compared to the one in short-end loading scheme.

The thesis extends the idea of passive inductor loading by using active inductor loading. The key benefit from active inductor loading is its smaller area overhead, tunability and high quality factor. The design is ready to be integrated into existed chips as well. Key design issues such as active inductor designs are explored. Three circuit designs with both single-ended and differential schemes are proposed. All of them achieves much higher quality factor than its passive inductor counterpart. The proposed CMOS active inductors are applied to a X-tree global clock distribution design to demonstrate the effectiveness of the standing wave generation. Simulation results show that the proposed clock distribution schemes with active inductor loading can provide clock delivery with low skew and jitter.

7.2 Future Research Directions

Several practical aspects of this research are worth to check for further investigation:
Firstly, the tuning range of the active inductor needs to be further improved with a reasonable quality factor, e.g. $Q$ more than 10. For modern microprocessors running at multi-GHz, power saving techniques like Dynamic voltage and frequency scaling (DVFS) and big-little architecture are vastly employed. Therefore, the clock frequency spans a huge dynamic range. For fine-grained power saving, the clock frequency range usually has a variation of more than 30%. In extreme case that the clock frequency might go down as far as 10% of its maximum. Mechanisms to switch between standing wave clock distribution and traditional clock distribution are worth to investigate too, since it provides a safe alternative and better reliability.

Secondly, the design of effective clock grid for standing wave resonance is an active research topics as well. Clock networks to completely remove the requirement of local buffers are actively exploited by various researcher. The buffer-less clock delivery concept has significant advantage on deep power saving.

Lastly, a systematic framework including automated clock distribution design, generation and skew/jitter calculation would be an interesting topic too. It will make the resonance clock distribution scheme widely deploy and practically use.
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