High Speed DRAM Transceiver Design for Low Voltage Applications with Process and Temperature Variation-Aware Calibration

A Dissertation Presented
by

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To my family.
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List of Acronyms

ADC  analog-to-digital converter
BER  bit error rate
C\textsuperscript{2}MOS  clocked complementary metal-oxide-semiconductor
CDR  clock and data recovery
CML  current mode logic
CP   charge pump
CTAT  complementary to absolute temperature
CTLE  continuous-time linear equalizer
DFE  decision feedback equalizer
DSP  digital signal processing
FIR  finite impulse response
HSUL  high speed un-terminated logic
IC  Integrated circuit
IIR  infinite impulse response
I/O  input/output
ISF  impulse sensitivity function
ISI  inter-symbol interference
LFSR  linear feedback shift register
LMS  least mean square
LPF  low-pass filter
LVSTL  Low Voltage Swing Terminated Logic
PCB  printed circuit board
PFD  phase frequency detector
PLL  phase-locked Loop
PTAT  proportional to absolute temperature
PVT  process, voltage and temperature
PRBS  pseudo-random binary sequence
RX  Receiver
SAFF  sense amplifier flip-flop
S/H  sample and hold
SSTL  stub series terminated logic
SS-LMS  sign-sign least mean square
TC  temperature coefficient
TX  Transmitter
UI  unit interval
VCO  voltage controlled oscillator
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Abstract of the Dissertation

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by

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Scaling down of integrated circuits (ICs) enables continuous improvement of the operation frequency on many processor and memory capacity. On the contrary, bus performance and I/O channel speed have not been followed the growth. The link speed is limited by the channel bandwidth due to its low pass filtering characteristics. To extend the channel bandwidth and increase signal integrity with low power consumption at multi-Gb/s data rates, new low-voltage signaling is adopted and channel equalization is an essential technique in mobile DRAM I/O part.

The impedance calibration for output driver of transmitter is a widely used and effective way to improve signal integrity against various chip variations such as process related parameters and operating temperature. As a fast and efficient impedance calibration solution, a novel on-chip impedance calibration methodology for the LVSTL (low voltage swing...
termination logic) application is proposed in this dissertation. The proposed variation-aware open-loop calibration utilizes local on-chip sensors to compensate mismatches and variations of the DRAM transmitter drivers from process and temperature variations. In addition, the output driver with shared resistance is proposed which significantly reduces the chip area by 50% compared to the conventional approach while maintaining same linearity characteristics.

The proposed circuitry is designed with a DRAM bidirectional transceiver, and implemented and tested with a standard 0.18\textmu m CMOS technology. The impedance calibration technique is demonstrated with external termination resistances of 40, 48, 60, 80, 120, and 240 \textOmega. The active area including power-ring of the transmitter is 0.14\text{mm}^2 with only 0.48\text{mm}^2 of the proposed calibration circuit overhead.

Input buffers in DRAMs convert attenuated signals to rail-to-rail signals. In conventional designs, differential input buffers are used for high-speed and low-power operation. However, according to the convention of LVSTL signaling, the input common-mode of receiver is significantly decreased to one-sixth of the supply voltage. Therefore, it is more efficient to design a sense amplifier with PMOS input, considering the input common-mode range to enhance sensitivity and detect the incoming signal. Moreover, the proposed receiver is designed with adaptively gain controlled performance to optimize operation speed of the receiver design and reduce the power consumption by 15-20% according to chips process variations with enough timing margin.

As the voltage swing becomes lower and lower, equalization is necessary at the receiver end. One of a common topology is the decision-feedback equalizer (DFE), a nonlinear equalizer design well-suited for multi-Gb/s date rates. In this work, two main blocks, the summer and sampler circuits, are merged to reduce power consumption. In addition, the sampler is designed as a cascode structure, which increases kick-back noise immunity and reduces power consumption by 11\%. To enhance equalization performance, a power efficient continuous-time linear equalizer (CTLE) is also implemented ahead of the DFE stage to demonstrate the bandwidth compensation functionality. The equalizer circuits are implemented in 45 nm CMOS technology. The equalizer design is demonstrated with channel loss of 15 dB at Nyquist frequency. Also, the phase-locked loop (PLL) integrated in the proposed receiver provides 5 GHz clock with 12.62 ps peak-to-peak jitter. The core receiver circuit consumes 14.3 mW with a 1.1 V supply voltage when processing data at 10 Gb/s rate.
Demand for higher data transmission bandwidth is continuously increasing as the requirement of many wireline applications increases. Bandwidth of DRAM also has been continuously increased as the amount of data transmission is rapidly increased along with the processing contents such as high-resolution display as well as high speed wireless communications [1,2]. Along with development of the DRAM performance, its applications are diversified and specified as well. DDR (double data rate) memory is classified into major three configurations based on different applications. Different from DDR memory mainly for PC applications, the graphics memory (GDDR) is developed toward high bandwidth memory for processing massive graphics data. Meanwhile, memory for mobile applications (LPDDR) have been also developed where low power consumption and less area are important design features. The performance trend of memory is shown in Figure [1.1] with supply voltage which refers to power consumption [3]. Not only performance but also battery lifetime are critical factors in the mobile devices, which makes power consumption issue
CHAPTER 1. INTRODUCTION

Figure 1.1: DRAM performance trend [3]

even more critical and many power reducing techniques are being used. Number of I/O pins is increased as a solution to extend the data bandwidth. Therefore, I/O part still takes a large portion in the power consumption [4].

Moreover, high density and signal integrity issues have to be resolved in high-speed operation with lower voltage between DRAM and memory controller unit. To alleviate those issues, several techniques are adopted to enhance BER such as channel equalization [5-7], pre-emphasis [6,8,10], de-skewing [11], duty cycle correction [12,13]. In addition, chip to chip or on-chip process and temperature variations lead to mismatch and degrade signal quality. Impedance matching technique is also an essential part to reduce signal reflections.
CHAPTER 1. INTRODUCTION

1.1 Motivation

Supply voltage gets lower and lower to satisfy low power consumption at high speed operation. Recently, low voltage swing termination logic (LVSTL) \([14]\) interface is adopted instead of stub series terminated logic (SSTL) or high speed un-terminated logic (HSUL) in mobile applications. With the low voltage signal swing, the signal integrity in transmitting and receiving the signal becomes more important along with the data transmitting speed. Since the serial interface between two different digital systems with communication channel is limited by the bandwidth, not only those problems caused by simultaneously switching noise (SSN) or crosstalk but also inter-symbol interference (ISI), signal attenuation or reflection problems caused by impedance mismatching in high frequency operation become challenging issues. Furthermore, the impedance mismatch comes from process and temperature variation, and device mismatches. The problems are exacerbated at the low power application, where the VOH is scaled down from VDDQ/2 to VDDQ/3 - VDDQ/4 in the LPDDR4.

As an efficient way to improve signal integrity by reducing signal reflections even in high speed signaling, ODT (on-die termination) and OCD (off-chip driver) have been standardized for DQ and DQS output level trimming in memory design. However, currently used driver calibration techniques \([15] - [18]\) require power consumption and timing burden, also uses ZQ pin to connect external resistor while calibration. Moreover, simple input buffers have been used due to the short channel length and operation speed at receiver designs. However, as the VDDQ and VOH get lower and lower in the low power applications, and also operation speed of transmitting signals is faster, it is difficult to guarantee high BER with
the conventional input buffer designs. Therefore, it is inevitable to use complex equalization technique on the receiver front-end. This dissertation investigates a novel on-chip open-loop self-calibration approach for output driver calibration without using external resistor and minimizes calibration timing and power consumption. In addition, a low power 1-tap discrete feedback equalizer (DFE) is designed for the low common-mode input signaling.

1.2 Objectives and contributions

In this dissertation, an on-chip open-loop self-calibration approach to minimized channel reflection at transmitter is designed and verified with chip testing. In the receiver, low power design with channel equalization is demonstrated. The main contributions of this research are:

– An on-chip open-loop self-calibration impedance matching for LVSTL signaling.
– Low power self-calibration with on-chip process and temperature sensing.
– Slew rate control and pre-emphasis design in transmitter
– Low common-mode receiver design with low power equalization.

1.3 Organization

Chapter 2 describes basic components of the high-speed memory interface system including transmitter and receiver. Also, channel loss and noise sources are introduced in this chapter. In Chapter 3 conventional impedance calibration schemes are studied. Chapter 4 shows the proposed on-chip driver impedance calibration technique on transmitter
CHAPTER 1. INTRODUCTION

design that is adopted on LVSTL signaling. In this chapter, on-chip process and temperature sensing designs are shown as an open-loop self-calibration method. Designed circuits are introduced with their simulation data. Fabricated chips are tested on printed circuit boards and the measurement data are shown in Chapter 5. Receiver equalization design with low VDDQ at 45nm CMOS process is in Chapter 6. Finally, the conclusion and future work are presented with the summary of this dissertation is in Chapter 7.
Chapter 2

Backgrounds

As CMOS technology developed and its rapid scaling enables the high volume of memory storage, it requires high bandwidth to process the vast amount of data. However, wire bandwidth limitation have not shown dramatic improvement over the years, while the on-chip speed has led to a growing interest in developing faster I/O for chip-to-chip communication [19–21]. Channels are used to transmit the data in the multi giga-bits per second range as interfaces between memory and its controller. Also, growing demand for reliable operation on lossy channels that produce significant inter-symbol interference (ISI) requires at least bit-error-rate (BER) of $10^{-14}$ on transceiver systems especially as the operation speed goes up. As will be described in later, there are major challenges in high speed data transfer; frequency dependent channel loss including ISI, crosstalk, and skin effect that affects significantly on correct data transmission even in short channels. In the beginning of this chapter, we introduce the memory I/O interface that is specialized design in order to achieve high data rates with high reliability. Detailed circuitry, transmitter and
CHAPTER 2. BACKGROUNDS

receiver, will be described later of dissertation. Before that, the basic concept and overview of design consideration will be introduced in this chapter.

2.1 DRAM Interface System

The I/O interface system enables transmission a large amount of data point-to-point while reducing the complexity, cost, and power. At higher-frequency rates, the problems associated with wide parallel buses are further exacerbated. A faster-switching parallel bus consumes more power and suffers from simultaneously switching noise (SSN). In addition, large skew mismatches can lead to timing issues at the receiver as many systems need to clock in the parallel data as a group of aligned bits. Many other problems arise for parallel data-bus implementations as frequency and transmission distance increase. Issues such as signal integrity, power usage, and timing can all have a significant impact on a I/O design. We introduce the basic concepts on the interface system, and discuss the circuit level design issues in the following sections.

The Figure 2.1 illustrates the I/O interface block diagram between LPDDR4 DRAM and controller. At the transmitter side, input data are serialized and transferred through a channel to increase the date rate. When the transmitted signals arrive at the receiver side, the signals are distorted and degenerated. The receiver block recovers the incoming data stream and compensates the signals. As the low common-mode voltage, the receiver uses pMOS input transistors with the VSSQ termination. The de-multiplexer is composed using a latch-type receiver for parallel interface.

In read operation, the transmitter delivers DQ, DQS_t, and DQS_c data to the controller.
In write operation, DQ data to the DRAM receiver comes with the DQS_t/DQS_c; sampling signals internally divided into the half; and then goes through de-multiplexer using a latch-type receiver. After then, the data (DQi) finally gets written to the DRAM cell. The transmitter takes a role for the training during write operation \[22\].

### 2.2 Data Transfer Rate

Maximum data transfer capacity is an important factor among various parameters to evaluate performance of interface circuitry. Shannon-Hartley theorem \[23\] describes the
upper limit on the data rate that can be transmitted over a communications channel. It is noted that the symbol transfer rate is related directly to the channel bandwidth by the Nyquist rate. By applying the theory to a non-return-to-zero (NRZ) signaling, the maximum data transfer rate in bits per second as a function of the interconnect channel bandwidth and the signal-to-noise ratio (SNR):  

\[ D = BW \log_2(1 + SNR) \]  

Equation (2.1) shows that we can increase throughput across interconnect either by increasing the SNR or by increasing the bandwidth of the signal. However, the lossy nature of PCB transmission lines will tend to nullify the benefit of increasing the signal bandwidth since the content at high frequencies will be attenuated by the interconnect, thereby limiting the usable bandwidth.

The data rate in high speed interface system can be limited not only by the channel and also by the circuit operation speed. The lock generation and distribution limits the circuit bandwidth. Generally, the maximum clock frequency that can be efficiently distributed is limited by clock buffers ability to propagate narrow pulses. The minimum clock period is assumed close to 8FO4 inverter delay.

Since the receiver circuitry converts the lossy signal through channel to rail-to-rail voltage swing and digital data, the error probability needs to be defined. The bit-error rate (BER) indicates the reliability of the link system. The BER specification is usually required \(10^{-12}\) or lower to insure the robustness of interface system. A BER of \(10^{-14}\) translates into
Figure 2.2: Example received eye diagram

\[ \frac{V_{pp}}{2 \sqrt{V_n^2}} = 7.6 \] from the following equation \[26\] where noise is only considered.

\[ BER = Q \left( \frac{V_{pp}}{2 \sqrt{V_n^2}} \right) \] \hfill (2.2)

where

\[ Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{x^2} \left( -\frac{u^2}{2} \right) du. \] \hfill (2.3)

\( V_{pp} \) is the peak-to-peak input swing and \( V_n \) is the total input referred noise.

To evaluate the BER of a signal and the system performance, most high-speed designs use the eye diagram. The eye diagram is constructed by slicing the time-domain signal waveform and superimposing a small number of symbols in length. The horizontal axis of the eye diagram represents time and is typically one or two unit intervals (UI), while the vertical axis represents the amplitude of the signal. The eye opening is a metric often used to judge the quality of the signal integrity and measured by eye height and eye width.
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Distortion of the signal from timing variation (jitter) and voltage noise causes the data eye to close.

A widely used method for evaluating whether or not the eye meets the system timing and noise requirements is to apply an eye mask. The mask represents a forbidden region that the actual eye must not cross, and it includes the receiver set-up and hold window and voltage specifications, and all jitter and noise terms [25]. We can evaluate the performance of a design by comparing it to a specification.

2.3 Channel

The channel is considered all materials including package, line trace, connectors, and vias on PCBs, between transmitter and receiver. In high-speed link system, the most common types of channels are printed circuit board (PCB) strips. At giga bit rate frequency, the FR4 trace behaves as a transmission line which has to consider frequency dependent loss and reflection. Therefore, the termination schemes are essential for impedance matching purpose.

Several physical effects degrade signal integrity at data rates above a few gigabits per second. Skin effect of the transmission lines become severe at the high data rates. Via stubs on the circuit boards and other impedance discontinuities associated with the chip packages and connectors cause reflections.

The channels are act as low-pass filters. This property significantly attenuates the signal and causes the inter-symbol interference. Since the transmitted signal is attenuated by loss, it is also easily corrupted by crosstalk from other channels. If the channel adding so much
CHAPTER 2. BACKGROUNDS

Figure 2.3: Example interconnect channel impact on a 4Gb/s signal waveform: (a) transmitter output; (b) receiver input

loss and distortion to the signal, the data eye at the receiver end can be completely closed, and advanced equalization is required to recover the transmitted bits [27].

2.3.1 Inter-Symbol Interference (ISI)

The most significant phenomenon of signal distortion is the inter-symbol interference (ISI). This is an unwanted phenomenon as the previous symbols have similar effect as noise, thus making the transmitted signal less reliable [28–31]. In Figure 2.3 a transmitted input
CHAPTER 2. BACKGROUNDS

![Graph showing frequency dependent channel loss]

Figure 2.4: Frequency dependent channel loss

signal and the channel response at the receiver end are also shown.

The high-frequency components get attenuated much more severely than do the low-frequency components, as displayed in Figure 2.4. Since losses increase with frequency, bit patterns that have a higher frequency content will be attenuated more. In other words, for fast bit patterns, the time it takes for the signal to charge up the interconnect and transition to its maximum value is greater than the switching rate of the transmitter. Since the disparity of losses between low and high frequencies is what causes ISI, the slope of the loss curve tends to outweigh its magnitude [25].

2.3.2 Inter-Channel Interference (Crosstalk)

DRAM signaling interfaces in which large numbers of transmission lines are routed in parallel through packages, connectors, and printed circuit boards same as other digital systems. Crosstalk occurs when one switching line injects noise into one or more neighbouring
CHAPTER 2. BACKGROUNDS

signals mostly through mutual capacitance and mutual inductance. The crosstalk can play an important role in determining the performance of the system.

As the ICs scaled down, crosstalk affects signal integrity and timing by modifying the propagation characteristics of the lines more seriously. Also, crosstalk couples noise onto lines, which harms signal integrity and reduces noise margins [25].

The crosstalk due to mutual inductance generates a voltage pulse as $V = L_M \frac{dI}{dt}$ on the victim line due to the $dI/dt$ on the aggressor line. Similarly, the mutual conductance also generates a voltage spike from $I = C_M \frac{dV}{dt}$ on the victim line [32]. To alleviate the crosstalk problems, there are several approaches on circuit design level to layout and PCB level. In transmitter design, one effective way is to increase the rise time of signal, called slew rate control, which That is introduced in the later chapter.

2.3.3 Skin Effect

At high frequencies, the resistance of wire becomes frequency dependent due to the phenomenon so called skin effect. High-frequency currents tend to flow primarily on the surface of a conductor, with the current density falling off exponentially with depth into the conductor as shown in Figure 2.5. Note that although the magnitude of the current density is oscillatory, it remains within the envelope defined by the exponential decay of the skin depth. The skin depth $\delta$ is defined as the depth at which the current falls off to a value of $e^{-1}$ of its nominal value, and is given by

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}}$$  (2.4)
where $\rho$ is the resistivity of the wire, $f$ is the frequency of the signal, and $\mu_r$ is relative permeability of the surrounding dielectric. Since the skin depth decreases with the square root of frequency, and since the resistance of a conductor increases linearly with conductor thickness, the apparent resistance of a conductor increases as the square root of frequency [32]. The increased resistance at high frequencies cause signal attenuation and distortion when the signal is transmitted over the wire or on board. Therefore, improved signal recovery strategies are necessary as the data transmission speed higher.
Chapter 3

Prior Arts of Transmitter Design

High speed data transmission between a DRAM device and a memory controller requires careful design of IO drivers to ensure that the required voltage levels of signals are achieved. Process, voltage, and temperature (PVT) variations in chip fabrication and different operation environment led to mismatch of the output driver impedance, resulting in deviations from the desired value. Many output driver calibrations are proposed and used in memory systems to improve operation limits and provide reliability over a wide range of operating conditions. In this chapter, the prior output driver calibrations will be studied and analyzed.

3.1 Output Driver Calibration

Incorporating a resistive termination within the DRAM device, which is often referred to as on-die termination (ODT), improves the signaling environment by reducing the electrical discontinuities introduced with off-die termination. With the off-die termination, a signal propagating from the memory controller to the DRAM encounters an impedance discontinu-
CHAPTER 3. PRIOR ARTS OF TRANSMITTER DESIGN

Figure 3.1: Data eye without/with output driver calibration

ity at the stub leading to the DRAM on the module. The signal that propagates along the stub to the DRAM will be reflected back onto the signal line, thereby introducing unwanted noise into the signal. The introduced noise and the consequential signal degradations that are not addressed by such off-die termination become more pronounced with higher data rates and longer stub lengths. By terminating transmission lines on die, the signal reflections and attenuations are significantly reduced that enables faster data rates [33].

However, the impedance value is also affected by PVT variations which reduces the eye opening of receiving data same as crosstalk or ISI reduce it. The eye opening, measured as eye height and eye width, is interpret into the signal quality as voltage/timing margin. That is, closing the eye leads to lower BER in transmitted data as shown in Figure 3.1. Before considering equalization techniques on transmitter and receiver circuits, compensation of the PVT variations is an efficient and effective way to increase reliability. Calibration for the transmitter output driver reduces impedance mismatch and reflections. In order to increase signal data rates and reduce IO power, output driver overshoot and undershoot must be managed.

The output driver calibration provides benefits from the device up through the system. By
CHAPTER 3. PRIOR ARTS OF TRANSMITTER DESIGN

increasing DRAM yield and allowing DRAM output drivers to automatically compensate for process variation, output driver calibration improves margin and device testability, saving design and test time. It also allows board designers to compensate for variations in trace impedance and termination voltage caused by manufacturing and assembly processes. This ability to compensate for manufacturing tolerances of some components enables test specifications to be relaxed and saves component and tester costs. At the system level, the calibration enables system integrators to use one DRAM in multiple designs that utilize different trace impedances and that operate in different environments. The output driver calibration also increases voltage and timing margins, resulting in higher system reliability over a wider range of operating conditions. In addition, adjustable drive strengths help compensate for variations in temperature which allows system integrators to more effectively manage their system power and thermal budgets, thereby decreasing overall system cost [33].

3.2 Conventional ZQ Calibrations

The basic concept of the conventional ZQ calibration for DRAM transmitter is exemplified in Fig. 3.2. The pull-up drivers are composed as NMOS devices in the low voltage swing termination logic (LVSTL), which is adopted in LPDDR4 DRAM for high speed operation in low VOH value using AC on-resistance at data transition points. In other cases, the pull-up drivers are designed with PMOS devices and the calibration concept explained in Figure 3.2 is applicable in both cases without difference.

One pull-up unit is composed of an n-bit pull-up transistor array to set 240 Ω pull-up driver. In this example, there are 6 units connected in parallel for different termination
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impedance matching cases, and pull-down driver is constructed in the same manner. When the ZQ (impedance matching calibration pin) command is launched, pull-down driver is trimmed first without pull-up transistors (switch 2 is open at this time in Fig. 3.2). The pull-down transistors are all turned off initially and the DQ (bi-directional data pin) node is connected to VDDQ through 240 Ω external resistor, and the DQ node voltage is compared to VDDQ/2. The calibration continues by turning the pull-down transistors one by one from LSB until the comparator detects that DQ node is low. The next step is to set VOH level from pull-up driver calibration. In this step, one of the comparator input voltages is switched to VOH, and the drive strength of the pull-up driver is adjusted in the same way as the pull-down driver. Commonly, DQS pins for clock signal also use the same calibration process, and the calibration command is enabled before every read and write operations. The main drawback of the conventional approach is that the calibration has to be performed

Figure 3.2: Concept of conventional ZQ calibration scheme.
Figure 3.3: Output driver self-calibration scheme with the option of externally undated calibration scheme in [15].

sequentially for each of the units and each of DQ pins due to the voltage and temperature drift.

An output driver self-calibration scheme used in DDR3 SDRAM is shown in Figure 3.3. The pull-up current is first self-calibrated by comparing it with the current flowing through the reference resistor connected to a pad newly added in DDR3 SDRAM and named as ZQ, and then the pull-down current is automatically tuned with the pull-up current that is already adjusted [15]. The calibration information is used in updating the registers that generate the signal bits to control the value of termination resistance depends on applications. This
CHAPTER 3. PRIOR ARTS OF TRANSMITTER DESIGN

Figure 3.4: Optimized impedance calibration circuit in [16].

calibration scheme utilizes comparator, external resistor and reference voltage that is similar method as in the reference calibration technique. Even though its self calibration operation, the calibration cycles for every DQ and DQS pins still remains within long operation cycles.

Another design for impedance calibration circuit is shown in Figure 3.4. In this design, the impedance calibration circuit operates when the chip is initialized or the auto-refresh command is issued. In conventional methods, an unexpected code variation can be generated during operation due to comparator input offset voltage, even though the external ZQ resistor and internal calibrated impedance are identical values. To reduce the unexpected errors, this calibration circuit has new feature that the structure of an impedance-to-digital converter. To increase calibration reliability, the comparison operation is executed twice with a digital low-pass filter (LPF) controlling the comparator output signal and code counter. The code counter is disabled when the two comparison results are same, accomplished by a register.
and XNOR circuit. With the LPF method, the impedance code has a fixed level that is captured in the offset voltage. Also, code shifter based output driver is used to reduce Cio and enhance data transfer rate. Even though the code shifter concept is used, the decoder part is still complicated, and the digital filters make the large circuit area in this design.

In the memory cell, only one pad, ZQ, is allocated for the external resistor. However, if x32 IOs are used, global ZQ calibration is needed. The Figure 3.5 displays the block diagram of the calibration in [17]. The calibration method can detect the impedance variations of each ODT/OCD independently with the help of the local PVT variation sensor. This design achieved the impedance matching with high accuracy by sensing global on-chip variation.
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However, controller, pre-amplifier and local sensors occupies more area than output drivers. Moreover, since the control circuit operates at high frequency (500MHz at 2Gbps maximum data rate) with ring counter, it consumes high power (18mW with 1.8V supply voltage) than other calibration schemes.
Chapter 4

Transmitter for LVSTL Signaling with Proposed Calibration Technique

We studied prior arts of output driver calibration in previous chapter. Although its advantages in high accuracy, there are drawbacks in duration of the calibration and its hardware complexity and power consumption. In this chapter, an open-loop on-chip calibration is introduced that corresponds to the global ZQ calibration. The output driver calibration is optimized to the LVSTL signaling for LPDDR4. In addition, a design approach for output driver is proposed, which makes it possible to save die area in transmitter driver size.

4.1 Low Voltage Swing Terminated Logic (LVSTL)

In DDR and GDDR DRAMs, the memory interface has been changed to enhance DRAM data ratem such as SSTL (Stub series termination logic), POD (Pseudo open drain). Similarly, termination changed from HSUL (High speed un-terminated logic) to LVSTL
CHAPTER 4. PROPOSED OUTPUT DRIVER CALIBRATION FOR LVSTL

Figure 4.1: VDDQ and low voltage swing with VSSQ termination (Low voltage swing termination logic) in LPDDR DRAMs [34–36].

The LVSTL interface has advantages of low $C_{io}$ (input/output capacitance) and low power consumption with lowered output swing level (VOH) and no static power consumption while driving logic low. With the low voltage signal swing, the signal integrity in transmitting and receiving the signal becomes more important along with the data transmitting speed. Since the serial interface between two different digital systems with communication channel is limited by the bandwidth, not only those problems caused by switching noise or crosstalk but also signal attenuation or reflection problems caused by impedance mismatching in high frequency operation become challenging issues. The problems are exacerbated at the low power application, where the VOH is scaled down to VDDQ/3 in the low power DDR standard as shown in Figure 4.1.

In the figure shown above for LPDDR, several I/O training operations have been used and additional constraints are included to achieve high data bandwidth and low BER. Trainings
for CA, DQ/DQS, and VREF are such operations for proper signal transmission. Currently, most of conventional impedance calibration schemes use the ZQ pin to compensate impedance mismatches [22, 37, 38]. The training sequences have to be placed between data read and write sequences to improve signal fidelity. Consequently, correct modeling of impedance calibration interval timing is important in the conventional methods to increase the data transfer rate. Moreover, another design challenge comes from the increased complexity of high volume memory due to the implementation of clocked dynamic calibration [39]. Furthermore, thermal issue is also a major issue not only in the currently used LPDDR4 standard but also beyond this configuration including wide I/O signal transmission. The thermal drift has a high correlation with refresh timing control of the training that is also a major concern to ensure reliable system operation and achieve high data rate [40].

4.1.1 A Prototype of NMOS-Only Output Driver (NOD)

A prototype of LVSTL I/O cell is presented in Figure 4.1, which is the pseudo open drain (POD) with VDDQ termination. However, it is hard to achieve LPDDR4 data rate even with VDDQ termination with lowered supply voltage. In LPDDR DRAMs, power consumption is a major performance with operation speed. Since the pull-up and pull-down devices operate at the linear region with POD transmitter, current capability decreases as following the scaled-down supply voltage. The driver size has to be increased for sufficient current driving capability, which limits the high frequency operation due to the increased Cio.

With the LVSTL signaling, transmitter can generate low voltage swing signals at high
CHAPTER 4. PROPOSED OUTPUT DRIVER CALIBRATION FOR LVSTL

Figure 4.2: I-V characteristics of each termination in Figure 4.1.

frequency with the VSSQ termination to reduce power consumption. The pull-up device operates as a source follower at the saturation region that provides fast current. It is also possible to reduce junction capacitance from the small pull-up device size with large gain. The VOH value is determined as $I_{PU} \times R_{term}$ and the pull-down device with $R_{term}$ formulates ground level [41].

4.2 Impedance Calibration Technique to Compensate Process and Temperature Variations

We studied prior arts in the previous chapter and also discussed about issues related to the new low voltage termination. As an efficient solution of the previously issues, we
proposed an on-chip variation aware open-loop self-calibration method to compensate offsets and improve the performance of the interface circuits. The open-loop technique provides much smaller, faster calibration and consumes less power than the conventional feedback calibrations with trade-off on inaccuracy. Another advantage is that timing burden and complexity of design are significantly reduced comparing to the conventional methods while preventing performance degradation from process variations and temperature drift. To demonstrate the feasibility of the method, we proposed an on-chip impedance open-loop calibration technique to actively control the characteristics of the transmitter output drivers. The impedance calibration targets to match VOH value at VDDQ/3 in this section followed by LPDDR4 standard.

4.2.1 Calibration Procedure

Figure 4.3 illustrates the proposed on-chip calibration technique at the interface between DRAM and SoC/AP application for the half DQ pins of the channel in LPDDR4 architecture. The proposed impedance calibration method compensates impedance mismatches from process and local temperature variations [42]. One process sensor is located in the die, on the other hand, two localized temperature-monitoring sensors are placed close to the 8 DQ pins to increase sensing reliability.

In this technique, ZQ pin and external termination resistance are unnecessary. Instead, impedance calibration codes are stored in a look-up table (or using decoders) for each of the process corner profiles and a wide temperature range of operation. Once the impedance calibration process is enabled, process sensor is activated and the quantized output is stored
Figure 4.3: Proposed on-chip impedance calibration scheme on DRAM-Soc/AP interface
CHAPTER 4. PROPOSED OUTPUT DRIVER CALIBRATION FOR LVSTL

in the register. The sensor output voltage range corresponds to one of process corners. Data conversion is required for the analog output of the sensors. In this research, a simple 2-bit flash analog-to-digital converter (ADC) is used to digitize sensor outputs, and to minimize power and silicon area. Once the valid data is stored in the register, the process sensor is disabled for power efficiency. On the other hand, the temperature-monitoring sensor operates in real-time mode to adjust VOH against temperature drift. The analog output of the temperature-monitoring sensor is digitized as well. The two digital codes representing process corner and temperature are decoded for optimum ZQ calibration codes that control the transistor arrays of transmitter driver with ZQ select code (ZQSB) for proper current strength selection on different applications. Finally, the termination impedance selection for different applications can be performed by controlling the ZQSB[5:0]. A table containing the control codes and corresponding termination impedance values is shown in Figure 4.3.

4.2.2 Proposed Process Sensor Design for Impedance Calibration

In this section, on-chip process sensors, which detect chip process variations, is introduced. Proposed circuit is shown and the analysis and simulated data are also followed.

The threshold voltage, $V_T$, is a dominant factor in process variation, and the on resistance, $R_{ON}$, is inversely proportional to $\mu_n C_{ox} W/L (V_{GS} - V_T)$. Therefore, the process variation is directly related to the impedance matching problem. The proposed process sensor design that produces different output voltage level depending on NMOS threshold voltage, $V_{TN}$. Also, the sensor output should not be affected by other parameters such as temperature and supply voltage variations, but be sensitive to process corners. Thus, looking into the process
 CHAPTER 4. PROPOSED OUTPUT DRIVER CALIBRATION FOR LVSTL

Figure 4.4: Proposed on-chip process sensor design

dependent parameters precedes the proposed design to understand major factors for sensor design.

The proposed on-chip CMOS process sensor design that utilized in the calibration architecture is shown Figure 4.4. The threshold voltage independent characteristic is referred from [43]. To supply a constant current source in all process corners, the threshold voltage independent current source is designed. There are other process dependent parameters which affect to drain current such as gate oxide thickness or mobility, however, the threshold voltage is a major parameter to determine the process corners. Therefore, a threshold voltages independent current source is designed, and the schematic is shown in the left side in the Figure. The NM1 and NM3 are operated in linear region, and the DC voltage applied to gates of NM1 and NM3 are VB and VB+dV, respectively. Each of the drain currents is
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noted in equation (4.1). The two input transistors should stay in linear region and have input voltage difference as $\Delta V$. If $V_{GS} - V_{th} >> V_{DS}$, the drain currents for $I_1$ and $I_2$ are written as

$$I_{D1} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th} - \frac{V_D}{2})V_D,$$

$$I_{D2} = \mu_n C_{ox} \frac{W}{L} (V_{GS} + dV - V_{th} - \frac{V_D}{2})V_D,$$

(4.1)

and

$$I_{REF} = I_{D2} - I_{D1} = \mu_n C_{ox} \frac{W}{L} dVV_D$$

(4.2)

Since the $V_{th}$ term is cancelled in equation (4.2), the current can be used as a process independent source.

On the right side of the circuit in Figure 4.4, PM3, NM4, and NM5 are composed as a process sensing part, where PM3 supplies a constant current mirroring from PM2, and output voltage level depends on the threshold voltages of nMOSFETs (NM4 and NM5). As the output drivers of the LPDDR4 transmitter are designed only with NMOS both pull-up and pull-down networks, process corner for NMOSFETs are interested no matter what the corner of pMOSFETs is. Therefore, the two nMOSFETs are stacked to differentiate among different process corners with the threshold voltage difference.

The process sensor is required at the beginning of the operation and the result can be stored in register instead of operating continuously. Therefore, a power switching part is added to disable the process sensing circuit and minimize power consumption.

Figure 4.5 shows a single-ended differential amplifier configuration. Due to the large input impedance and the high gain of the operation amplifier, the drain voltage $V_D$ in
Figure 4.5: Schematic of differential amplifier in Fig. 4.4

Figure 4.6: Monte Carlo simulation results with device mismatch in different process corners.

Figure 4.4 is guaranteed to be driven to the reference drain voltage value. Further, the voltage follower arrangement isolates the drain reference voltage, from the actual drains of the input NMOS devices.
CHAPTER 4. PROPOSED OUTPUT DRIVER CALIBRATION FOR LVSTL

Voltage output of the process sensor from Monte Carlo simulations are presented in Figure 4.6. The iteration is a hundred times in each process corners (SSS, SFT, SFS, SFF, TTT, FFF, FST, FSS, and FSF). The waveforms are separated in three groups. First, the group in the top of the plot, nMOSFETs are in slow corner. The waveform group in the bottom of the plot is in fast corner, and typical corner nMOSFETs are congregated in the middle group. Clearly, the output voltage of the sensor shows 70-73mV gap between different corners, and it is also significantly not affected by PMOS corners. In addition, it shows flatten slopes in supply voltage variations. The nominal supply voltage is 1.8V.

4.2.3 Temperature-Monitoring Sensor Design

Among various device parameters in semiconductor technologies, the characteristics of bipolar transistors have proven the most reproducible and well-defined quantities that can provide positive and negative temperature coefficients (TCs). Even though many parameters of MOS devices have been considered for the task of reference generation [44,45], bipolar operation still forms the core of such circuits [46]. While virtually every device has temperature-dependent characteristics, bipolar transistors are particularly suitable for generating the signal [47]. In the standard CMOS process, substrate bipolar transistors can be used for generating proportional to absolute temperature (PTAT) device accurately.

The base-emitter voltage $V_{BE}$ of a BJT in its forward-active region can be described by the following well-known equation:

$$V_{BE}(T) = \frac{kT}{q} \ln \left( \frac{I_{bias}(T)}{I_S(T)} \right)$$  \hspace{1cm} (4.3)

where $kT/q$ is the thermal voltage ($V_T$), $I_S$ is the BJT’s saturation current and $I_{bias}$ is its
collector current \([48]\). As a result of the temperature dependency, the thermal voltage has a positive temperature coefficient of about 2mV/C.

The temperature sensor shown in Figure 4.7 is composed of start-up circuit, proportional to absolute temperature (PTAT) current generation circuit, and temperature dependent voltage output. The output voltage is obtained as

\[
V_{R1} = V_{BE1} - V_{BE2} = V_T \ln n,
\]

\[
V_{out} = \frac{R_2}{R_1} V_T \ln n
\]  

(4.4)

The difference in \(V_{BE}\), \(\Delta V_{BE}\), is depends on the ratio \(n\) as described in \(4.5\). A larger ratio results in a larger \(\Delta V_{BE}\), but care has to be taken to ensure that both transistors remain in
CHAPTER 4. PROPOSED OUTPUT DRIVER CALIBRATION FOR LVSTL

\[ \Delta V_{BE}(T) = \frac{kT}{q} ln(n) \] (4.5)

From the current curve in Figure 4.8, there exists another stable operating point with all currents equal zero besides the desired operating point. On the left part of the schematic in Figure includes the start-up circuit to prevent from entering the unwanted operation of the self-biased circuit.

The output voltage of the temperature-monitoring sensor is displayed in Figure 4.9 under slow/typical/fast process corners and temperature range of -20 C to 120 C. The result shows that the output has a good linearity in the operation range and it is insensitive to process variations.

The temperature-monitoring sensor in Figure 4.7 consumes large die area due to the BJTs, Q1 and Q2. Moreover, the output is not stable with supply voltage variation. The reference current generated in the schematic of the temperature sensor II shown in Figure 4.10 is

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Figure 4.9: Output voltage of the temperature-monitoring circuit I with process variations. Designed as independent of supply voltage. The reference current can be written as \[ I_{REF} = \frac{1}{2R^2KPnW_0/L_0} \] (4.6)

Similar to the design I, it composed with start-up circuit, current generation circuit, temperature sensing circuit, and output driver. Instead of increasing area of BJTs, control the current on PM3 and PM4 that makes the difference in VBE, \( \Delta V_{BE} \), same as in equation (4.5). The \( \Delta V_{BE} \) is amplified through the differential amplifier in output stage. To achieve high temperature to voltage sensitivity, the gain of the differential amplifier can be increased. The output voltage graphs of the temperature sensor design with process variation are shown in Figure 4.11. Gap between the different process corner cases are reduced from the previous design.

In Figure 4.12, the supply voltage values are swept from 0.9 V to 2.0 V. The graph is slightly deviated from group when the supply voltage is 0.9 V at low temperature range, and
Figure 4.10: Temperature-monitoring sensor design II.

Figure 4.11: Output of the temperature-monitoring sensor II with process variations.

the other cases show uniform outputs.
4.2.4 Effective Distance for Temperature Sensors

Since the thermal coupling with the low power DRAM devices are tight, hot spots on an SOC can induce thermal gradients across the LPDDR4 device. As these hot spots may not be located near the device thermal sensor, the devices temperature compensated self-refresh circuit may not generate enough refresh cycles to guarantee memory retention [14]. In an integrated system, the electrothermal coupling effects from circuits further than 150μm away from circuit under test (CUT) are attenuated by more than one order of magnitude, but their impacts can be accounted for by injecting their power dissipations as currents into the extended RC grid [50]. Therefore, the distance between sensor locations are determined as four DQ pads in this design.
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4.2.5 Analog-to-Digital Converter (ADC) Design

ADC circuit is designed between the analog sensor outputs and digital codes for pre-drivers. As a part of the calibration system, power and area overhead of the ADC has to be minimized. The resolution of the ADC is determined according to the combinational complexity of the calibration codes. Consequently, a flash type data converter is suitable in the on-chip calibration system due to its simplicity and speed of conversion, especially in the small number of bit data conversion. The schematic of the ADC in calibration system is illustrated in Figure 4.13 and its input/output waveforms are displayed. The input voltage range is divided into three regions through the ADC; region 1 is low temperature where the temperature from sensor is between -20C to 10C, region 2 is medium temperature range which corresponds to temperature between 10C to 70C, and finally region 3 is high temperature range.
A
mplitude [V]

T
ime [s]

IN [V] OUT [V]

Figure 4.14: Comparator output waveform without hysteresis

The output waveform shows hysteresis characteristics. Noise or signal variation at the comparison threshold will cause multiple transitions as shown in Figure 4.14. Also, the temperature-monitoring circuit generates the input signal of the flash ADC in the calibration circuit. As the chip temperature changes continuously and noise is added on it, the comparator should have the hysteresis to increase noise immunity and stability. The output of the temperature monitoring sensor has a sensitivity of 2mV/C. From the waveform in Figure 4.13, the hysteresis band is design as 14mV which is correspondence to 7C degree of temperature variation without other noise. Which prevents from fluctuating at the edge of decision point.

The schematic of comparator with internal hysteresis design is illustrated in Figure 4.15. The transistor NM1, NM4, PM2, PM4, and PM5 compose fundamental structure of comparator and the hysteresis voltage is introduced by NM2 and NM3. When $V_{INP}$ is much higher than $V_{INN}$ and the output is in logic ‘0’, NM1 and NM2 are off, and bias current
CHAPTER 4. PROPOSED OUTPUT DRIVER CALIBRATION FOR LVSTL

Figure 4.15: Schematic of comparator with internal hysteresis for flash ADC

$I_{BIAS}$ flows through NM3 and NM4 to ground. The output transition from logic low to high happens when $V_{INP}$ gradually reduces to the potential lower than $V_{INN}$, and $I_{BIAS}$ also flows through NM1 and NM2, until $V_{INP}$ equals to the lower trip point. At this point, NM1 and NM2 are turned on, and NM3 and NM4 are off. The trip point is given as [51]

$$V_{TRIP_{\pm}} = V_{INN} \pm \sqrt{\frac{2I_{BIAS}}{\mu_n C_{ox} (W/L)_{P4,5}}} \times \frac{\sqrt{k} - 1}{\sqrt{k} + 1}$$  \hspace{1cm} (4.7)

where $k$ is ratio between NM1, NM4 to NM2, NM3.

4.2.6 Output Driver Optimization Technique

Schematic of a generic NMOS-only output driver is shown in Figure 4.16, which is a simplified version to verify the functionality of the proposed calibration method. The basic slice is composed of an array to tune the impedance of the pull-up driver and the pull-down driver to 480 $\Omega$ and 240 $\Omega$, respectively. To satisfy the multiple output current driving
An area efficient design of the DRAM output driver is proposed in Figure 4.17. While the conventional transmitter uses 12 series resistors for six slices as shown in Figure 4.16, the proposed scheme uses only 6 series resistors because six slices share the resistors. The series resistors are connected to two different transistor arrays, the first array (shaded) can be tuned to 440 $\Omega$ and the latter array (light color) is used to tune to $1100/3 \ \Omega$ for the pull-up network. Likewise, the pull-down network is designed to set 200 $\Omega$ and $400/3 \ \Omega$ for the shaded and light array, respectively. Since the series resistors still hold all the paths from pull-up arrays and pull-down arrays, the linearity is not degenerated as well. Total area is reduced by 50% from $3461 \mu m^2$ to $1620 \mu m^2$ when the proposed design is compared to the conventional one.
in the 0.18\textmu m CMOS process. The silicon area for resistors are significantly reduced while the area increase for the array is minimal. If the following criteria is satisfied, the proposed output driver design takes

\[(\alpha - 1) \leq \frac{1}{2} \cdot \frac{A_{RC}}{A_{TC}} \tag{4.8}\]

where \(\alpha\) is ratio of the total transistor width of the conventional approach and the total transistor width of the proposed approach, \(A_{RC}\) is the total area of series resistor in conventional design, and \(A_{TC}\) is the total transistor width in conventional design. Designing
CHAPTER 4. PROPOSED OUTPUT DRIVER CALIBRATION FOR LVSTL

Table 4.1: Area comparison of output driver

<table>
<thead>
<tr>
<th>Sheet resistivity (max/min)</th>
<th>$R_{ESD}$ area (40 Ω)</th>
<th>W</th>
<th>$\alpha_{max}$</th>
<th>ΔArea</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 (+150%)</td>
<td>306 µm²</td>
<td>228 µm²</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>7 (+115%)</td>
<td>264 µm²</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>83 (±10%)</td>
<td>3020 µm²</td>
<td>228 µm²</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Shared-$R_{ESD}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 (+150%)</td>
<td>153 µm²</td>
<td>324 µm²</td>
<td>7.4</td>
<td>40%</td>
</tr>
<tr>
<td>7 (+115%)</td>
<td>132 µm²</td>
<td>324 µm²</td>
<td>6.4</td>
<td>38%</td>
</tr>
<tr>
<td>83 (±10%)</td>
<td>1510 µm²</td>
<td>324 µm²</td>
<td>76</td>
<td>50%</td>
</tr>
</tbody>
</table>

in Figure 4.17, $A_{RC}$ is 3120µm² and $A_{TC}$ is 41µm². That is, the proposed approach has area-saving advantage until $\alpha$ is smaller than 76. In actual design, $\alpha$ is obtained as 1.4.

Area comparison with conventional design and proposed shared ESD resistor is found in Table 4.1. The comparison covers with different types of resistors. In the tape-out process design kit, the proposed output driver is effective with all of the resistors, and we chose one that has minimum variation.

Simulation data of the proposed shared-resistor output driver design are displayed in Figure 4.18. The VOH values at DQ pin are compared after the impedance calibration processes under different conditions including supply voltage, temperature, and termination impedance. Even though the proposed calibration method does not consider supply voltage variation, the output signal swing errors are within allowable range (±10%) as displayed in Figure 4.18(a). The steep changes of VOH in Figure 4.18(b) are due to the calibration code updates at given temperature points. Additional calibration steps can be added to reduce the steepness and get higher accuracy with extra bits of calibration codes.

In Figure 4.19, the VOH values after calibration at six different device mismatches and process variation conditions are displayed. Total 1.8K times Monte-Carlo simulation
data with local and global mismatch statistics is shown with three different terminations (40/48/120 Ω). More than 95% of the cases fall into right target specification.

The proposed design is implemented and demonstrated using an 0.18μm standard CMOS process technology. The circuit simulation set-up is shown in Figure 4.3 and the channel between DRAM and controller is modeled as a 3-inch RLGC model and pad/package parasites are also modeled. The clock frequency is 800MHz, which corresponds to technology scaling from standard LPDDR4 speed. The results of the impedance calibration are evaluated as VOH level measurements. Figure 4.20 shows eye-diagrams of the transmitter outputs after the proposed impedance calibration process. The supply voltage is 1.8V, and
the target voltage level of output logic high is 600mV. For the six different termination cases (40/48/60/80/120/240 Ω), the deviation from the specifications is less than 20mV.

In Figure 4.21, rising and falling switching of the post-layout simulation of transmitter output driver under various impedance values (40/48/60/80/120/240 ohm) are shown. The simulation set-up includes other on-chip elements such as PAD and ESD circuits, and also evaluates off-chip parameters. That is, the parasitic values are extracted at worst case condition, including RC, coupling capacitor, self-inductance, and mutual inductance. Also, the simulation environment includes chip package parasitic values from low quad flat package (LQFP), which is not suitable for high speed operation circuit. The data rate is 200Mbps due to the high package parasitic values and high capacitance on ESD circuits.
CHAPTER 4. PROPOSED OUTPUT DRIVER CALIBRATION FOR LVSTL

Figure 4.20: Eye diagrams with different termination values after calibration at 1.6Gbps, typical corner, room temperature [42]

Figure 4.21: Post-layout simulation of transmitter output driver.
Chapter 5

Experimental Results

The proposed transceiver design was implemented in a 0.18\( \mu \text{m} \) CMOS process with diffusion resistors that has \( \pm 15\% \) of absolute accuracy at 1.8V of supply voltage. Figure 5.1 illustrates a transceiver circuit test with the proposed impedance calibration. The input data signals are selected from external data or from internal pseudo random bit sequence (PRBS) circuit after serializer. The pre-driver receives the processed driver calibration codes

![Diagram of transceiver circuit with transmitter calibration test using PRBS and Checker](image)

Figure 5.1: Transceiver circuit with transmitter calibration test using PRBS and Checker
CHAPTER 5. EXPERIMENTAL RESULTS

from local sensors. Throughout the output driver on DQ pins, the data is transmitted to receiver, where termination resistances are set one of (40/48/60/80/120/240 Ω) depends on each applications. Also, the 6-bit ZQS code controls the number of parallel arrays of the output diver corresponding to the termination resistance. Regenerated signal through the Rx on receiver-end is deserialized and check the data with error detection code.

The chip micro-photograph is shown in Fig. 5.2 where the proposed transmitter design is located on top with the calibration circuits. The transmitter calibration circuit includes process sensor, temperature sensor, ADCs, decoders, and current source are shown in Figure 5.2(a). Also, PRBS 9 and error checker circuit, and SerDes circuit as a test circuit is shown in Figure 5.2(b). The implemented circuits occupy 0.486 mm² including decoupling capacitors.

Test boards are fabricated to measure the proposed circuit characteristics and behavior, and it is shown in Figure 5.3 Chip socket is embedded on the board to collect measurement data from each fabricated chip as shown in Figure 5.3(a). Performance of temperature sensor, process sensor, ring oscillator, and other circuits is measured with chip to chip variation data. The socket is not proper to test high speed operations due to its high capacitive loads. The transceiver test with on board channel is performed a board in Figure 5.3(b).

The outputs of the analog parts composed in the calibration circuit directly cannot be measured, because analog output node is affected by output conditions. Therefore, the sensor operation is observed by measuring duplicated sensors, which is shown in Figure 5.2(a). Figure 5.4(a) shows the measured data of the output of the voltage temperature monitoring circuit with simulated data. The gap between the post-layout simulation results and measured
data is due to difference between the ambient temperature and the junction temperature. While the ambient temperature is easy to measure, the junction temperature is very difficult to measure. Therefore, the chip junction temperature is obtained from the following equation

\[ T_J = T_A + \theta_{JA} \cdot P_D \]  \hspace{1cm} (5.1)

where \( T_A \) is ambient temperature for the package, \( \theta_{JA} \) is junction to ambient thermal resistance, and \( P_D \) is power dissipation in package \[52\]. The process corner detection results are shown in Figure 5.4(b), where output voltages of the process sensor circuit on each chip are summarized. Due to the limited number of sample chips, it is not possible to present
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Figure 5.3: Print circuit boards to test multi-chip statistics and transceiver test through on-board channel.

Figure 5.4: Measured temperature monitoring sensor and statistics of process sensor output
CHAPTER 5. EXPERIMENTAL RESULTS

Table 5.1: Post-layout simulation for process variation sensing

<table>
<thead>
<tr>
<th>Corner</th>
<th>Temp.[C]</th>
<th>$f_{OSC}$ [MHz]</th>
<th>$f/8_{OSC}$ [MHz]</th>
<th>$f/16_{OSC}$ [MHz]</th>
<th>Sensor Out [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast / Fast</td>
<td>-50</td>
<td>841</td>
<td>105.2</td>
<td>52.6</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>703</td>
<td>87.9</td>
<td>43.9</td>
<td>625</td>
</tr>
<tr>
<td>Typical / Typical</td>
<td>-50</td>
<td>608</td>
<td>76.4</td>
<td>38.3</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>512</td>
<td>64.0</td>
<td>32.0</td>
<td>687</td>
</tr>
<tr>
<td>Slow / Slow</td>
<td>-50</td>
<td>444</td>
<td>55.5</td>
<td>27.7</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>372</td>
<td>46.5</td>
<td>23.2</td>
<td>757</td>
</tr>
</tbody>
</table>

enough data that are statistically meaningful. On-chip ring oscillator is designed to measure the process corner indirectly and the its output frequency is divided for easy measurements. The ring oscillator data is shown in Table 5.1. Voltage range between 620mV and 760mV in Figure 5.4 (b) indicates that the chip has been fabricated in typical process corner. Except for the chip #8 in the figure, all the data indicated that the process corner of the fabricated chips are in typical corner. This corresponds to the measured frequencies of on-chip ring oscillators.

As the data rates of state-of-the-art broadband circuits increase, these circuits outperform commercially available test equipment and verification of error-free operation becomes more challenging. Hence, custom circuits are needed to generate input data for testing purposes. [53] In serial interconnect technology, it is very common to use pseudo-random binary sequence (PRBS) patterns to test the robustness of links. [54] The circuit that generates or checks a PRBS sequence is based on a linear feedback shift registers (LFSR).

In Figure 5.1 there are PRBS and checker circuits for on-chip self-test. The parallel PRBS generator and detector design, which is shown Figure 5.5 is used. A procedure for translating into the PRBS generator schematic with parallel outputs is given in [55]. The flip-flops are connected as a parallel register with the output fed back to the input through
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Figure 5.5: PRBS9 8-bit parallel generation

Figure 5.6: PRBS7 8-bit parallel error detection circuit
CHAPTER 5. EXPERIMENTAL RESULTS

Figure 5.7: Post-layout results (a) Eye-diagram of Serializer output (b) Error detector output

The XOR gates. The XOR gates are connected so each bit of the new word is generated according to a given polynomial equation.

To transmit the PRBS signal, 8-to-1 multiplexer is used. Also, the error detection configuration is shown in Figure 5.6. Each of the eight consecutive data from PRBS9 parallel generator are used as a set to check error, which are all known values. The serial data are XOR-ed, thus error detection signal generates zero, if they are identical after the combinational logic. If one of data has error, it will generate error signal. The serialized PRBS signals are shown in Figure 5.7 as a post-layout simulation result. An eye-diagram is shown in Figure 5.7(a) with its jitter histogram from post-layout simulation. The clock frequency used in this test is 400MHz. The maximum jitter is 23ps and no error signal is received after initialization.

The eye diagrams of transmitter signals are shown in Figure 5.8. The all the VOH values are in the VDDQ/3±10% range.
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Figure 5.8: Measured eye diagrams with multiple termination values
Chapter 6

Proposed Receiver Designs

Input buffer in DRAM converts attenuated signal to rail-to-rail signal. In conventional designs, differential input buffer is used for high-speed and low power operation. However, in high frequency operation with low VOH, channel loss increased that caused by skin effects, dielectric losses and reflections on PCB traces. The channel loss and ISI affects significantly on correct data transmission even in short channels [56–58]. Moreover, as the voltage swing is lower and lower to reduce power consumption and increased data speed, the data eye opening is not enough to use the conventional input buffers. As a result, advanced receiver design is required over the conventional input buffer to improve signal integrity and meet the data transfer speed.

In this chapter, low-common mode input sense amplifier design is introduced with adaptive gain control (AGC) feature to optimize the performance and reduce power consumption. Next, a high-speed receiver equalizer design and simulation results of the architecture are introduced. Linear equalization technique is applied in data receiver stages to com-
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Figure 6.1: Schematic of the proposed receiver design. (a) Schematic of the PMOS-input sense amplifier (b) Schematic of the PMOS-input sense amplifier with an automatic gain control

pensate completely closed eye of received signal and recover the data. A system level design overview is given such as circuit designs and description of the CTLE and DFE line equalizations.

6.1 Low-Common Mode Input Sense Amplifier

According to the convention of the LVSTL signaling, the input common mode on receiver is significantly decreased to one-sixth of the supply voltage. Therefore, it is more efficient to design sense amplifier with PMOS input considering the input common mode range to enhance sensitivity and detect incoming signal through transmission line as shown in Figure 6.1(a). In this design, one of the output nodes (Q or QB) is charged during the evaluation phase, while both nodes are discharged in reset phase. Furthermore, the reference
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voltage (VREF) is lowered than the conventional NMOS input sense amplifiers, and the gain of the input transistor is more important. The total delay of the voltage sense amplifier can be expressed as

\[
t_{\text{delay}} = \frac{2C_L V_{tn}}{I_{\text{tail}}} + \frac{C_L g_m}{V_{tn}} \left\{ \frac{1}{V_{tn}} \sqrt{\frac{I_{\text{tail}}}{2\beta} \Delta V_{\text{out}}} \right\}
\]

where \(I_{\text{tail}}\) is the bias current and \(\beta\) refers \(\mu_n C_{\text{ox}} W/L\) [59]. The operation speed is strongly proportional to the tail current and transconductance of the input transistors from (6.1). Also, the delay is proportional to threshold voltage that is a major parameter of process variation as shown in the equation. Considering the relationships and trade-offs among the design parameters, performance, and the impact of process variation on performance, an adaptive gain control (AGC) voltage sense amplifier is proposed as depicted in Figure 6.1(b). The input and tail transistors are designed as digitally controlled 2-bit arrays, which is a viable solution using AGC to optimize the performance against process variations and to achieve low power consumption as well. The input control signal is delivered from the process sensor utilized in transmitter impedance calibration circuit.

The simulated performance metrics of the proposed low common-mode adaptively gain controlled sense amplifier design are shown in Figure 6.2 at each process corner. The sense amplifier operates in either high-performance mode or low-power mode. The delay and average power consumption in the two operation modes are compared with the conventional design that uses a single transistor with the same size as the maximum case’s (all transistors in the array are turned on) in the proposed one. For the slow corner case, the receiver always operates as high-performance mode, and low-power operation is not supported. Due to the increased loading on input nodes of additional switches, there are slightly increased delays.
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Figure 6.2: Simulated performance metrics of automatic gain controlled sense amplifier: delay time and average power consumption.

on the high-performance mode compared to the design without AGC. The input signals are generated from the proposed transmitter circuit with 600mV VOH value at 2Gbps speed at 0.18\(\mu m\) CMOS technology. The pseudo random input bits are composed of even number of logic HIGHs and LOWs. The power consumption is reduced as much as 15-20% from the design without AGC when the receiver is in low-power mode.

The \(t_{CK-Q}\) values are optimized to cover the worst case process condition. Therefore, the delays in best to typical cases are close to the worst case performance in low-power mode. The slave latch followed by sense-amplifier is shown in Figure 6.3 where the SR latch is modified from [60] because the input transistors of the sense amplifier should be PMOS due to the low common mode input voltage and SR latch truth table needs to be
corrected. To improve the performance of the slave latch, the source node voltage of NMOS transistor is adjusted to increase the threshold voltage of the inverter by applying the control voltage. The voltage is connected from resistor ladder, and the connection switches are controlled by ADC output followed by process sensor. The increased threshold voltage improves $t_{CK-Q}$ from fast pull-down of the inverter and reduces decision time.

Performance measurement data of the receiver circuit is shown in Figure 6.4. The AGC feature is not included in this design. The measured $t_{CK-Q}$ delay values are less than 500ps when the supply voltage is higher than 1.5V, and the delay exponentially increases as the supply voltage decreases under 1.5V. Also, from Figure 6.4(b), the $t_{CK-Q}$ is measured less than 500ps when the input amplitude is higher than 460mV.
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Figure 6.4: Performance measurement of PMOS input sense amplifier design (a) Delay time at supply voltage sweep (b) Delay time with different VOH level

6.2 Equalizer Design

The low common mode input sense amplifier introduced in previous section is an effective input buffer. However, it cannot recover data from completely closed eye from eye-diagram. Therefore, special circuitry is required to achieve low BER.

A common form of equalization is the decision feedback equalizer (DFE) which operates by subtracting the ISI arising from previously detected data symbols from the symbol currently being received. The DFE is suitable to the receive equalizer function as the slicer nonlinearity allows it to amplify the recovered signal while rejecting noise [61]. However, DFE alone is also not a complete solution for equalization, because it cannot eliminate precursor ISI. Therefore, a receiver architecture consisted of a continuous-time linear equalizer (CTLE) followed by one-tap decision feedback equalizer is often used for
lossy channels [62].

However, the linear equalizer amplifies crosstalk noise. Even though, purpose of linear equalizer design is signal boosting and provide sufficient eye-opening to DFE stage. Inherit of its high-pass filter characteristics, additional nonlinear equalization such as DFE is essential. The nonlinear equalizers generate sharp notches in the channel due to impedance discontinuities and also avoid the amplification of crosstalk due to high-frequency peaking [63].

### 6.3 Equalizer Classification

In order to decide which topology is adequate for equalizer design with the specification and environment, each of advantages and challenges are analysed. In this chapter, most common equalizer topologies are classified and discussed.

The most common equalization technique on receiver stage is the DFE [64–69], which is preferred over linear equalization for compensate high-loss channels. The DFE is suitable to the receive equalizer function as the slicer nonlinearity allows it to amplify the recovered signal while rejecting noise. In contrary, CTLE has a drawback that amplifies noise and crosstalk along with desired signal. However, DFE itself is not an complete solution for equalization, because it cannot eliminate precursor ISI. Therefore, single stage of CTLE is preceding to DFE for solid equalization with the combination of those two architectures.
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6.3.1 Continuous Time Linear Equalizer

In order to compensate the channel loss, both of the pre-cursor and post-cursor ISI can be cancelled using the linear equalizer. The compensation can be realized as implementation of a high-pass transfer function.

The linear equalizer is designed to extend bandwidth by cancelling the first pole in the channel. In Figure 6.5, the transfer function of the CTLE is visualized. The pole cancellation increases bandwidth, also boosts gain at the high frequency by creating a zero at low frequency then poles. The bandwidth is specified according to data rate which is constrained by Nyquist bandwidth.

The active CTLE can boost high frequency by means of real zeros trade off DC loss with capacitive degeneration method. The implementation of differential pair with resistive load is shown in Figure 6.6. The transfer function of the active CTLE is

\[ H(s) = g_m \frac{s + \frac{1}{R_s C_s}}{C_p \left( s + \frac{1+g_m R_s/2}{R_s C_s} \right) \left( s + \frac{1}{R_D C_p} \right) }. \] (6.2)
At low frequency, the capacitor $C_s$ acts as an open circuit, and the source degeneration resistor $R_s$ is dominant effect to the gain of the equalizer. Which is corresponding to the DC gain:

$$DC\text{gain} = \frac{g_m R_D}{1 + (g_m + g_m b) R_s / 2}. \quad (6.3)$$

Similarly, at high frequency, the impedance of $C_s$ is low enough to act as a short circuit, and according that high frequency gain can be achieved. In addition, the location of one zero and two poles are give as

$$\omega_z = \frac{1}{R_s C_s}, \quad (6.4)$$

$$\omega_{p1} = (1 + \frac{(g_m + g_m b) R_s}{2}) \frac{1}{R_s C_s}, \quad (6.5)$$

$$\omega_{p2} = \frac{1}{R_D C_p} \quad (6.6)$$
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Here, $C_p$ includes parasitic capacitance of output node and total input capacitance of next stage.

The ideal peak gain is

$$g_mR_D$$  \hspace{1cm} (6.7)

The active CTLE has gain boosting at Nyquist frequency so as to compensate channel loss in high frequency range with lower power and area. The capacitor $C_s$ provides the high frequency boosting because of . The boosting property and good linearity of the source degeneration structure depict that the CTLE is a good candidate for equalizer. However, it also amplifies undesired signals such as high frequency noise and cross-talk. In addition, vulnerability to PVT variations of the CTLE undermines its usage on increasing data rate and IC technology scaling.

6.3.2 Discrete Time Linear Equalizers

While the linear equalizer can be easily implemented, there are few drawbacks such as amplifying high frequency noise along with desired signals, limiting to compensate non-linear distortions. In addition, ISI arisen from impedance mismatches, offset, cross-talk, or parasitic poles/zeros from package parasitics cannot be compensated as well. Inherit of its high-pass filter characteristics, additional non-linear equalization is essential and the decision feedback equalizer (DFE) is widely used in that purpose. The non-linear equalizers generate sharp notches in the channel due to impedance discontinuities and also avoid the amplification of cross-talk due to high-frequency peaking [63]. Several topologies are proposed to improve performance of the DFE architecture. In this section,
some of the topologies, which are widely used, will be reviewed with their superiorities and disadvantages in various points of view in design aspects.

6.3.2.1 Direct Feedback DFE

One possible approach to design a DFE is the direct feedback architecture \([71-74]\) in Figure 6.8. It is operated as a half-baud-rate receiver, where the two slicers sample data at each of the clock edges. The summer should have enough bandwidth to process addition of the tap values in time. In this topology, data must be resolved and fed back in 1 unit interval (UI). Even though this topology has an advantage of power consumption, because it uses
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Figure 6.8: ADC based DFE architecture [75]

less slicer counts than loop unrolling technique, the speed is limited due to the critical path timing issue.

6.3.2.2 ADC based DFE

The analog-to-digital converter (ADC) and digital signal processing (DSP) incorporated DFE architecture has robustness on equalization to channel [76 77]. The digital signal processing can be advantageous in that it is less sensitive than analog circuitry to process, voltage and temperature variations, is highly programmable, and scales well with CMOS process advances [76]. However, high specification ADCs are required to achieve very high sampling rate using sophisticated techniques such as parallelization or interleaving [78 79]. In addition, the use of ADC with high frequency operation is inevitable consumption of high power. Moreover, the performance of equalization is dependent and limited to the speed and resolution of the ADC. An ADC sampling frequency equal to the symbol rate is needed for muti-giga-bit-per-second data transmission. A higher resolution is needed for ISI compensation by any subsequent digital equalizers. The required number of bits of resolution depends on the channel characteristics [75]. A limited bandwidth of the ADC would appear
Fig. 6. Timing diagram of (a) direct DFE; (b) simplified version of proposed DFE.

Fig. 6(a) shows the timing diagram of a direct-feedback DFE to illustrate the comparison. In a direct-feedback DFE, a decision is made only at the edge of the clock. In contrast, the S/H in our proposed DFE extends the available time period for a decision to the hold time of the S/H. While a hard decision is still made at the latching transition, the latch provides the information for subtracting ISI 1 bit time earlier.

The improved critical path from the soft-decision architecture is even more dramatic when interleaving by 4 and using sampling clocks with skewed duty cycle. Fig. 7 shows the implementation of our 2-tap DFE used in a test chip. The four S/Hs are triggered by clocks with phases separated by 1 bit-time. Each clock has 25% duty cycle. The clocks are created by the NOR of two 90° shifted 50% duty-cycle clocks. The skewed duty cycle allows the S/H to hold the data for 3/4 of the cycle or 3 bit-times. As shown in Fig. 8, the longer hold period extends the period for soft decisions. The clock used for the latches are still 50% duty cycle so that the data at the output of the latch is held for 2 bit-times. By holding the data for 2 bit-times, the decision can be applied to two subsequent paths forming two parallel 2-tap DFEs. The highlighted traces in Fig. 7 illustrate that two soft decisions are calculated simultaneously when and are HIGH.

Fig. 8 highlights the third interleave path (OUT3) of Fig. 7 to illustrate the operation. The third S/H is clocked by the clock phase . The outputs of the latches from both of the previous paths, and, are summed by the adder to produce . In the first bit time (first), of the hold period, the data from both previous paths are soft decisions so and are added in the signal . In the second bit time (second), the value from the first path, becomes a hard decision, , due to the latching edge of . And in the last bit time (third) of the second path becomes a hard decision, . The latch output makes a soft decision in the second and third bit-times and passes the partial result to the fourth and first paths. Finally, a hard decision is made at the end of the hold period of the S/H.

Figure 6.9: Direct feedback with soft decision DFE architecture with 4-way interleaving [83] as a low-pass filter that would result in more ISI and thus is undesirable [80–82].

6.3.2.3 Soft DFE

A direct implementation of the DFE structure requires high-speed and low-fanout circuits in order to meet the timing requirement. The soft DFE is a developed version of the direct feedback DFE to improve critical path timing using interleaving paths. In the operation from simplified block diagram of soft DFE in Figure 6.9, the sample and hold (S/H) is placed to hold the analog value of the input signal. In the next phase, the latch behaves as a low-gain amplifier that passes the output of the S/H. The output of the latch is fed to the delay line of the feedback filter of a subsequent phase and summed. Because the latch is passing an amplified version of the input signal, the information being fed back is a “soft” decision. The soft decision DFE not only relaxes the critical path of direct feedback DFE, also suitable
for lower power I/O link application in a short channel [83–85].

6.3.2.4 IIR-DFE

A multiple-tap DFE is adopted to compensate the ISI, which is induced by postcursors due to the non-ideal channel impulse responses. To avoid the power and area penalty due to the many postcursors, a DFE with infinite impulse response (IIR) filter feedback has been presented. The generic diagram of the IIR-DFE architecture with K-taps and N-filters is in Figure 6.10. A continuous-time tap can be created using an (IIR) filter in the DFE. This approach allows several post-cursor ISI taps to be cancelled simultaneously with reduced power consumption. With respect to the power and area advantage, it is currently being studied because of the high performance and suitable for high channel losses. The channel
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Figure 6.11: 5-tap FIR-DFE structure \[91\]

needs to be smooth, that is reflections should not be serious, for proper functioning \[86-90\].

6.3.2.5 FIR Equalization

Figure [6.11] shows the block diagram of FIR equalization with 5-tap structure. The finite impulse response (FIR) filter based equalization is suitable for high performance and high channel losses for long channel. It is possible to cancel both pre-cursor and post-cursor ISI. However, it cannot avoid noise and crosstalk amplification from the inherent property. Solve the system stability issue could be challenging. In addition, implementation of the analog delay cells, denoted as \( z^{-1} \) in Figure 6.11 is challenging. Because the delay cells should provide a constant group delay and magnitude response over the bandwidth of the data. Tap precision significantly affects to equalization performance as well \[76,91,93\].
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Instead of feeding back the slicer decision for the first tap, a look-ahead DFE makes two decisions with two slicers where each slicer assumes the previous bit is a 0 and 1 as illustrated in Figure 6.12. The received data value is selected from these two slicer outputs based on the previous data value with a multiplexer.

The look-ahead technique is typically limited to only one tap because of an exponential increase in the number of slicers with the number of taps. The speculative method for two taps requires additional two multiplexers and four slicers. Moreover, the count would be doubled for half rate sampling. As a result, the second and higher order taps of the DFE are often fed back directly. With the loop unrolling technique, the critical path timing is relaxed for the first tap, which is most critical path. However, the second-tap feedback still results in a timing constraint [94–98].

Because of the robustness, the speculative DFE is the most commonly used architecture. The basic structure from this equalizer is adopted in this thesis.

Figure 6.12: 1-tap speculative DFE [94]
6.4 CTLE Design for LVSTL Signaling

The continuous time linear equalizer is introduced as shown in previous chapter. In addition that, more detailed implementation consideration and analysis is described in this section. The equalizer filter must provide sufficient gain boosting around bandwidth so as to equalize the signal spectrum. To do that, the CTLE circuit should satisfy certain requirements such as matching the inverse loss profile of the channel with reasonable tolerance, high characteristic of linearity so that the equalizer transfer function indeed acts as the inverse of the channel loss profile [63]. In addition, small input and output capacitance which are dominant factor for pole locations and high frequency design challenge. Due to the low input common mode in LVSTL, another purpose in CTLE circuit is to change the
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common mode voltage.

A conventional capacitively degenerated differential amplifier design and its DC gain control in frequency response are shown in Figure 6.13. From the equation (6.6), the second pole location is limited by the load capacitance of the linear equalizer, which is the drain capacitance of the CTLE, total input capacitances of next stage, and wire capacitance. The load resistor, $R_D$, is defined by current and output biasing. Next, the current value and average power dissipation are defined. By setting the peak gain from the equation (6.7), the $g_m$ of PM1 and PM2 value can be optimized.

The linear equalizer is designed to provide a boost factor of 5dB at the Nyquist frequency and low-frequency loss from 0dB to -6dB with a DC gain control by source degeneration resistance, $R_s$, that allows a wide range of transmitter amplitudes while maintaining proper linear operating range for the remainder of the receiver data path. The single stage CTLE increases eye height to support decision in samplers, but it cannot provide enough gain to recover symbols, also boosts high frequency noises.

6.4.1 Performance Analysis

The transition frequency characteristics of pMOSFET is displayed in Figure 6.14. The input voltage swing is 0.3V to ground and common mode voltage is 0.15V. Biasing current value also verifies at operation frequency range.

Figure 6.15 shows the gain and phase response at typical process corner. The well-behaved phase response should be analyzed to achieve a low jitter. In Figure 6.16, the gain plots of the CTLE from AC simulation results are shown. Different sets of source
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Figure 6.14: Transition frequency characteristics of pMOSFET in 45nm CMOS technology degeneration resistor and capacitor values are tuned to optimize. A plot has lowest DC gain is simulated at fast corner, the worst case corner simulation, which is in tunable range. The peak gain at the Nyquist frequency is between 5.5 dB and 6.2 dB. In Figure 6.17, frequency response of the continuous-time linear equalizer with Cs variation is displayed. The capacitance is inversely proportional to zero and the first pole frequency. Therefore, in the fixed bandwidth, $f_{p2}$, the peak frequency and the peak gain are also affected. Frequency response of the continuous-time linear equalizer with Rs variation is shown in Figure 6.18. The source degeneration resistor value is dominant to decide low frequency gain, and not affected to peak frequency and its gain.

In Figure 6.19, transient waveform of differential signal in receiver stage are displayed before equalization and after linear equalizer. Figure 6.20 is eye diagram of signals before
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Figure 6.15: AC simulation of the continuous-time linear equalizer: gain and phase response

Figure 6.16: AC simulation of the continuous-time linear equalizer (1) slow corner at 125C (2) typical corner at 25C (3) fast corner at 0C
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Figure 6.17: Frequency response of the continuous-time linear equalizer with Cs variation and after linear equalization. The transmitted signal after the channel shows completely close eye. The channel model corresponds to 6 inch long and 5 mil trace width microstrip line on 6-layer FR4 PCB line. After the linear equalization, the eye width is 144ps and eye height is 85mV opened. Also, the common mode voltage is shifted from 150mV to 500mV.
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Figure 6.19: Transient waveform of differential signal in receiver stage (a) before equalization (b) signal after linear equalizer

Figure 6.20: Eye diagram after channel loss and at CTLE output

The average power consumption is 1.67mW at 1V supply voltage.
6.5 Design of an Adaptive Decision Feedback Equalizer

Even if the CTLE stage amplifies the signal, the critical drawback is noise amplification. Instead of building multiple linear equalizer for higher gain, the next stage is composed as discrete equalizer, DFE. From the FR4 channel profile, the ISI shows 10% of the 1-st post cursor, and the other residual signal tail is negligible. Therefore, 1-tap DFE equalizer is designed in this section.

6.5.1 DFE System Design

The DFE compensates insufficient gain of the CTLE and eliminates residual post-cursor of ISI and unintended high frequency noise amplified at the linear equalizer. Figure 6.21 shows the 1-tap lookahead DFE with single-ended diagram for simplification, which operates
at half-rate clocking. In speculation, each (even and odd) path has decisions for both cases, in which the previous bit was a 1 and 0. A correct speculative path is chosen through a multiplexer and either adds or subtracts the feedback tap coefficient (H1) from the output signal of the preceding linear equalizer stage before a regeneration section in the sampler. The H1 feedback delay time is relaxed in the speculative design, because both possible events are calculated in advance at the cost of doubled device area for summation and decision paths.

In multi-giga bit rates DFE design, the primary challenge is feeding back the decisions quickly enough to implement the filter tap [70]. Therefore, the design of the DFE circuit has to be accompanied by critical path timing analysis to guarantee proper operation. In Figure 6.21, the critical timing path is the feedback signal from the mux output to the summer to settle signal in one unit interval (UI). The timing constraint of critical paths are expressed as

\[ t_{CK2Q,SA} + t_{pd,MUX} + t_{SETUP,ff} < 2UI \]

for the decision path and

\[ t_{CK2Q,ff} + t_{sum} + t_{SETUP,SA} < 1UI \]

for the feedback path where \( t_{CK2Q,SA} \) is clock-to-Q delay time of a sampler, \( t_{pd,MUX} \) is propagation delay of a mux, \( t_{SETUP,ff} \) is setup time of a D flip-flop and \( t_{sum} \) is delay time of a summer.

### 6.5.2 Sampler Circuit

The conventional latch design is the strong-arm latch in Figure 6.22. It uses single clock signal and low-power design. It has sampling noise and charge kickback from clock
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Figure 6.22: Strong-arm latch

Figure 6.23: Dummy switch for clock feedthrough alleviation

switching as illustrated in Figure 6.23.

The path selection multiplexers are designed as CMOS transmission gates. To improve critical path timing, one of the mux output is fed as a selection signal for the other one. Each of the four samplers, directly connected from the linear equalizer, has current injection paths from current digital-to-analog converters (IDACs). The current injection paths employ no other summer block to eliminate ISI from main cursor. To minimize glitches and mismatch,
the 6-bit IDACs are implemented as fully differential circuits. The currents, $I_{DP}$ and $I_{DN}$ in Figure 6.24, are mirrored from IDACP and IDACN, respectively, to ensure linear transfer characteristics for offset controls and the currents are injected to FB and FBB nodes, respectively. The P6a and P6b are turned on and off followed by CKB to prevent static operation. The current $I_{DP}$ and $I_{DN}$ are controlled by a binary weighted current-DAC.
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Figure 6.25: Optimized SR latch

circuit in Figure 6.26. The injected charges from $I_{DP}$ and $I_{DN}$ make the sampler as either a strong 1 or a strong 0 sampler. The 6-bit IDAC design and its output linearity are illustrated in Figure 6.26, where output offset of the sampler is controllable to 50mV. The equalization tap coefficient is adjusted by the sign-sign LMS (SS-LMS) algorithm [99–101].

In order to alleviate the kickback noise [102] from clock signal and minimize signal distortion impact from output to input nodes, the sampler in Figure 6.24 is designed as a modification from [103]. The N1a and N1b are used to isolate input pair from output nodes, also N3a and N3b isolate input pair from clock signal to reduce kickback noise. The cascode transistors block the reflection signals, also reduce voltage level from $V_{DD}$ to $V_{DD} - V_{DS}$, which reduce power consumption as well as increase decision speed. Because of the voltage reduction, the proposed sampler achieves 11% power reduction. Instead of $C_d$, parasitic
capacitance of differential amplifier pair at drain node, relatively small size of cascode pair can reduce the parasitic capacitance of the output node. Therefore, the discharging speed of the output nodes is improved. For the sampler operation, transistors N6 is turned off and reset transistor P2a and P2b charge both output nodes to supply voltage during reset phase. In the mean time, P1a and P1b are turned off and nodes FB and FBB are discharged. At the comparison phase, N3a and N3b are initially switched on. P3a is turned on before

Figure 6.26: 6-bit current DAC
Figure 6.27: Sampler output signal waveforms.

P3b and FB is pulled toward VDD while FBB remains near ground for sufficient input differential amplitude. Figure 6.27 shows the output signal waveforms of the proposed latch and conventional latch for comparison.

The positive edge triggered D flip-flop design used in DFE is shown in Figure 6.28. It is composed as master and slave latches, also contains clock and complementary clock buffers.
Figure 6.28: C\textsuperscript{2}MOS D flip-flop
6.6 Overall Architecture

Figure 6.29 illustrates a half-baud-rate receiver architecture which consists of a continuous-time linear equalizer, a 1-tap lookahead decision feedback equalizer with on-die termination, PLL and 2:8 deserializer for a pseudo-random bit sequence (PRBS) checker circuit. The receiver input, RX, is terminated to a regulated common-mode point through an on-chip 50Ω resistor. The low-impedance termination voltage provides better common-mode return loss over a wide frequency than a simple voltage divider solution [70].

To demonstrate real-time operation of the proposed receiver architecture, a channel loss model at 10 Gb/s using in transient simulation. The channel characteristic is shown in Figure 6.30, in which a 12-in board trace is included and the channel loss is 15-dB at the Nyquist frequency. As an input data pattern, $2^7 - 1$ PRBS7 is transmitted to the receiver stage at
5GHz clock frequency through the channel model. The rail-to-rail DFE output is connected to PRBS checker circuit with de-serialized signals at the 1/4 data rate. Same environment set up and transient simulation is repeated while clock phase is shifted to acquire pass/fail diagram.

Noise contribution of the devices is considered as injecting white noise and flicker noise sources in transient simulation, where the noise characteristics are extracted from each component properties. The bandwidth of a maximum pseudo-random noise is limited to 10 GHz. Simulation results data from worst case corner simulation and mismatch samples with transient noise simulation sweeps are performed.

### 6.6.1 PLL Design for Clock Distribution

The diagram of a phase-locked loop (PLL) is shown in Figure 6.31 which is designed as a conventional PLL architecture to generate 5GHz clock frequency. It is composed with
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Figure 6.31: PLL diagram

Figure 6.32: Phase frequency detector and charge pump
a phase-frequency detector (PFD), a charge pump (CP), a passive low-pass filter (LPF), voltage controlled oscillator (VCO), and a frequency divider. The phase-frequency detector and the charge pump are shown in Figure 6.32.

Figure 6.33: PLL frequency in transient simulation

Figure 6.34: PLL Jitter performance

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The PFD schematic is used as a widely implemented design, basically consisting of two positive-edge triggered D-flip flops. Each of the Q output enables a positive current source and negative current source, respectively. The transient simulation result in Figure 6.33 shows that frequency of the PLL is settled at 5GHz with noise and mismatch injections. The lock time is around 350 ns, and the overall jitter performance of a PLL which provides 5 GHz clock signal is shown in Figure 6.34, where the clock jitter is 12.62 ps from mismatch and noise contribution simulation analysis.

6.6.2 Simulation Results

Sub-figures in Figure 6.35 show the eye diagrams after the channel with 15 dB loss at the Nyquist frequency, CTLE output, and DFE output signals, respectively. The eye opening of the CTLE output eye diagram measured as 107 mV height and 68 ps width. The output signal of DFE shows rail-to-rail swing.

The pass/fail diagram from transient simulation is shown in Figure 6.36. The dark area is the equalization failure region, whereas the bright area is pass region. The phase of clock signal from the PLL is shifted from -0.3 UI to 0.3 UI and the input amplitude is varied from 50mV to 1V in situ. The result indicates that the timing margin is 0.2 UI for 1 V transmitted signal.
Figure 6.35: Eye diagram at (a) channel (b) CTLE output (c) DFE output [104]
CHAPTER 6. PROPOSED RECEIVER DESIGNS

Figure 6.36: Pass/fail diagram of receiver

Table 6.1: Comparison with the Prior Arts

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Chapter 7

Conclusion

7.1 Contribution Summary

The DRAM transceiver design and calibration approaches in low voltage have been studied in this dissertation. The on-chip open-loop impedance calibration for transceiver output driver in LVSTL memory interface is proposed with an area-efficient output driver design. The proposed circuit detects impedance mismatch due to process and temperature variations using analog sensors and it turns out that the proposed calibration method is a viable solution for each of termination resistances. Moreover, area of the transmitter output driver is reduced by 50% from the conventional design with the proposed design.

In receiver design, PMOS input sense amplifier is designed for low common mode voltage of the LVSTL signaling. As a power saving strategy, adaptive gain controlled (AGC) feature is used on the sense amplifier design, which utilizes process sensor outputs from the calibration circuit. As a result, power consumption is reduce by 15-20%. The
CHAPTER 7. CONCLUSION

The proposed circuit is implemented and demonstrated using an 0.18\(\mu\)m standard CMOS process technology.

Next, continuous-time linear equalizer and a 1-tap decision feedback equalizer receiver architecture is presented that can properly receive a current-mode differential signal in medium-loss multi-giga bit per second serial link. The sampler in the 1-tap DFE architecture is designed to prevent kickback noise and embraced the DFE summer block as an current injection block to improve critical path timing. Functional demonstration and performance improvements are supported by simulation results. The wireline receiver design achieves 1.43 mW/Gb/s power efficiency at 5 GHz clock frequency and 1.1 V supply voltage in a 45 nm standard CMOS technology.
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BIBLIOGRAPHY


Appendix A

Schematic Netlists

// Generated for: spectre
// Design library name: MPW_MH1504_FINAL_V4
// Design cell name: Whole_Calibration_TX_rev2_5_1
// Design view name: schematic
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global 0
include "/home/centos/DB_PDK/Hynix1504_V2/SPICE_Model/HL18G-SL3.7/SPECTRE/corner_HL18G.scs" section=ttt

// Library name: MPW_MH1504_FINAL_V4
// Cell name: invX1_MPW_MH1504_FINAL_Q
// View name: schematic
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// Library name: MPW_MH1504_FINAL_V4
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// View name: schematic
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APPENDIX A. SCHEMATIC NETLISTS

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ends invX1_guarding_dnw_LPDDR4_Q
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: COMP_Guardring_dnw_LPDDR4_Q
// View name: schematic
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I0 (AGND EN net28 AVDD) invX1_guarding_dnw_LPDDR4_Q
PM5 (VOUT ibias AVDD AVDD) pchd_tn w=(2u) l=2u ad=710f
as=1.005p \n
pd=2.71u ps=4.005u nrd=177.5m nrs=251.25m m=(1)∗(4)
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pd=2.71u ps=4.005u nrd=177.5m nrs=251.25m m=(1)∗(4)
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pd=2.71u ps=4.005u nrd=177.5m nrs=251.25m m=(1)∗(4)
PM0 (ibias ibias AVDD AVDD) pchd_tn w=(2u) l=2u ad=710f
as=1.005p \n
pd=2.71u ps=4.005u nrd=177.5m nrs=251.25m m=(1)∗(4)
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as=2.5125p \n
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as=1.005p \n
115
APPENDIX A. SCHEMATIC NETLISTS

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// Cell name: Transmission_gate_Guardring_dnw_LPDDR4_Q
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\[ \text{PM1} \quad \text{(in p_in out VDD)} \quad \text{pchd}_{-}\text{tn} \quad w=(220n) \quad l=180n \quad \text{ad}=198.4f \quad \text{as}=198.4f \]
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ends Transmission_gate_Guardring_dnw_LPDDR4_Q
// End of subcircuit definition.

// Library name: MPDK_HL18G
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// View name: schematic
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\[ \text{R15} \quad \text{(n15 n16 B)} \quad \text{rdhpo}_{-}\text{ns} \quad w=\text{segW} \quad l=\text{segL} \quad \text{mcmode}=\text{nMcMode} \quad \text{mult}=\text{mult_top} \]
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mult_top
R2 (n2 n3 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=
mult_top
R1 (n1 n2 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=
mult_top
R0 (PLUS n1 B) rdhpo_ns w=segW l=segL mcmode=nMcMode
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      mult=mult_top
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      mult=mult_top
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// End of subcircuit definition.

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// View name: schematic
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      mult=mult_top
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   R7 (n7 n8 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=
mult_top
   R6 (n6 n7 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=
APPENDIX A. SCHEMATIC NETLISTS

// End of subcircuit definition.

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  I0 (AGND AVDD EN VIN net044 net039 ibias1) COMP_Guardring_dnw_LPDDR4_Q
  I8 (AGND AVDD net047 PT_EN B0 PT_EN\#) \ /
    Transmission_gate_Guardring_dnw_LPDDR4_Q
  I7 (AGND AVDD AVDD PT_EN\# B0 PT_EN) \ /
    Transmission_gate_Guardring_dnw_LPDDR4_Q
  I5 (AGND AVDD AGND PT_EN\# B1 PT_EN) \ /
    Transmission_gate_Guardring_dnw_LPDDR4_Q
  I3 (AGND AVDD net045 PT_EN B1 PT_EN\#) \ /
    Transmission_gate_Guardring_dnw_LPDDR4_Q
  R3 (AGND AGND net038) rdhpo_ns_pcell_0 m=1 segW=2u segL=30.3u \n    nMcMode=1 mult_top=(1)
  R0 (AGND net038 net039) rdhpo_ns_pcell_1 m=1 segW=2u segL=30u \n    nMcMode=1 mult_top=(1)
  R1 (AGND net039 VREF) rdhpo_ns_pcell_2 m=1 segW=2u segL=37.5u \n    nMcMode=1 mult_top=(1)
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  I2 (AGND net044 net045 AVDD) invX4_Guardring_dnw
  I9 (AGND PT_EN PT_EN\# AVDD)
    invX2_Guardring_dnw_LPDDR4_Q
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// End of subcircuit definition.

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// View name: schematic
APPENDIX A. SCHEMATIC NETLISTS

```
subckt invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q gnd in out vdd
  PM0 (out in vdd vdd) pch_tn w=(1.7u) l=180n ad=816f as=816f pd=4.36u \n    ps=4.36u nrd=282.353m nrs=282.353m m=(1)*(1)
  NM0 (out in gnd gnd) nch_tn w=(880n) l=180n ad=422.4f as=422.4f \n    pd=2.72u ps=2.72u nrd=545.455m nrs=545.455m m=(1)
  *1
ends invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
  // End of subcircuit definition.

  // Library name: MPW_MH1504_FINAL_V4
  // Cell name: invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
  // View name: schematic
subckt invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q gnd in out vdd
  PM0 (out in vdd vdd) pch_tn w=(1.76u) l=180n ad=624.8f as=884.4f \n    pd=2.47u ps=3.645u nrd=201.705m nrs=285.511m m=(1)
  *4
  NM0 (out in gnd gnd) nch_tn w=(880n) l=180n ad=312.4f as=442.2f \n    pd=1.59u ps=2.325u nrd=403.409m nrs=571.023m m=(1)
  *4
ends invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
  // End of subcircuit definition.

  // Library name: MPW_MH1504_FINAL_V4
  // Cell name: OPAMP_Guardring_dnw_LPDDR4_Q
  // View name: schematic
subckt OPAMP_Guardring_dnw_LPDDR4_Q AGND AVDD EN VN VOUT VP ibiasop
  10 (AGND EN net113 AVDD) invX1_guarding_dnw_LPDDR4_Q
  C0 (net111 VOUT) cmim1pl w=21.445u l=21.445u area=459.888p peri=85.78u \n    entrymode=1 mcmode=1 m=1 mult=1
  PM0 (ibiasop ibiasop AVDD AVDD) pchd_tn w=(2u) l=2u ad=540f as=645f \n    pd=2.54u ps=3.145u nrd=135m nrs=161.25m m=(1)*(8)
  PM2 (ibiasop EN AVDD AVDD) pchd_tn w=(2u) l=180n ad=960f as=960f \n    pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1)
  PM5 (VOUT ibiasop AVDD AVDD) pchd_tn w=(16u) l=2u ad
```

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APPENDIX A. SCHEMATIC NETLISTS

\[
\begin{align*}
\text{PM1 (net107 i bias op AVDD AVDD) pchd_tn w=(8u) l=2u ad} \\
pd=16.71u \ ps=20.028u \ nrd=22.1875m \ nrs=25.875m \ m=(1) \\
*(10)
\end{align*}
\]

\[
\begin{align*}
\text{PM4 (net109 VP net107 AVDD) pchd_tn w=(16u) l=2u ad} \\
pd=16.71u \ ps=20.028u \ nrd=22.1875m \ nrs=25.875m \ m=(1) \\
*(10)
\end{align*}
\]

\[
\begin{align*}
\text{PM3 (net105 VN net107 AVDD) pchd_tn w=(16u) l=2u ad} \\
pd=16.71u \ ps=20.028u \ nrd=22.1875m \ nrs=25.875m \ m=(1) \\
*(10)
\end{align*}
\]

\[
\begin{align*}
\text{R0 (AGND net109 net111) rdhpo ns pcell 1 m=1 segW=2u} \\
segL=10u \ nMcmode=1 \ mult\_top=(1)
\end{align*}
\]

\[
\begin{align*}
\text{NM2 (VOUT net109 AGND AGND) nchd_tn w=(2.7u) l=1u ad} \\
as=1.35675f \ pd=3.41u \ ps=5.055u \ nrd=131.481m \ nrs \\
=186.11m \ m=(1) \ *(4)
\end{align*}
\]

\[
\begin{align*}
\text{NM3 (VOUT net113 AGND AGND) nchd_tn w=(1u) l=180n ad=650} \\
as=650f \ pd=3.3u \ ps=3.3u \ nrd=650m \ nrs=650m \ m=(1) \ *(1)
\end{align*}
\]

\[
\begin{align*}
\text{NM1 (net105 net105 AGND AGND) nchd_tn w=(4u) l=2u ad=2.6} \\
pd=9.3u \ ps=9.3u \ nrd=162.5m \ nrs=162.5m \ m=(1) \ *(1)
\end{align*}
\]

\[
\begin{align*}
\text{NM0 (net109 net105 AGND AGND) nchd_tn w=(4u) l=2u ad=2.6} \\
pd=9.3u \ ps=9.3u \ nrd=162.5m \ nrs=162.5m \ m=(1) \ *(1)
\end{align*}
\]

ends OPAMP_Guardring_dnw_LPDDR4_Q
// End of subcircuit definition.

// Library name: MPDK_HL18G
// Cell name: rdhpo_ns
// View name: schematic
subckt rdhpo_ns_pcell_3 B MINUS PLUS
parameters segW=2u segL=10u nMcMode=1 mult_top=(1)
R23 (n23 MINUS B) rdhpo_ns w=segW l=segL mcmode=nMcMode
mult=mult_top
R22 (n22 n23 B) rdhpo_ns w=segW l=segL mcmode=nMcMode

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\[
\text{mult} = \text{mult\_top}
\]

R21 (n21 n22 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R20 (n20 n21 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R19 (n19 n20 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R18 (n18 n19 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R17 (n17 n18 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R16 (n16 n17 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R15 (n15 n16 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R14 (n14 n15 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R13 (n13 n14 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R12 (n12 n13 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R11 (n11 n12 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R10 (n10 n11 B) rdhpo ns w=segW l=segL mcmode=nMcMode
mult = mult_top

R9 (n9 n10 B) rdhpo ns w=segW l=segL mcmode=nMcMode mult = mult_top

R8 (n8 n9 B) rdhpo ns w=segW l=segL mcmode=nMcMode mult = mult_top

R7 (n7 n8 B) rdhpo ns w=segW l=segL mcmode=nMcMode mult = mult_top

R6 (n6 n7 B) rdhpo ns w=segW l=segL mcmode=nMcMode mult = mult_top

R5 (n5 n6 B) rdhpo ns w=segW l=segL mcmode=nMcMode mult = mult_top

R4 (n4 n5 B) rdhpo ns w=segW l=segL mcmode=nMcMode mult = mult_top

R3 (n3 n4 B) rdhpo ns w=segW l=segL mcmode=nMcMode mult = mult_top

R2 (n2 n3 B) rdhpo ns w=segW l=segL mcmode=nMcMode mult = mult_top

R1 (n1 n2 B) rdhpo ns w=segW l=segL mcmode=nMcMode mult =
APPENDIX A. SCHEMATIC NETLISTS

mult_top
R0 (PLUS n1 B) rdhpo_ns w=segW l=segL mcmode=nMcMode
mult=mult_top
.ends rdhpo_ns_pcell_3
// End of subcircuit definition.

// Library name: MPDK_HL18G
// Cell name: rdhpo_ns
// View name: schematic
.subckt rdhpo_ns_pcell_4 B MINUS PLUS
parameters segW=2u segL=10u nMcMode=1 mult_top=(1)
   R5 (n5 MINUS B) rdhpo_ns w=segW l=segL mcmode=nMcMode
      mult=mult_top
R4 (n4 n5 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=
      mult_top
R3 (n3 n4 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=
      mult_top
R2 (n2 n3 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=
      mult_top
R1 (n1 n2 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=
      mult_top
R0 (PLUS n1 B) rdhpo_ns w=segW l=segL mcmode=nMcMode
mult=mult_top
.ends rdhpo_ns_pcell_4
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: P_monitoring_sensor_Guardring_dnw_multi_rev1
// View name: schematic
.subckt P_monitoring_sensor_Guardring_dnw_multi_rev1 EN GND OUT VDD ibiasop
   I1 (GND VDD EN OUT OUT net078 ibiasop)
      OPAMP_Guardring_dnw_LPDDR4_Q
PM3 (net050 net034 VDD VDD) pchd_tn w=(8u) l=8u ad=3.84p
   as=3.84p \% 
      pd=16.96u ps=16.96u nrd=60m nrs=60m m=(2)*(1)
PM5 (net078 net078 net050 VDD) pchd_tn w=(1u) l=12u ad
   =480f as=480f \% 
      pd=2.96u ps=2.96u nrd=480m nrs=480m m=(2)*(1)
PM2 (net034 net034 VDD VDD) pchd_tn w=(8u) l=8u ad=3.84p
   as=3.84p \% 
      pd=16.96u ps=16.96u nrd=60m nrs=60m m=(2)*(1)
APPENDIX A. SCHEMATIC NETLISTS

PM1 (net032 net034 VDD VDD) pchd_tn w=(8u) l=8u ad=3.84p as=3.84p \  
\ \pd=16.96u ps=16.96u nrd=60m nrs=60m m=(2)*(1)  
PM9 (GND net073 net075 VDD) pchd_tn w=(1u) l=1u ad=480f  
as=480f  
\ \pd=2.96u ps=2.96u nrd=480m nrs=480m m=(1)*(1)  
PM8 (net074 net074 VDD VDD) pchd_tn w=(440n) l=180n ad =211.2f  
as=211.2f pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091  
m=(1)*(1)  
PM7 (net073 net073 net074 VDD) pchd_tn w=(440n) l=180n ad =211.2f  
as=211.2f pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091  
m=(1)*(1)  
Q3 (GND GND net082) vp2tn m=8  
Q2 (GND GND net075) vp2tn m=1  
R4 (GND net077 net078) rdhpo_ns_pcell_3 m=1 segW=2u segL =31.25u  
\ \nMcMode=1 mult_top=(1)  
R3 (GND net082 net053) rdhpo_ns_pcell_4 m=1 segW=2u segL =40.005u  
\ \nMcMode=1 mult_top=(1)  
NM9 (net077 net077 GND GND) nchd_tn w=(220n) l=180n ad =198.4f  
as=198.4f pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917  
m=(1)*(1)  
NM0 (net034 net032 net053 GND) nchd_tn w=(2u) l=8u ad =960f as=960f  
pd=4.96u ps=4.96u nrd=240m nrs=240m m=(2)*(1)  
NM1 (net032 net032 net075 GND) nchd_tn w=(2u) l=8u ad =960f as=960f  
pd=4.96u ps=4.96u nrd=240m nrs=240m m=(2)*(1)  
NM6 (net073 net073 net071 GND) nchd_tn w=(220n) l=180n ad=198.4f  
as=198.4f pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917  
m=(1)*(1)  
NM5 (net071 net071 GND GND) nchd_tn w=(220n) l=180n ad =198.4f  
as=198.4f pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917  
m=(1)*(1)  
ends P_monitoring_sensor_Guardring_dnwo_multi_revl  
// End of subcircuit definition.
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// Library name: MPDK_HL18G
// Cell name: rdhpo_ns
// View name: schematic
subckt rdhpo_ns_pcell_5 B MINUS PLUS
parameters segW=2u segL=10u nMcMode=1 mult_top=(1)
R19 (n19 MINUS B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R18 (n18 n19 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R17 (n17 n18 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R16 (n16 n17 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R15 (n15 n16 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R14 (n14 n15 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R13 (n13 n14 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R12 (n12 n13 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R11 (n11 n12 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R10 (n10 n11 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R9 (n9 n10 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R8 (n8 n9 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R7 (n7 n8 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R6 (n6 n7 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R5 (n5 n6 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R4 (n4 n5 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R3 (n3 n4 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R2 (n2 n3 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top

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R1 (n1 n2 B) rdhp0_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R0 (PLUS n1 B) rdhp0_ns w=segW l=segL mcmode=nMcMode
mult=mult_top
ends rdhp0_ns_pcell_5
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: T_monitoring_sensor_Guardring_dnw_rev2
// View name: schematic
subckt T_monitoring_sensor_Guardring_dnw_rev2 EN GND OUT VDD

ibiasop
Q1 (GND GND net131) vp2tn m=1
Q0 (GND GND net134) vp2tn m=8
I4 (GND VDD EN OUT OUT net023 ibiasop)

OPAMP_Guardring_dnw_LPDDR4_Q
PM2 (net041 net041 VDD VDD) pchd_tn w=(4u) l=8u ad=1.42p
as=2.01p \npd=4.71u ps=7.005u nrd=88.75m nrs=125.625m m=(1)*(4)
PM1 (net122 net041 VDD VDD) pchd_tn w=(4u) l=8u ad=1.42p
as=2.01p \npd=4.71u ps=7.005u nrd=88.75m nrs=125.625m m=(1)*(4)
PM0 (net130 net130 VDD VDD) pchd_tn w=(440n) l=180n ad
=211.2f \nas=211.2f pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091
m=(1)*(1)
PM4 (net129 net129 net130 VDD) pchd_tn w=(440n) l=180n
ad=211.2f \n
as=211.2f pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091
m=(1)*(1)
PM6 (GND net129 net131 VDD) pchd_tn w=(1u) l=1u ad=480f
as=480f \n
pd=2.96u ps=2.96u nrd=480m nrs=480m m=(1)*(1)
PM8 (net023 net041 VDD VDD) pchd_tn w=(4u) l=8u ad
=1.81333p \n
as=1.81333p pd=6.24u ps=6.24u nrd=113.333m nrs
=113.333m m=(1)*(3)
R14 (GND net023 GND) rdhp0_ns_pcell_5 m=1 segW=2u segL
=32.815u \n
nMcMode=1 mult_top=(1)
R1 (GND net134 net135) rdhp0_ns_pcell_1 m=1 segW=2u segL
=23.34u \n
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nMcMode=1 mult_top=(1)
NM1 (net122 net122 net131 GND) nchd_tn w=(2u) l=8u ad
=710f as=1.3p \n
pd=2.71u ps=5.3u nrd=177.5m nrs=325m m=(1)*(2)
NM0 (net041 net122 net135 GND) nchd_tn w=(2u) l=8u ad
=710f as=1.3p \n
pd=2.71u ps=5.3u nrd=177.5m nrs=325m m=(1)*(2)
NM2 (net129 net129 net127 GND) nchd_tn w=(220n) l=180n
ad=198.4f \n
as=198.4f pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917
m=(1)*(1)
NM3 (net127 net127 GND GND) nchd_tn w=(220n) l=180n ad
=198.4f \n
as=198.4f pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917
m=(1)*(1)
ends T_monitoring_sensor_Guardring_dnw_rev2

// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: invX32_LPDDR4_Q
// View name: schematic
subckt invX32_LPDDR4_Q gnd in out vdd

PM0 (out in vdd vdd) pch_tn w=(3.52u) l=180n ad=1.2496p
as=1.7688p \n
pd=4.23u ps=6.285u nrd=100.852m nrs=142.756m m=(1)
*(4)
NM0 (out in gnd gnd) nch_tn w=(1.76u) l=180n ad=624.8f
as=884.4f \n
pd=2.47u ps=3.645u nrd=201.705m nrs=285.511m m=(1)
*(4)
ends invX32_LPDDR4_Q

// End of subcircuit definition.

// Library name: MPDK_HL18G
// Cell name: rjnd_ns
// View name: schematic
subckt rjnd_ns_pcell_6 B MINUS PLUS
parameters segW=2u segL=10u nMcMode=1 mult_top=(1)
R4 (PLUS MINUS B) rjnd_ns w=segW l=segL mcmode=nMcMode
mult=mult_top
R3 (PLUS MINUS B) rjnd_ns w=segW l=segL mcmode=nMcMode
mult=mult_top

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R2 (PLUS MINUS B) rjnd_ns w=segW l=segL mcmode=nMcMode
mult=mult_top
R1 (PLUS MINUS B) rjnd_ns w=segW l=segL mcmode=nMcMode
mult=mult_top
R0 (PLUS MINUS B) rjnd_ns w=segW l=segL mcmode=nMcMode
mult=mult_top
ends rjnd_ns_pcell_6
// End of subcircuit definition.

// Library name: MPDK_HL18G
// Cell name: rjnd_ns
// View name: schematic
subckt rjnd_ns_pcell_7 B MINUS PLUS
parameters segW=2u segL=10u nMcMode=1 mult_top=(1)
R0 (PLUS MINUS B) rjnd_ns w=segW l=segL mcmode=nMcMode
mult=mult_top
ends rjnd_ns_pcell_7
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: Calibration design_TX_test_2_MPW_MH1504_FINAL_Q
// View name: schematic
subckt Calibration_design_TX_test_2_MPW_MH1504_FINAL_Q DQ_out GND PD0 PD1 \PD2 PD3 PU0 PU1 PU2 PU3 VDD vr1 vr2
R7 (GND DQ_out vr1) rjnd_ns_pcell_6 m=1 segW=2u segL
=10.155u nMcMode=1 \mult_top=(1)
R5 (GND net027 net028) rjnd_ns_pcell_7 m=1 segW=2u segL
=10.155u \nMcMode=1 mult_top=(1)
R3 (GND net031 net032) rjnd_ns_pcell_7 m=1 segW=2u segL
=10.155u \nMcMode=1 mult_top=(1)
R1 (GND vr2 DQ_out) rjnd_ns_pcell_6 m=1 segW=2u segL
=10.155u nMcMode=1 \mult_top=(1)
NM7 (vr2 PD3 GND GND) nch_tn w=(1.225u) l=180n ad
=572.688f as=822.281f \pd=2.16u ps=3.18u nrd=381.633m nrs=547.959m m=(1) *(4)
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NM6 (vr2 PD2 GND GND) nch_tn w=(1.7u) l=180n ad=1.53p as =1.53p pd=5.2u \  ps=5.2u nrd=529.412m nrs=529.412m m=(1)*n
NM5 (vr2 PD1 GND GND) nch_tn w=(600n) l=180n ad=318f as =318f pd=2.26u \  ps=2.26u nrd=883.333m nrs=883.333m m=(1)*n
NM4 (vr2 PD0 GND GND) nch_tn w=(300n) l=180n ad=206.4f as=206.4f \  pd=1.88u ps=1.88u nrd=2.29333m nrs=2.29333m m=(1) *(4)
NM3 (VDD PU3 vr1 GND) nch_tn w=(4.5u) l=180n ad=3.51p as =5.13p \  pd=6.06u ps=9.03u nrd=173.333m nrs=253.333m m=(1) *(4)
NM2 (VDD PU2 vr1 GND) nch_tn w=(7u) l=180n ad=3.57p as =5.145p pd=8.02u \  ps=11.97u nrd=72.8571m nrs=105m m=(1)*(4)
NM0 (VDD PU0 vr1 GND) nch_tn w=(2.375u) l=180n ad =843.125f as=1.19344p \  pd=3.085u ps=4.5675u nrd=149.474m nrs=211.579m m=(1) *(4)
NM1 (VDD PU1 vr1 GND) nch_tn w=(2.75u) l=180n ad=1.05875p as=1.50563p \  pd=3.52u ps=5.22u nrd=199.091m nrs=199.091m m=(1) *(4)

ends Calibration_design_TX_test_2_MPW_MH1504_FINAL.Q
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: Current_source_wo_R_guardring_dnw
// View name: schematic
subckt Current_source_wo_R_guardring_dnw CS_Rvar_N CS_Rvar_P GND \  Ibias_ADC_P1 Ibias_ADC_P2 Ibias_ADC_T1 Ibias_ADC_T2 Ibias_P \  Ibias_T VDD
Q1 (GND GND net112) vp2tn m=1
Q0 (GND GND CS_Rvar_N) vp2tn m=8
NM4 (net027 net027 GND GND) nchd_tn w=(3u) l=2u ad=1.95p as=1.95p \  pd=7.3u ps=7.3u nrd=216.667m nrs=216.667m m=(1) *(1)
NM5 (net020 net020 net112 GND) nchd_tn w=(2u) l=8u ad =710f as=1.005p \  pd=2.71u ps=4.005u nrd=177.5m nrs=251.25m m=(2) *(4)
APPENDIX A. SCHEMATIC NETLISTS

NM0 (net114 net020 CS_Rvar_P GND) nchd_tn w=(2u) l=8u ad
=710f \
as=1.005p pd=2.71u ps=4.005u nrd=177.5m nrs=251.25m
m=(2)*(4)
NM18 (Ibias_P net027 GND GND) nchd_tn w=(3u) l=2u ad
=1.95p as=1.95p \
pd=7.3u ps=7.3u nrd=216.667m nrs=216.667m m=(1)*(1)
NM2 (net119 net119 net117 GND) nchd_tn w=(220n) l=180n
ad=269.8f \
as=269.8f pd=2.22u ps=2.22u nrd=5.57438 nrs=5.57438
m=(1)*(1)
NM19 (Ibias_T net027 GND GND) nchd_tn w=(3u) l=2u ad
=1.95p as=1.95p \
pd=7.3u ps=7.3u nrd=216.667m nrs=216.667m m=(1)*(1)
NM20 (Ibias_ADC_P1 net027 GND GND) nchd_tn w=(3u) l=2u
ad=1.95p \
as=1.95p pd=7.3u ps=7.3u nrd=216.667m nrs=216.667m m
=(1)*(1)
NM3 (net117 net117 GND GND) nchd_tn w=(220n) l=180n ad
=269.8f \
as=269.8f pd=2.22u ps=2.22u nrd=5.57438 nrs=5.57438
m=(1)*(1)
NM21 (Ibias_ADC_P2 net027 GND GND) nchd_tn w=(3u) l=2u
ad=1.95p \
as=1.95p pd=7.3u ps=7.3u nrd=216.667m nrs=216.667m m
=(1)*(1)
NM22 (Ibias_ADC_T1 net027 GND GND) nchd_tn w=(3u) l=2u
ad=1.95p \
as=1.95p pd=7.3u ps=7.3u nrd=216.667m nrs=216.667m m
=(1)*(1)
NM23 (Ibias_ADC_T2 net027 GND GND) nchd_tn w=(3u) l=2u
ad=1.95p \
as=1.95p pd=7.3u ps=7.3u nrd=216.667m nrs=216.667m m
=(1)*(1)
PM3 (net027 net114 VDD VDD) pchd_tn w=(2u) l=8u ad=710f
as=1.005p \
pd=2.71u ps=4.005u nrd=177.5m nrs=251.25m m=(2)*(4)
PM2 (net114 net114 VDD VDD) pchd_tn w=(2u) l=8u ad=710f
as=1.005p \
pd=2.71u ps=4.005u nrd=177.5m nrs=251.25m m=(2)*(4)
PM1 (net020 net114 VDD VDD) pchd_tn w=(2u) l=8u ad=710f
as=1.005p
APPENDIX A. SCHEMATIC NETLISTS

\[
\begin{align*}
\text{pd} &= 2.71 \mu \text{s}, \quad \text{ps} = 4.005 \mu \text{s}, \quad \text{nr}d = 177.5 \text{m}, \quad \text{nr}s = 251.25 \text{m}, \quad m = (2) \times (4) \\
\text{PM0} (\text{net120 net120 VDD VDD}) & \quad \text{pchd}_\text{tn} = (880n), \quad l = 180n, \quad \text{ad} = 572f, \quad \text{as} = 572f \\
\text{pd} &= 3.06 \mu \text{s}, \quad \text{ps} = 3.06 \mu \text{s}, \quad \text{nr}d = 738.636 \text{m}, \quad \text{nr}s = 738.636 \text{m}, \quad m = (1) \\
\text{PM4} (\text{net119 net119 net120 VDD}) & \quad \text{pchd}_\text{tn} = (880n), \quad l = 180n, \quad \text{ad} = 572f, \quad \text{as} = 572f \\
\text{pd} &= 3.06 \mu \text{s}, \quad \text{ps} = 3.06 \mu \text{s}, \quad \text{nr}d = 738.636 \text{m}, \quad \text{nr}s = 738.636 \text{m}, \quad m = (1) \\
\text{PM6} (\text{GND net119 net112 VDD}) & \quad \text{pchd}_\text{tn} = (1u), \quad l = 1u, \quad \text{ad} = 650f, \quad \text{as} = 650f \\
\text{pd} &= 3.3 \mu \text{s}, \quad \text{ps} = 3.3 \mu \text{s}, \quad \text{nr}d = 650m, \quad \text{nr}s = 650m, \quad m = (1) \times (1)
\end{align*}
\]

\text{ends Current_source_wo_R.guarding_dn}

// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: NAND_LPDDR4_Q_MPW_MH1504_FINAL_Q
// View name: schematic
\text{subckt NAND_LPDDR4_Q_MPW_MH1504_FINAL_Q GND VDD in1 in2 out}
\text{NM1 (net21 in2 GND GND) nch}_\text{tn} = (1u), \quad l = 180n, \quad \text{ad} = 650f, \quad \text{as} = 650f \\
\text{pd} = 3.3 \mu \text{s}, \quad \text{ps} = 3.3 \mu \text{s}, \quad \text{nr}d = 650m, \quad \text{nr}s = 650m, \quad m = (1) \times (1)
\text{NM0 (out in1 net21 GND) nch}_\text{tn} = (1u), \quad l = 180n, \quad \text{ad} = 650f, \quad \text{as} = 650f \\
\text{pd} = 3.3 \mu \text{s}, \quad \text{ps} = 3.3 \mu \text{s}, \quad \text{nr}d = 650m, \quad \text{nr}s = 650m, \quad m = (1) \times (1)
\text{PM1 (out in2 VDD VDD) pch}_\text{tn} = (1u), \quad l = 180n, \quad \text{ad} = 650f, \quad \text{as} = 650f \\
\text{pd} = 3.3 \mu \text{s}, \quad \text{ps} = 3.3 \mu \text{s}, \quad \text{nr}d = 650m, \quad \text{nr}s = 650m, \quad m = (1) \times (1)
\text{PM0 (out in1 VDD VDD) pch}_\text{tn} = (1u), \quad l = 180n, \quad \text{ad} = 650f, \quad \text{as} = 650f \\
\text{pd} = 3.3 \mu \text{s}, \quad \text{ps} = 3.3 \mu \text{s}, \quad \text{nr}d = 650m, \quad \text{nr}s = 650m, \quad m = (1) \times (1)
\text{ends NAND_LPDDR4_Q_MPW_MH1504_FINAL_Q}

// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q
// View name: schematic
\text{subckt AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q GND VDD in1 in2 out}
\text{I0 (GND VDD in1 in2 net14) NAND_LPDDR4_Q_MPW_MH1504_FINAL_Q}
\text{I1 (GND net14 out VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q}
\text{ends AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q}

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// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name:
// Transmission_gate_Guardring_dnw_Chip_FloorPlan_v7
// View name: schematic
subckt Transmission_gate_Guardring_dnw_Chip_FloorPlan_v7 GND VDD in n_in \ out p_in
NM1 (in n_in out GND) nchd_tn w=(220n) l=180n ad=198.4f as=198.4f \ pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)
PM1 (in p_in out VDD) pchd_tn w=(220n) l=180n ad=198.4f as=198.4f \ pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)
ends Transmission_gate_Guardring_dnw_Chip_FloorPlan_v7
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: invX1_garding_dnw_Chip_FloorPlan_v7
// View name: schematic
subckt invX1_garding_dnw_Chip_FloorPlan_v7 gnd in out vdd
NM0 (out in gnd gnd) nchd_tn w=(220n) l=180n ad=198.4f as=198.4f \ pd=1.88u ps=1.88u nrd=4.09917 nrs=4.09917 m=(1)*(1)
PM0 (out in vdd vdd) pchd_tn w=(440n) l=180n ad=211.2f as=211.2f \ pd=1.84u ps=1.84u nrd=1.09091 nrs=1.09091 m=(1)*(1)
ends invX1_garding_dnw_Chip_FloorPlan_v7
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: COMP_Guardring_dnw_Chip_FloorPlan_v7
// View name: schematic
subckt COMP_Guardring_dnw_Chip_FloorPlan_v7 AGND AVDD EN VN VOUT VP ibias
  I0 (AGND EN net28 AVDD)
    invX1_garding_dnw_Chip_FloorPlan_v7
  PM5 (VOUT ibias AVDD AVDD) pchd_tn w=(2u) l=2u ad=710f as=1.005p \ pd=2.71u ps=4.005u nrd=177.5m nrs=251.25m m=(1)*(4)
  PM4 (net21 VP net18 AVDD) pchd_tn w=(2u) l=4u ad=710f as
APPENDIX A. SCHEMATIC NETLISTS

=1.005p  
  pd=2.71u  ps=4.005u  nrd=177.5m  nrs=251.25m  m=(1)*(4)  
PM3 (net16  VN  net18  AVDD)  pchd_tn  w=(2u)  l=4u  ad=710f  as=1.005p  
  pd=2.71u  ps=4.005u  nrd=177.5m  nrs=251.25m  m=(1)*(4)  
PM2 (ibias  EN  AVDD  AVDD)  pchd_tn  w=(550n)  l=180n  ad=357.5f  as=357.5f  
  pd=2.4u  ps=2.4u  nrd=1.18182m  nrs=1.18182m  m=(1)*(1)  
PM1 (net18  ibias  AVDD  AVDD)  pchd_tn  w=(2u)  l=2u  ad=710f  as=1.005p  
  pd=2.71u  ps=4.005u  nrd=177.5m  nrs=251.25m  m=(1)*(4)  
PM0 (ibias  ibias  AVDD  AVDD)  pchd_tn  w=(2u)  l=2u  ad=710f  as=1.005p  
  pd=2.71u  ps=4.005u  nrd=177.5m  nrs=251.25m  m=(1)*(4)  
NM5 (VOUT  net21  AGND  AGND)  nchd_tn  w=(5u)  l=1u  ad=1.775p  as=2.5125p  
  pd=5.71u  ps=8.505u  nrd=71m  nrs=100.5m  m=(1)*(4)  
NM3 (VOUT  net28  AGND  AGND)  nchd_tn  w=(550n)  l=180n  ad=357.5f  as=357.5f  
  pd=2.4u  ps=2.4u  nrd=1.18182m  nrs=1.18182m  m=(1)*(1)  
NM1 (net16  net16  AGND  AGND)  nchd_tn  w=(2u)  l=4u  ad=710f  as=1.005p  
  pd=2.71u  ps=4.005u  nrd=177.5m  nrs=251.25m  m=(1)*(4)  
NM0 (net21  net16  AGND  AGND)  nchd_tn  w=(2u)  l=4u  ad=710f  as=1.005p  
  pd=2.71u  ps=4.005u  nrd=177.5m  nrs=251.25m  m=(1)*(4)  
ends  COMP_Guardring_dnw_Chip_FloorPlan_v7
//  End of subcircuit definition.

//  Library name:  MPW_MH1504_FINAL_V4
//  Cell name:  invX2_Guardring_dnw_Chip_FloorPlan_v7
//  View name:  schematic
subckt  invX2_Guardring_dnw_Chip_FloorPlan_v7  gnd  in  out  vdd  
  NM1 (out  in  gnd  gnd)  nchd_tn  w=(440n)  l=180n  ad=211.2f  as=211.2f  
    pd=1.84u  ps=1.84u  nrd=1.09091m  nrs=1.09091m  m=(1)*(1)  
  PM4 (out  in  vdd  vdd)  pchd_tn  w=(880n)  l=180n  ad=422.4f  as=422.4f  
    pd=2.72u  ps=2.72u  nrd=545.455m  nrs=545.455m  m=(1)  
    *(1)
ends  invX2_Guardring_dnw_Chip_FloorPlan_v7
//  End of subcircuit definition.
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// Library name: MPDK_HL18G
// Cell name: rdhpo_ns
// View name: schematic
subckt rdhpo_ns_pcell_8 B MINUS PLUS
parameters segW=2u segL=10u nMcMode=1 mult_top=(1)
   R11 (n11 MINUS B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R10 (n10 n11 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R9 (n9 n10 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R8 (n8 n9 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R7 (n7 n8 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R6 (n6 n7 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R5 (n5 n6 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R4 (n4 n5 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R3 (n3 n4 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R2 (n2 n3 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R1 (n1 n2 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R0 (PLUS n1 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
ends rdhpo_ns_pcell_8
// End of subcircuit definition.

// Library name: MPDK_HL18G
// Cell name: rdhpo_ns
// View name: schematic
subckt rdhpo_ns_pcell_9 B MINUS PLUS
parameters segW=2u segL=10u nMcMode=1 mult_top=(1)
   R3 (n3 MINUS B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
   R2 (n2 n3 B) rdhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top

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R1 (n1 n2 B) rhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
R0 (PLUS n1 B) rhpo_ns w=segW l=segL mcmode=nMcMode mult=mult_top
ends rhpo_ns_pcell_9
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: 2bit_FLASH_ADC_T_Guardring_dnw
// View name: schematic
subckt

MPW_MH1504_FINAL_V4_2bit_FLASH_ADC_T_Guardring_dnw_schematic

AGND \ AVDD B0 B1 EN PT_EN VIN VREF ibias3 ibias4
18 (AGND AVDD net29 PT_EN B0 PT_EN\#) \ Transmission_gate_Guardring_dnw_Chip_FloorPlan_v7
17 (AGND AVDD AVDD PT_EN\# B0 PT_EN) \ Transmission_gate_Guardring_dnw_Chip_FloorPlan_v7
15 (AGND AVDD AGND PT_EN\# B1 PT_EN) \ Transmission_gate_Guardring_dnw_Chip_FloorPlan_v7
13 (AGND AVDD net31 PT_EN B1 PT_EN\#) \ Transmission_gate_Guardring_dnw_Chip_FloorPlan_v7
11 (AGND AVDD EN VIN net29 Vref_b0 ibias4) \ COMP_Guardring_dnw_Chip_FloorPlan_v7
10 (AGND AVDD EN VIN net31 Vref_b1 ibias3) \ COMP_Guardring_dnw_Chip_FloorPlan_v7
14 (AGND PT_EN PT_EN\# AVDD)
invX2_Guardring_dnw_Chip_FloorPlan_v7
R2 (AGND AGND Vref_b0) rhpo_ns_pcell_10 m=1 segW=2u segL =26.8u \ nMcMode=1 mult_top=(1)
R1 (AGND Vref_b1 VREF) rhpo_ns_pcell_8 m=1 segW=2u segL =44u nMcMode=1 \ mult_top=(1)
R0 (AGND Vref_b0 Vref_b1) rhpo_ns_pcell_9 m=1 segW=2u segL=30u \ nMcMode=1 mult_top=(1)
ends

MPW_MH1504_FINAL_V4_2bit_FLASH_ADC_T_Guardring_dnw_schematic

// End of subcircuit definition.
APPENDIX A. SCHEMATIC NETLISTS

// Library name: MPW_MH1504_FINAL_V4
// Cell name: NAND_3input
// View name: schematic
subckt NAND_3input GND VDD in1 in2 in3 out
   NM2 (net26 in3 GND GND) nch_tn w=(1u) l=180n ad=480f as
     =480f pd=2.96u \n     ps=2.96u nrd=480m nrs=480m m=(1)*(1)
   NM1 (net27 in2 net26 GND) nch_tn w=(1u) l=180n ad=480f as=480f \n     pd=2.96u ps=2.96u nrd=480m nrs=480m m=(1)*(1)
   NM0 (out in1 net27 GND) nch_tn w=(1u) l=180n ad=480f as
     =480f pd=2.96u \n     ps=2.96u nrd=480m nrs=480m m=(1)*(1)
   PM2 (out in3 VDD VDD) pch_tn w=(800n) l=180n ad=384f as=384f \n     pd=2.56u ps=2.56u nrd=600m nrs=600m m=(1)*(1)
   PM1 (out in1 VDD VDD) pch_tn w=(800n) l=180n ad=384f as=384f \n     pd=2.56u ps=2.56u nrd=600m nrs=600m m=(1)*(1)
   PM0 (out in2 VDD VDD) pch_tn w=(800n) l=180n ad=384f as=384f \n     pd=2.56u ps=2.56u nrd=600m nrs=600m m=(1)*(1)
ends NAND_3input
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: AND_3
// View name: schematic
subckt AND_3 GND VDD in1 in2 in3 out
   I0 (GND VDD in1 in2 in3 net16) NAND_3input
   I1 (GND net16 out VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
ends AND_3
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: NOR_LPDDR4_Q
// View name: schematic
subckt NOR_LPDDR4_Q GND VDD in1 in2 out
   NM1 (out in2 GND GND) nch_tn w=(350n) l=180n ad=211.4f as=211.4f \n     pd=1.88u ps=1.88u nrd=1.72571 nrs=1.72571 m=(1)*(1)
   NM0 (out in1 GND GND) nch_tn w=(350n) l=180n ad=211.4f
APPENDIX A. SCHEMATIC NETLISTS

```
as=211.4 f \n  pd=1.88 u ps=1.88 u nrd=1.72571 nrs=1.72571 m=(1)*(1)
PM1 (net18 in1 VDD VDD) pch_tn w=(1.4 u) l=180 n ad=672 f
  as=672 f \n  pd=3.76 u ps=3.76 u nrd=342.857 m nrs=342.857 m m=(1)
  *(1)
PM0 (out in2 net18 VDD) pch_tn w=(1.4 u) l=180 n ad=672 f
  as=672 f \n  pd=3.76 u ps=3.76 u nrd=342.857 m nrs=342.857 m m=(1)
  *(1)
ends NOR_LPDDR4_Q
// End of subcircuit definition.
```

```
// Library name: MPW_MH1504_FINAL_V4
// Cell name: OR_2_LPDDR4_Q
// View name: schematic
subckt OR_2_LPDDR4_Q GND VDD in1 in2 out
  I0 (GND VDD in1 in2 net14) NOR_LPDDR4_Q
  I1 (GND net14 out VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
ends OR_2_LPDDR4_Q
// End of subcircuit definition.
```

```
// Library name: MPW_MH1504_FINAL_V4
// Cell name: NOR_3input
// View name: schematic
subckt NOR_3input GND VDD in1 in2 in3 out
  PM2 (out in3 net25 VDD) pch_tn w=(2 u) l=180 n ad=960 f as
    =960 f pd=4.96 u \n    ps=4.96 u nrd=240 m nrs=240 m m=(1)*(1)
PM1 (net25 in2 net26 VDD) pch_tn w=(2 u) l=180 n ad=960 f as
    =960 f pd=4.96 u \n    ps=4.96 u nrd=240 m nrs=240 m m=(1)*(1)
PM0 (net26 in1 VDD VDD) pch_tn w=(2 u) l=180 n ad=960 f as
    =960 f pd=4.96 u \n    ps=4.96 u nrd=240 m nrs=240 m m=(1)*(1)
NM2 (out in3 GND GND) nch_tn w=(350 n) l=180 n ad=211.4 f as
    =211.4 f pd=1.88 u \n    ps=1.88 u nrd=1.72571 nrs=1.72571 m=(1)*(1)
NM1 (out in2 GND GND) nch_tn w=(350 n) l=180 n ad=211.4 f as
    =211.4 f pd=1.88 u \n    ps=1.88 u nrd=1.72571 nrs=1.72571 m=(1)*(1)
NM0 (out in1 GND GND) nch_tn w=(350 n) l=180 n ad=211.4 f
```

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as=211.4f \
  pd=1.88u ps=1.88u nrd=1.72571 nrs=1.72571 m=(1)*(1)
ends NOR_3input
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: OR_3
// View name: schematic
subckt OR_3 GND VDD in1 in2 in3 out
  I0 (GND VDD in1 in2 in3 net16) NOR_3input
  I1 (GND net16 out VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
ends OR_3
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: PU_decoder_rev
// View name: schematic
subckt PU_decoder_rev A B C D D0 D1 D2 GND VDD
  I19 (GND VDD A D net37)
    AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I17 (GND VDD B C net36)
    AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I20 (GND VDD A net011 C net39) AND_3
  I16 (GND VDD A net011 net25 net38) AND_3
  I21 (GND VDD net37 net39 D1) OR_2_LPDDR4_Q
  I18 (GND VDD net36 net38 D D0) OR_3
  I22 (GND C net25 VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I18 (GND B net011 VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I24 (GND net011 D2 VDD)
    invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
ends PU_decoder_rev
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
// View name: schematic
subckt bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q GND VDD in out
  I1 (GND net11 out VDD)
    invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I0 (GND in net11 VDD) invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
ends bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
// End of subcircuit definition.
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// Library name: MPW_MH1504_FINAL_V4
// Cell name: NOR_4input_LPDDR4_Q
// View name: schematic
subckt NOR_4input_LPDDR4_Q GND VDD in1 in2 in3 in4 out
   NM3 (out in4 GND GND) nch_tn w=(350n) l=180n ad=211.4f
       as=211.4f \n       pd=1.88u ps=1.88u nrd=1.72571 nrs=1.72571 m=(1)*(1)
   NM2 (out in3 GND GND) nch_tn w=(350n) l=180n ad=211.4f
       as=211.4f \n       pd=1.88u ps=1.88u nrd=1.72571 nrs=1.72571 m=(1)*(1)
   NM1 (out in1 GND GND) nch_tn w=(350n) l=180n ad=211.4f
       as=211.4f \n       pd=1.88u ps=1.88u nrd=1.72571 nrs=1.72571 m=(1)*(1)
   NM0 (out in2 GND GND) nch_tn w=(350n) l=180n ad=211.4f
       as=211.4f \n       pd=1.88u ps=1.88u nrd=1.72571 nrs=1.72571 m=(1)*(1)
   PM3 (net31 in1 VDD VDD) pch_tn w=(3u) l=180n ad=1.44p as
       =1.44p \n       pd=6.96u ps=6.96u nrd=160m nrs=160m m=(1)*(1)
   PM2 (net32 in2 net31 VDD) pch_tn w=(3u) l=180n ad=1.44p
       as=1.44p \n       pd=6.96u ps=6.96u nrd=160m nrs=160m m=(1)*(1)
   PM1 (net33 in3 net32 VDD) pch_tn w=(3u) l=180n ad=1.44p
       as=1.44p \n       pd=6.96u ps=6.96u nrd=160m nrs=160m m=(1)*(1)
   PM0 (out in4 net33 VDD) pch_tn w=(3u) l=180n ad=1.44p as
       =1.44p \n       pd=6.96u ps=6.96u nrd=160m nrs=160m m=(1)*(1)
ends NOR_4input_LPDDR4_Q
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: OR_4_LPDDR4_Q
// View name: schematic
subckt OR_4_LPDDR4_Q GND VDD in1 in2 in3 in4 out
   I0 (GND VDD in1 in2 in3 in4 net19) NOR_4input_LPDDR4_Q
   I1 (GND net19 out VDD) invX4_LPDDR4_Q
ends OR_4_LPDDR4_Q
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4

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// Cell name: PD_decoder_rev
// View name: schematic
subckt PD_decoder_rev A B C D D0 D1 D2 GND VDD
  I9 (GND VDD A C net58) AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I7 (GND VDD B C net57) AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I6 (GND VDD net22 D net61)
    AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I2 (GND VDD A D net55) AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I0 (GND VDD A net19 net56)
    AND_2_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I10 (GND VDD B net58 D2) OR_2_LPDDR4_Q
  I8 (GND VDD net60 net61 net57 D1) OR_3
  I4 (GND VDD A net21 net19 net60) AND_3
  I3 (GND VDD net22 C net41 net59) AND_3
  I5 (GND VDD B net56 net55 net59 D0) OR_4_LPDDR4_Q
  I14 (GND D net41 VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I13 (GND C net19 VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I12 (GND B net21 VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
  I11 (GND A net22 VDD) invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
ends PD_decoder_rev
// End of subcircuit definition.

// Library name: MPW_MH1504_FINAL_V4
// Cell name: Whole_Calibration_TX_rev2_5_1
// View name: schematic
I52 (GND net0176 net0146 DVDD1) invX1_MPW_MH1504_FINAL_Q
I48 (GND net0178 net0149 DVDD1) invX1_MPW_MH1504_FINAL_Q
I44 (GND net0177 net0152 DVDD1) invX1_MPW_MH1504_FINAL_Q
I40 (GND net0175 net0143 DVDD1) invX1_MPW_MH1504_FINAL_Q
I36 (GND net057 net090 DVDD1) invX1_MPW_MH1504_FINAL_Q
I32 (GND net054 net093 DVDD1) invX1_MPW_MH1504_FINAL_Q
I28 (GND net047 net096 DVDD1) invX1_MPW_MH1504_FINAL_Q
I18 (GND net046 net083 DVDD1) invX1_MPW_MH1504_FINAL_Q
I17 (GND net051 net079 DVDD1) invX1_MPW_MH1504_FINAL_Q
I15 (GND net049 net084 DVDD1) invX1_MPW_MH1504_FINAL_Q
I11 (GND net0184 net0178 net0177 EN_P_ADC PT_EN_P_ADC Vout_P
  VREF_P_ADC \n    net222 net221) \n  MPW_MH1504_FINAL_V4_2bit_FLASH_ADC_P_Guardring_dnw_schematic
I53 (GND net0146 net0145 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q

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APPENDIX A. SCHEMATIC NETLISTS

I49 (GND net0149 net0148 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
I45 (GND net0152 net0151 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
I43 (GND net0143 net0142 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
I37 (GND net090 net0116 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
I33 (GND net093 net092 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
I29 (GND net096 net095 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
I11 (GND net083 net080 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
I10 (GND net079 net081 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
I9 (GND net084 net082 DVDD1)
  invX4_LPDDR4_Q_MPW_MH1504_FINAL_Q
I55 (GND net0145 net0144 DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I50 (GND net0148 net0147 DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I46 (GND net0151 net0150 DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I42 (GND net0142 net0141 DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I39 (GND net0116 pd_buf\<2\> DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I34 (GND net092 pd_buf\<1\> DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I30 (GND net095 pd_buf\<0\> DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I14 (GND net080 pu_buf\<2\> DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I13 (GND net081 pu_buf\<1\> DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I12 (GND net082 pu_buf\<0\> DVDD1)
  invX16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I59 (EN_P_monitoring GND Vout_P AVDD1 net220)
  P_monitoring_sensor_Guardring_dnw_multi_rev1
I60 (EN_T_monitoring GND Vout_T AVDD1 net217)
  T_monitoring_sensor_Guardring_dnw_rev2
APPENDIX A. SCHEMATIC NETLISTS

I54 (GND net0144 T_ADC_B1 DVDD1) invX32_LPDDDR4_Q
I51 (GND net0147 P_ADC_B0 DVDD1) invX32_LPDDDR4_Q
I47 (GND net0150 P_ADC_B1 DVDD1) invX32_LPDDDR4_Q
I41 (GND net0141 T_ADC_B0 DVDD1) invX32_LPDDDR4_Q
I38 (GND pd_buf<2> PD_D2 DVDD1) invX32_LPDDDR4_Q
I35 (GND pd_buf<1> PD_D1 DVDD1) invX32_LPDDDR4_Q
I31 (GND pd_buf<0> PD_D0 DVDD1) invX32_LPDDDR4_Q
I27 (GND pu_buf<2> PU_D2 DVDD1) invX32_LPDDDR4_Q
I26 (GND pu_buf<1> PU_D1 DVDD1) invX32_LPDDDR4_Q
I15 (GND pu_buf<0> PU_D0 DVDD1) invX32_LPDDDR4_Q
I56 (DQ_out GND PD_D0_out PD_D1_out PD_D2_out PD_D3_out
  PU_D0_out \ 
  PU_D1_out PU_D2_out PU_D3_out VDDQ net0181 net0183)
  Calibration_design_TX_test_2_MPW_MH1504_FINAL_Q
I6 (CS_Rvar_N CS_Rvar_P GND net222 net221 net219 net218
net220 net217 \ 
  AVDD1) Current_source_wo_R_guardring_dnw
I25 (GND DVDD1 PD_D3 Data_B net0128)
  AND_2_LPDDDR4_Q_MPW_MH1504_FINAL_Q
I24 (GND DVDD1 net057 Data_B net0127)
  AND_2_LPDDDR4_Q_MPW_MH1504_FINAL_Q
I23 (GND DVDD1 net054 Data_B net0126)
  AND_2_LPDDDR4_Q_MPW_MH1504_FINAL_Q
I22 (GND DVDD1 net047 Data_B net0124)
  AND_2_LPDDDR4_Q_MPW_MH1504_FINAL_Q
I21 (GND DVDD1 PU_D3 Data net0121)
  AND_2_LPDDDR4_Q_MPW_MH1504_FINAL_Q
I20 (GND DVDD1 net046 Data net0122)
  AND_2_LPDDDR4_Q_MPW_MH1504_FINAL_Q
I19 (GND DVDD1 net051 Data net0123)
  AND_2_LPDDDR4_Q_MPW_MH1504_FINAL_Q
I18 (GND DVDD1 net049 Data net0125)
  AND_2_LPDDDR4_Q_MPW_MH1504_FINAL_Q
I61 (GND net0188 net0175 net0176 EN_T_ADC PT_EN_T_ADC Vout_T
  VREF_T_ADC \ 
  net219 net218) \ 
  MPW_MH1504_FINAL_V4_2bit_FLASH_ADC_T_Guardring_dnw_schematic
I17 (net0178 net0177 net0176 net0175 net049 net051 net046
  GND DVDD1) \ 
  PU_decoder_rev
APPENDIX A. SCHEMATIC NETLISTS

I68 (GND DVDD1 net0121 PU_D3_out)
bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I67 (GND DVDD1 net0122 PU_D2_out)
bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I66 (GND DVDD1 net0123 PU_D1_out)
bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I65 (GND DVDD1 net0125 PU_D0_out)
bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I70 (GND DVDD1 net0126 PD_D1_out)
bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I69 (GND DVDD1 net0124 PD_D0_out)
bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I71 (GND DVDD1 net0127 PD_D2_out)
bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I72 (GND DVDD1 net0128 PD_D3_out)
bufferx16_LPDDR4_Q_MPW_MH1504_FINAL_Q
I2 (net0178 net0177 net0175 net047 net054 net057 GND DVDD1) \n
PD_decoder_rev
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \ntnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \nmaxnotes=5 maxwarns=5 \ndigits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.
output" \nchecklimitdest=psf
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub

// Generated for: spectre
// Generated on: Nov 6 16:06:08 2016
// Design library name: A_Thesis
// Design cell name: TB_SerDes_Pre_emp
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
parameters freq_in
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include "/home/centos/DB_PDK/gpdk045_v_3_5/gpdk045/../../models/spectre/gpdk045.scs" section=mc

// Library name: A_Thesis
// Cell name: Inv_600n
// View name: schematic
subckt Inv_600n GND IN OUT VDD
    NM0 (OUT IN GND GND) g45n1hvt w=(600n) l=45n nf=1 as=84f ad=84f \n        ps=1.48u pd=1.48u nrd=233.333m nrs=233.333m sa=140n sb=140n \n        sd=160n sca=91.32138 scb=0.07706 scc=0.01082 m=(1)
    PM0 (OUT IN VDD VDD) g45p1hvt w=(680n) l=45n nf=1 as=95.2f ad=95.2f \n        ps=1.64u pd=1.64u nrd=205.882m nrs=205.882m sa=140n sb=140n \n        sd=160n sca=85.86137 scb=0.07381 scc=0.01017 m=(1)
ends Inv_600n
// End of subcircuit definition.

// Library name: A_Thesis
// Cell name: Inv_200n
// View name: schematic
subckt Inv_200n GND IN OUT VDD
    NM0 (OUT IN GND GND) g45n1hvt w=(200n) l=45n nf=1 as=28f ad=28f \n        ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n \n        sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
    PM0 (OUT IN VDD VDD) g45p1hvt w=(230n) l=45n nf=1 as=32.2f ad=32.2f \n        ps=740n pd=740n nrd=608.696m nrs=608.696m sa=140n sb=140n sd=160n \n        sca=155.75886 scb=0.10583 scc=0.01925 m=(1)
ends Inv_200n
// End of subcircuit definition.

// Library name: A_Thesis
// Cell name: TGFF
// View name: schematic
subckt TGFF CK_in D GND Q QB VDD
    I9 (GND net07 QB VDD) Inv_600n

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I4 (GND QB Q VDD) Inv_600n
NM6 (net018 QB GND GND) g45n1svt w=(200n) l=45n nf=1 as=28f ad=28f
\begin{verbatim}
  ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
  sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
\end{verbatim}
NM5 (net07 CKB net018 GND) g45n1svt w=(200n) l=45n nf=1 as=28f ad=28f
\begin{verbatim}
  ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
  sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
\end{verbatim}
NM2 (net6 net5 GND GND) g45n1svt w=(200n) l=45n nf=1 as=28f ad=28f
\begin{verbatim}
  ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
  sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
\end{verbatim}
NM1 (net7 CK net6 GND) g45n1svt w=(200n) l=45n nf=1 as=28f ad=28f
\begin{verbatim}
  ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
  sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
\end{verbatim}
PM5 (net07 CKB net5 VDD) g45p11vt w=(200n) l=45n nf=1 as=28f ad=28f
\begin{verbatim}
  ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
  sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
\end{verbatim}
PM0 (net7 CK net1 VDD) g45p11vt w=(200n) l=45n nf=1 as=28f ad=28f
\begin{verbatim}
  ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
  sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
\end{verbatim}
NM4 (net07 CK net5 GND) g45n11vt w=(200n) l=45n nf=1 as=28f ad=28f
\begin{verbatim}
  ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
  sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
\end{verbatim}
NM0 (net7 CKB net1 GND) g45n11vt w=(200n) l=45n nf=1 as=28f ad=28f
\begin{verbatim}
  ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
  sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
\end{verbatim}
I8 (GND CKB CK VDD) Inv_200n

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I12 (GND CK_in CKB VDD) Inv_200n
I6 (GND net7 net5 VDD) Inv_200n
I11 (GND D net1 VDD) Inv_200n
PM7 (net017 QB VDD VDD) g45p1svt w=(200n) l=45n nf=1 as =28f ad=28f \\
   ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd =160n \\
   sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
PM6 (net07 CK net017 VDD) g45p1svt w=(200n) l=45n nf=1 as =28f ad=28f \\
   ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd =160n \\
   sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
PM3 (net8 net5 VDD VDD) g45p1svt w=(200n) l=45n nf=1 as =28f ad=28f \\
   ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd =160n \\
   sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
PM2 (net7 CKB net8 VDD) g45p1svt w=(200n) l=45n nf=1 as =28f ad=28f \\
   ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd =160n \\
   sca=169.02145 scb=0.10920 scc=0.02100 m=(1)

ends TGFF
// End of subcircuit definition.

// Library name: A_Thesis
// Cell name: MUX_2
// View name: schematic
subckt MUX_2 A B GND SEL VDD Y
   NM1 (Y SEL A GND) g45n11vt w=(200n) l=45n nf=1 as=28f ad =28f ps=680n \\
      pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n \\
      sca=169.02145 \ \\
      scb=0.10920 scc=0.02100 m=(1)
   NM0 (Y SEL_B B GND) g45n11vt w=(200n) l=45n nf=1 as=28f ad=28f ps=680n \\
      pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n \\
      sca=169.02145 \ \\
      scb=0.10920 scc=0.02100 m=(1)
   PM1 (Y SEL_B A VDD) g45p11vt w=(200n) l=45n nf=1 as=28f ad=28f ps=680n \\

APPENDIX A. SCHEMATIC NETLISTS

pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
sca=169.02145 \n
scb=0.10920 scc=0.02100 m=(1)
PM0 (Y SEL B VDD) g45p11vt w=(200n) l=45n nf=1 as=28f ad
=28f ps=680n \n
pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
sca=169.02145 \n
scb=0.10920 scc=0.02100 m=(1)

I8 (GND SEL SEL_B VDD) Inv_600n
ends MUX_2
// End of subcircuit definition.

// Library name: A_Thesis
// Cell name: Serializer_Half_rate
// View name: schematic
subckt Serializer_Half_rate CK CK_by_2 CK_by_4 DATA\<0\> DATA\<1\> \n
DATA\<2\> DATA\<3\> Serial_DATA Serial_DATA_B
I54 (CK net015 0 Serial_DATA Serial_DATA_B vdd!) TGFF
I47 (CK_by_2 net016 0 DC net023 vdd!) TGFF
I43 (CK_by_2 net017 0 AB net022 vdd!) TGFF
I24 (CK_by_4 DATA\<2\> 0 C net14 vdd!) TGFF
I18 (CK_by_4 DATA\<0\> 0 A net16 vdd!) TGFF
I27 (CK_by_4 DATA\<3\> 0 D net13 vdd!) TGFF
I21 (CK_by_4 DATA\<1\> 0 B net15 vdd!) TGFF
I48 (AB DC 0 CK_by_2 vdd! net015) MUX_2
I37 (C D 0 CK_by_4 vdd! net016) MUX_2
I34 (A B 0 CK_by_4 vdd! net017) MUX_2
ends Serializer_Half_rate
// End of subcircuit definition.

// Library name: A_Thesis
// Cell name: Clock_Gen_4Phase
// View name: schematic
subckt Clock_Gen_4Phase CK0 CK_180 CK_270 CK_90 CLKB_in
CLK_in
I3 (CLKB_in net8 0 net013 net8 vdd!) TGFF
I18 (CLK_in net010 0 net7 net010 vdd!) TGFF
I44 (0 net015 CK_270 vdd!) Inv_600n
I39 (0 net017 CK_90 vdd!) Inv_600n
I69 (0 net023 net024 vdd!) Inv_600n
I32 (0 net020 net015 vdd!) Inv_600n
APPENDIX A. SCHEMATIC NETLISTS

I67 ( 0 net024 CK_180 vdd ! ) Inv_600n
I77 ( 0 net016 CK_0 vdd ! ) Inv_600n
I78 ( 0 net018 net016 vdd ! ) Inv_200n
I25 ( 0 net8 net020 vdd ! ) Inv_200n
I68 ( 0 net010 net023 vdd ! ) Inv_200n
I76 ( 0 net7 net018 vdd ! ) Inv_200n
I17 ( 0 net013 net019 vdd ! ) Inv_200n
I26 ( 0 net019 net017 vdd ! ) Inv_200n

ends Clock_Gen_4Phase
// End of subcircuit definition.

// Library name: A_Thesis
// Cell name: ANDx1
// View name: schematic

subckt ANDx1 A B Y
  NM3 ( Y net06 0 0 ) g45n1hvt w=(200n) l=45n nf=1 as=28f ad=
   =28f ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
   sca=169.02145 \n   scb=0.10920 scc=0.02100 m=(1)
  NM2 ( net06 A net18 0 ) g45n1hvt w=(200n) l=45n nf=1 as=28f ad=
   =28f ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
   sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
  NM0 ( net18 B 0 0 ) g45n1hvt w=(200n) l=45n nf=1 as=28f ad=
   =28f ps=680n pd=680n nrd=700m nrs=700m sa=140n sb=140n sd=160n
   sca=169.02145 scb=0.10920 scc=0.02100 m=(1)
  PM2 ( Y net06 vdd ! vdd ! ) g45p1hvt w=(230n) l=45n nf=1 as=
   =32.2f ad=32.2f ps=740n pd=740n nrd=608.696m nrs=608.696m sa=140n sb
   =140n sd=160n sca=155.75886 scb=0.10583 scc=0.01925 m=(1)
  PM1 ( net06 B vdd ! vdd ! ) g45p1hvt w=(230n) l=45n nf=1 as=
   =32.2f ad=32.2f ps=740n pd=740n nrd=608.696m nrs=608.696m sa=140n sb
   =140n sd=160n sca=155.75886 scb=0.10583 scc=0.01925 m=(1)
  PM0 ( net06 A vdd ! vdd ! ) g45p1hvt w=(230n) l=45n nf=1 as=
   =32.2f ad=32.2f \n
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APPENDIX A. SCHEMATIC NETLISTS

```
ends ANDx1
// End of subcircuit definition.

// Library name: A_Thesis
// Cell name: Inv_2uX2
// View name: schematic
subckt Inv_2uX2 GND IN OUT VDD
  NM0 (OUT IN GND GND) g45n1hvt w=(2u) 1=45n nf=4 as=220f ad=160f \\
    ps=3.88u pd=2.64u nrd=40m nrs=55m sa=140n sb=140n sd \\
    =160n \\
    sca=100.34014 scb=0.08228 scc=0.01192 m=(2)
  PM0 (OUT IN VDD VDD) g45p1hvt w=(2.26u) l=45n nf=4 as \\
    =248.6f ad=180.8f \\
    ps=4.27u pd=2.9u nrd=35.3982m nrs=48.6726m sa=140n sb=140n sd=160n \\
    sca=94.14966 scb=0.07872 scc=0.01116 m=(2)
ends Inv_2uX2
// End of subcircuit definition.

// Library name: gpdk045
// Cell name: resnsnpoly_2
// View name: schematic
subckt resnsnpoly_2_pcell_0 MINUS PLUS inh_bulkn
parameters segL=8u segW=1.5u
  R1 (PLUS MINUS inh_bulkn) g45rnsnp l=segL w=segW \\
  R0 (PLUS MINUS inh_bulkn) g45rnsnp l=segL w=segW
ends resnsnpoly_2_pcell_0
// End of subcircuit definition.

// Library name: A_Thesis
// Cell name: Inv_600nX4
// View name: schematic
subckt Inv_600nX4 GND IN OUT VDD
  NM0 (OUT IN GND GND) g45n1hvt w=(2.4u) 1=45n nf=4 as=264f ad=192f \\
    ps=4.48u pd=3.04u nrd=33.3333m nrs=45.8333m sa=140n sb=140n \\
    sd=160n sca=91.32138 scb=0.07706 scc=0.01082 m=(1)
```
APPENDIX A. SCHEMATIC NETLISTS

PM0 (OUT IN VDD VDD) g45p1hvt w=(2.72u) l=45n nf=4 as =299.2f ad=217.6f \nps=4.96u pd=3.36u nrd=29.4118m nrs=40.4412m sa=140n \nsb=140n \nsc=160n nca=85.86137 scb=0.07381 scc=0.01017 m=(1) ends Inv_600nX4
// End of subcircuit definition.

// Library name: A_Thesis
// Cell name: TB_SerDes_Pre_emp
// View name: schematic
I51 (CK CK_by_2 CK_by_4 DATA\<0\> DATA\<1\> DATA\<2\> DATA \<3\> S_DATA \S_DATA_B) Serializer_Half_rate
V3 (net2 0) vsource type=pulse edgetype=halfsine val0=1 val1 =0 \nperiod=1/freq_in rise=0.05/freq_in fall=0.05/freq_in \nwidth=0.45/freq_in
V5 (net1 0) vsource type=pulse edgetype=halfsine val0=0 val1 =1 \nperiod=1/freq_in rise=0.05/freq_in fall=0.05/freq_in \nwidth=0.45/freq_in
V7 (net015 0) vsource dc=600.0m type=dc
V4 (vdd! 0) vsource dc=1 type=dc
I8 (CK_0 CK_180 CK_270 CK_90 net2 net1) Clock_Gen_4Phase
I18 (CK_0 net3 0 CK_by_4 net3 vdd!) TGFF
I78 (CKB net021 0 Dly_DATA Dly_DATA_B vdd!) TGFF
I179 (0 net053 net057 vdd!) Inv_600n
I145 (0 net031 net034 vdd!) Inv_600n
I140 (0 net036 net035 vdd!) Inv_600n
I100 (0 net013 net020 vdd!) Inv_600n
I121 (0 net042 net028 vdd!) Inv_600n
I88 (0 net016 net021 vdd!) Inv_600n
I64 (0 net011 CK_by_2 vdd!) Inv_600n
I75 (0 net2 CK vdd!) Inv_600n
I82 (0 net1 CKB vdd!) Inv_600n
I69 (0 CK_90 net012 vdd!) Inv_600n
I71 (0 CK_270 net014 vdd!) Inv_600n
I67 (0 CK_180 net011 vdd!) Inv_600n
V0 (DATA\<3\> 0) vsource val1=1 val0=0 delay=0.25/freq_in \n
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APPENDIX A. SCHEMATIC NETLISTS

\[
\text{rise }= 0.05/\text{freq}_{\text{in}} \quad \text{fall }= 0.05/\text{freq}_{\text{in}} \quad \text{period }= 4/\text{freq}_{\text{in}} \\
\text{type}=\text{prbs} \\
\text{seed}= 7
\]

\[
V1 \text{ (DATA}<2\text{)}> 0 \text{ vsource vall}=1 \text{ val0}=0 \text{ delay}=0.25/\text{freq}_{\text{in}} \\
\text{rise }= 0.05/\text{freq}_{\text{in}} \quad \text{fall }= 0.05/\text{freq}_{\text{in}} \quad \text{period }= 4/\text{freq}_{\text{in}} \\
\text{type}=\text{prbs} \\
\text{seed}= 17
\]

\[
V2 \text{ (DATA}<0\text{)}> 0 \text{ vsource vall}=1 \text{ val0}=0 \text{ delay}=0.25/\text{freq}_{\text{in}} \\
\text{rise }= 0.05/\text{freq}_{\text{in}} \quad \text{fall }= 0.05/\text{freq}_{\text{in}} \quad \text{period }= 4/\text{freq}_{\text{in}} \\
\text{type}=\text{prbs} \\
\text{seed}= 61
\]

\[
V6 \text{ (DATA}<1\text{)}> 0 \text{ vsource vall}=1 \text{ val0}=0 \text{ delay}=0.25/\text{freq}_{\text{in}} \\
\text{rise }= 0.05/\text{freq}_{\text{in}} \quad \text{fall }= 0.05/\text{freq}_{\text{in}} \quad \text{period }= 4/\text{freq}_{\text{in}} \\
\text{type}=\text{prbs} \\
\text{seed}= 128
\]

I178 (0 net056 net053 vdd!) Inv_200n
I174 (0 net055 net056 vdd!) Inv_200n
I170 (0 S\_DATA_B net038 vdd!) Inv_200n
I168 (0 net038 net055 vdd!) Inv_200n
I158 (0 net040 net041 vdd!) Inv_200n
I156 (0 net041 net042 vdd!) Inv_200n
I162 (0 S\_DATA net039 vdd!) Inv_200n
I164 (0 net039 net040 vdd!) Inv_200n
I103 (0 S\_DATA_B net013 vdd!) Inv_200n
I102 (0 S\_DATA net016 vdd!) Inv_200n
I105 (net020 Dly\_DATA net031) ANDx1
I104 (net021 Dly\_DATA_B net036) ANDx1
I184 (0 net035 P\_edge vdd!) Inv_2uX2
I185 (0 net034 N\_edge vdd!) Inv_2uX2
R6 (0 net061 0) resnspoly\_2\_pcell\_0 segL=3.6u segW=1.5u
R5 (0 net063 0) resnspoly\_2\_pcell\_0 segL=3.6u segW=1.5u
R1 (net048 net064 0) resnspoly\_2\_pcell\_0 segL=600n segW=1.5u
R0 (net064 net049 0) resnspoly\_2\_pcell\_0 segL=600n segW=1.5u
I180 (0 net057 Serial\_DB vdd!) Inv_600nX4
I108 (0 net028 Serial\_DATA vdd!) Inv_600nX4
NM2 (net051 P\_edge net026 0) g45n1s vtw=(60u) l=45n nf=30 as =5.04p ad=4.8p \\
\quad ps=69.04u pd=64.8u nrd=1.33333m nrs=1.4m sa=140n sb =140n sd=160n \\
\quad sca=56.99756 scb=0.05691 scc=0.00695 m=(2)

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APPENDIX A. SCHEMATIC NETLISTS

NM3 (net037 N_edge 0 0) g45n1svt w=(40u) l=45n nf=20 as=3.44
  ps=47.44u pd=43.2u nrd=2m nrs=2.15m sa=140n sb=140n
  sd=160n
  sca=56.99756 scb=0.05691 scc=0.00695 m=(2)
NM1 (net048 Serial_DB 0 0) g45n1svt w=(20u) l=45n nf=10 as
  =1.84p ad=1.6p
  ps=25.84u pd=21.6u nrd=4m nrs=4.6m sa=140n sb=140n
  sd=160n
  sca=56.99756 scb=0.05691 scc=0.00695 m=(2)
NM0 (net015 Serial_DATA net049 0) g45n1svt w=(34u) l=45n nf
  =17 as=2.84p
  ad=2.84p ps=38.84u pd=38.84u nrd=2.45675m nrs
  =2.45675m sa=140n
  sb=140n sd=160n sca=56.99756 scb=0.05691 scc=0.00695
  m=(2)
MSL0 (net064 0 net063 0) msline l=70m w=800.00u h=159.000u t
  =35u eps=4.8
  fmax=2.25G
C1 (net063 0) capacitor c=200f
C0 (net064 0) capacitor c=200f
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e
  -12 temp=27
  tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1
  maxnotes=5 maxwarns=5
  digits=5 cols=80 pivrel=1e-3 sensfile="./psf/sens.
  output"
  checklimitdest=psf
modelParameter info what=models where=rawfile
  element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub