An Area Efficient 4Gb/s 3-Tap Decision Feedback Equalizer with Current-Integrating Summer

A Thesis Presented
by
Chen Zhang
to
The Department of Electrical and Computer Engineering
in partial fulfillment of the requirements for the degree of
Master of Science
in
Electrical and Computer Engineering

Northeastern University
Boston, Massachusetts

April 2016
To my family.
Contents

List of Figures v
List of Tables vii
List of Acronyms viii
Acknowledgments ix
Abstract of the Thesis x

1 Introduction 1

2 Basic Theory of Equalizer 3
  2.1 Backplane 3
  2.2 Intersymbol Interference 4
  2.3 Equalization on the Transmitter Side 5
  2.4 Equalization on the Receiver side 6
    2.4.1 Continuous Time Linear Equalizer 6
    2.4.2 Decision-Feedback Equalizer 6

3 Prior DFE Architecture 10
  3.1 Timing Constraint-Relaxed DFE 10
    3.1.1 First-Tap Speculation 11
    3.1.2 Half-Rate and Quarter-Rate Approach 12
    3.1.3 Soft-Decision 12
    3.1.4 Feed-Forward Approach 13
  3.2 Less Taps Involved without Sacrifice in Accuracy 14
    3.2.1 Floating-Tap Approach 15
    3.2.2 Combination with IIR Filter 15
  3.3 Tap Coefficients Adaptation 16
    3.3.1 Data-Based Adaptation 17
    3.3.2 Edge-Based Adaptation 17
    3.3.3 Edge and Data Combined Adaptation 17
List of Figures

2.1 Backplane channel .......................................................... 3
2.2 Signals before and after transmission line ................................. 4
2.3 The frequency response of pre-emphasis equalizer ...................... 5
2.4 The frequency response of continuous time linear equalizer .......... 7
2.5 Block diagram of a decision feedback equalizer ....................... 7
2.6 Channel output signal with ISI and recovered data after DFE .......... 9

3.1 Conventional 3-tap full-rate decision feedback equalizer ............... 10
3.2 Decision feedback equalizer with speculation method .................. 11
3.3 Half-rate decision feedback equalizer .................................... 12
3.4 1-tap soft-decision DFE architecture: (a) schematic and (b) timing diagram 13
3.5 Equalization with feed-forward and decision feedback ................. 14
3.6 Block diagram of floating-tap data engine ............................... 15
3.7 DFE with continuous-time IIR filter feedback tap ...................... 16
3.8 Different architectures of XDFEs: Coupled data and edge DFE; (b) Separated data and edge DFE 18

4.1 Block diagram of 3-tap half-rate DFE with first tap speculation ........ 19
4.2 Odd path flow diagram: Summer ......................................... 20
4.3 3-tap conventional resistor-based summer ............................... 21
4.4 3-tap current-integrating summer ....................................... 22
4.5 Current digital to analog converter ...................................... 23
4.6 Switched-capacitor summer design A .................................... 24
4.7 Switched-capacitor summer design B .................................... 25
4.8 Odd path flow diagram: Sample-and-Hold ............................... 25
4.9 Sample-and-Hold ............................................................ 26
4.10 Clock feedthrough effect suppressed by dummy switch ............... 27
4.11 Flow diagram: Slicer ....................................................... 27
4.12 Conventional regenerative comparator: (a) Pre-amplification (b) Regenerative latch 28
4.13 Flow diagram: Multiplexer ............................................... 29
4.14 Flow diagram: D Flip-Flop ............................................... 29
4.15 D flip-flop circuit .......................................................... 30
4.16 Simplified CMOS D-latch ................................................ 31
4.17 Clocking scheme of D flip-flop

5.1 3-tap half-rate first-tap speculative DFE architecture with proposed current-integrating summer

5.2 Proposed current-integrating summer with two separated stages

5.3 Simplified switched-capacitor stage with clocking scheme

5.4 The implementation of adjustable first-tap voltage

5.5 Diagram for summer operation

6.1 Channel connection

6.2 Channel output waveform (a)

6.3 Channel output waveform (b)

6.4 Channel loss

6.5 A single pulse signal (a) before channel (b) after channel

6.6 Eye diagram (a) before DFE (b) after DFE

6.7 XOR gate for error detection

6.8 BER bathtub curve for 28dB channel at 4 Gb/s with DFE switched off

6.9 BER bathtub curve for 28dB channel at 4 Gb/s with DFE active

6.10 Signal waveforms of essential nodes in DFE (a)

6.11 Signal waveforms of essential nodes in DFE (b)

6.12 Power consumption of each block in DFE
List of Tables

6.1 Power consumption of each block ............................................. 56
6.2 Prior 180nm DFE works ......................................................... 58
List of Acronyms

**DFE** Decision Feedback Equalizer.

**ISI** Inter-symbol Interference.

**UI** Unit Interval. The unit interval is the minimum time interval between condition changes of a data transmission signal, also known as the pulse time or symbol duration time [1].

**IIR** Infinite Impulse Response.

**LMS** Least Mean Square. The Least Mean Square algorithm is an algorithm which minimizes mean square error between two signals.

**DAC** Digital to Analog Converter.

**CDR** Clock and Data Recovery.

**BER** Bit-Error Rate.
Acknowledgments

Here I would like to express my deepest gratitude to my advisor, Prof. Yong-Bin Kim, for offering me the opportunity in his group and the support for my Master study. I appreciate his immense knowledge and skill in many areas and his assistance in my thesis writing. This thesis could not have been finished without his guidance, patience and motivation. Moreover, I would like to thank the rest of my thesis committees, Prof. Nian X. Sun and Prof. Fabrizio Lombardi, for their support and insightful comments.

I am also so thankful to my labmates in Northeastern University High Performance VLSI lab, Yongsuk Choi and Gyunam Jeon, for their selfless help and patient guidance.

Last but not least, thanks go to my parents for their love and unconditional support throughout my life. Thanks for always standing by my side.
Abstract of the Thesis

An Area Efficient 4Gb/s 3-Tap Decision Feedback Equalizer with Current-Integrating Summer

by

Chen Zhang

Master of Science in Electrical and Computer Engineering
Northeastern University, April 2016
Prof. Yong-Bin Kim, Adviser

As the requirement of wire line applications increases, the demand for higher data transmission bandwidth is continuously exploding. While the on-chip speed has led to a growing interest in developing faster I/O for chip-to-chip and backplane communication, bandwidth limitation has not shown dramatic improvement over the years. Consequently, it presents great challenges to achieving multi-gigabits per second signaling rate. The inherent undesirable electrical characteristics of channel and issues induced by neighboring channels such as crosstalk severely degrade the transmitted signal.

According to prior research works, Intersymbol Interference (ISI) is the dominant noise for high-speed backplane transmission, which makes one data bit broaden to greater than one Unit Interval (UI). High possibility of error is shown in data detecting at receiver due to the interference between the current data bit and the accumulated “tail”s which come from its preceding bits. Nowadays, there are number of equalization methods that are applied to both transmitter and receiver to eliminate the effect of ISI. Among these equalizers, Decision Feedback Equalizer (DFE) is the most widely-used discrete-time equalizer, which stores and feeds back the decisions it has made for the previous bits and subtracts the ISI of these stored bits from the current signal. The DFE shows a good advantage that it reduces signal distortion without amplifying noise or crosstalk.

In this research, an area efficient decision feedback equalizer with a new current-integrating summer in standard CMOS 180nm technology node is designed and simulated in Cadence. Since the feedback timing constraint for the first tap is one of the greatest challenge in DFE design, first-tap speculative architecture is commonly used to relax this timing margin. For conventional first-tap speculative half-rate DFE, four parallel paths have exactly the same hardware and the main part of summer in two speculative paths is redundant. In order to optimize the structure, a new current-integrating summer with switched-capacitors is proposed. Unlike the conventional one, the proposed
summer separates the first speculative tap which allows two parallel paths for speculation to be driven by a single summer instead of two. The proposed DFE consumes 17.4mW with 1.8V supply voltage when equalizing 4Gb/s data passed over a channel with 28dB loss at 2GHz. Simulation result shows that a horizontal 40% eye opening at BER less than $10^{-6}$ is derived.
Chapter 1

Introduction

As the requirement of wire line applications increases, the demand for higher data transmission bandwidth is continuously exploding. While the on-chip speed has led to a growing interest in developing faster I/O for chip-to-chip and backplane communication, bandwidth limitation has not shown dramatic improvement over the years. Consequently, it presents great challenges to achieving multi-gigabits per second signaling rate. The undesirable electrical characteristics of channel and issues induced by neighboring channels such as crosstalk severely degrade the transmitted signal. For high-speed backplane transmission, Inter-symbol Interference (ISI) is the dominant noise, which makes one data bit broaden to greater than 1 Unit Interval (UI). High possibility of error is shown in data detection at receiver due to the interference between the current data bit and the accumulated “tail”s which come from its preceding bits. Nowadays, there are number of equalization methods applied to either transmitter or receiver to eliminate the effect of ISI. Among these equalizers, Decision Feedback Equalizer (DFE) is the most widely-used discrete-time equalizer, which stores and feeds back the decisions it has made for the previous bits and subtracts the ISI of these stored bits from the current signal. The DFE shows a good advantage that it reduces signal distortion without amplifying noise or crosstalk.

However, most of those researches of DFE published so far have disadvantages in efficiency, area or power. This research proposed a novel DFE architecture that demonstrates the effectiveness of DFE as well as the improvement in terms of area and power comparing to the conventional approach.

In DFE implementation, the feedback timing constraint for the first tap is one of the greatest challenge. To relax this timing margin, first-tap speculative architecture is commonly used. For conventional first-tap speculative half-rate DFE, four parallel paths have exactly the same hardware and the main part of summer in two speculative paths is redundant. In order to optimize the structure,
CHAPTER 1. INTRODUCTION

A novel current-integrating summer with switched-capacitors is proposed in this research. Unlike the conventional one, the proposed summer separates the first speculative tap, which allows two parallel paths for speculation to be driven by a single summer instead of two.

The remaining of the paper is organized as following. Chapter 2 introduces the motivation and background of decision feedback equalizer. After the characteristics of backplane channel and ISI distortion are explored, different equalization methods used to eliminate the attenuation generated by the channel are presented. Among these equalizers, the decision feedback equalizer is emphasized at the end of this chapter.

A brief overview of the current state-of-the-art involving DFE is shown in Chapter 3. DFE architectures are classified in tradeoffs among output signal accuracy, timing constraint relaxing, and area / power consumption. The advantages and disadvantages of each type are also discussed. In addition, different methods for coefficient adaptation is shortly introduced at the end.

In Chapter 4, circuits and functions of main components in conventional DFE are described separately. Since the summer block is the most important part of DFE where the subtraction of ISI is implemented, it is emphasized at the very beginning of this chapter. Two types of conventional summer are introduced, which help the understanding of the proposed summer presented in Chapter 5. All other components except summer used in the proposed DFE are then introduced in sequence.

The proposed current-integrating summer is presented in Chapter 5, where the circuits and the operation of two stages inside are clearly explained. Three important design considerations need to be considered in implementation. They are charge sharing effect, implementation of voltage source, and clock signal requirement.

Chapter 6 presents the simulation results of the proposed DFE. The characteristics of channel model used in this work are introduced first for a better understanding of the DFE performance. Eye diagrams, Bit-Error Rate (BER) results, and power consumption of each component in DFE are derived in this chapter.

In Chapter 7, the conclusions for proposed DFE are presented and the improvements and future research direction is described.
Chapter 2

Basic Theory of Equalizer

2.1 Backplane

A high-speed backplane channel is a point-to-point connection that can be modeled as a long multi-layer, multi-link PCB channel to interconnect a transmitter and a receiver attached with connectors on either end [2] as shown in Figure 2.1. The main mechanism for signal degradation in backplane transmission is insertion loss, such as conductor loss, dielectric loss and return loss. In addition, noises like reflections and crosstalk from other channels also affect the data transmission.

Figure 2.1: Backplane channel (Source [2])

The main effect of these loss mentioned above is ISI (Intersymbol interference) shown
CHAPTER 2. BASIC THEORY OF EQUALIZER

in the channel output. In the following parts of this chapter, the characteristics of ISI and different methods of equalization are introduced in detail.

2.2 Intersymbol Interference

High-speed signal is attenuated and distorted during transmission through backplane channel. As a form of distortion in which one symbol interferes with subsequent symbols, ISI is dominant over cross-talk and other effects. The spreading of the pulse beyond its allotted time interval causes it to interfere with neighboring pulses. As shown in Figure 2.2, an ideal pulse signal transmitted through channel is degraded and expanded when it arrives at the receiver. The ISI which overlaps with the preceding and succeeding signal bits are called post-cursor ISI and pre-cursor ISI.

![Diagram of Transmitter, Channel, and Receiver](image)

Figure 2.2: Signals before and after transmission line

Two main characteristics of ISI is going to be analyzed here. One is the “tail” length of a single pulse signal after being transmitted through channel. The longer the “tail” is, more data bits behind the current bit will be influenced. For a specific channel, as the input signal frequency increases, the current bit expands more backward. Besides, although the input signal with the same frequency is transmitted through, channel with more severe loss also shows the same effect. Another
one is the magnitude of ISI. If the same channel is used, although the output signal certainly shows a larger amplitude when a larger input signal is transmitted, the ratio between the magnitude of “tail” and main pulse remains the same value. Therefore, from the analysis mentioned above, it is not hard to find that ISI produced by a single data bit at channel output is unchangeable when a stable input signal is transmitted through a specific channel.

Since the ISI that comes from previous data bits affects the current bit, the presence of ISI makes it possible for the data detector in receiver to have a wrong decision, which can significantly degrade the bit error rate performance of receiver when channel loss is severe. To prevent the errors caused by ISI, different types of equalizers are introduced both on the transmitter and receiver side.

2.3 Equalization on the Transmitter Side

Pre-emphasis (de-emphasis) method are well-known on the transmitter side. Due to the dielectric loss and other effects, the channel works as a lowpass filter. High-frequency component of the input signal is attenuated significantly compared with low-frequency content. Therefore, by boosting the gain of high-frequency content (or reducing the low-frequency content), the pre-emphasis (de-emphasis) equalizer can help derive a uniform frequency response at the input of receiver in a specific desired frequency range, which is shown in Figure 2.3. The benefit of this method is relative simplicity and low power [2].

![Figure 2.3: The frequency response of pre-emphasis equalizer](image-url)
CHAPTER 2. BASIC THEORY OF EQUALIZER

The implementation of pre-emphasis (de-emphasis) is achieved by feedback. Delayed inverse of transmitted signals are added back to the original signal with proper weight to pre-distort the input signal in the opposite direction of the distortion that is going to suffer in the channel, so that compensates the ISI in the current data from nearby signals.

However, the pre-emphasis (de-emphasis) has several limitations. Since it increases the signal edge rate, the crosstalk on the neighboring channels is amplified too. Meanwhile, because the pre-emphasis only emphasizes the transition bits, the discontinuity along the channel is more complicated than the situation without pre-emphasis [4].

2.4 Equalization on the Receiver side

Apart from the pre-emphasis (de-emphasis) methods, there are two common types of equalizers used in receiver side for ISI compensation, which are continuous time linear equalizer (CTLE) and decision feedback equalizer (DFE).

2.4.1 Continuous Time Linear Equalizer

The basic idea of continuous time linear equalizer is described in Figure 2.4. Since the gain of channel with short bandwidth drops steeply at a specific frequency that is much smaller than the frequency of transmitted signal, the high-frequency input signal is attenuated severely. To boost the gain of high-frequency content, CTLE works as a corresponding frequency response function to be multiplied with channel response. Consequently, CTLE effectively helps widen the bandwidth and flatten the channel response. Besides, the poles and zeros inside the CTLE frequency response function are well-selected by changing the value of resistor $R$ and capacitor $C$ in circuit. CTLE usually shows a low power consumption, but its disadvantage is that it amplifies the high-frequency noise at the same time.

2.4.2 Decision-Feedback Equalizer

Unlike the CTLE, which simply amplifies the high-frequency content, decision feedback equalizer (DFE) compensates channel attenuation based on the previous decisions without noise enhancement. Nowadays, DFE is widely used to eliminate the post-cursor ISI in receiver side. The block diagram of DFE is shown in Figure 2.5
CHAPTER 2. BASIC THEORY OF EQUALIZER

Figure 2.4: The frequency response of continuous time linear equalizer

Figure 2.5: Block diagram of a decision feedback equalizer
CHAPTER 2. BASIC THEORY OF EQUALIZER

For a specific channel through which a digital signal sequence is transmitted, the post-cursor ISI in the received current data bit produced by the bits from n-UI before are stable. Assuming that no signal is sent into the channel before the first “1” in the sequence and the post-cursor ISI only affect two succeeding bits, an example of “1110111” sequence is given in Figure 2.6 where only the signal at the positive node of differential input signal is presented. Due to the influence of ISI from previous data bits, the amplitude of “0” is so small that wrong decision is possible to be made by the receiver without DFE.

To subtract these accumulated ISI in current bit one by one, the previous digital bits, which have been already regenerated by DFE, will be fed back and summed with the current signal after multiplied with some proper coefficients. The coefficients used in DFE can be adaptively adjusted with the help of least mean square (LMS) algorithm. Thus DFE is able to cancel ISI without amplifying noise, which outperforms traditional linear equalizer.

However, since the decision for the current data bit strongly depends on previous detections especially if the tap coefficients are large in order to compensate severe channel loss, the performance of DFE will has a high probability to show great degradation when incorrectly decisions are fed back. The phenomenon that a single bit error produces a very long burst of errors is called error propagation. Some research has concentrated on minimizing error propagation in DFE and several techniques have been presented [5] [6].
Figure 2.6: Channel output signal with ISI and recovered data after DFE
Chapter 3

Prior DFE Architecture

The principle of decision feedback equalizer was first introduced by Austin in 1967 [7]. The main challenges faced in implementing DFE since then mainly come from three aspects, which are the first-tap feedback timing constraint, area and power consumption, and the tradeoff between tap number and accuracy of DFE. The most conventional full-rate DFE is shown in Figure 3.1. On this basis, researchers struggled to overcome these problems and presented a number of new DFE architectures. In this chapter, a glance at the state-of-the-art of decision feedback equalizer is given.

![Figure 3.1: Conventional 3-tap full-rate decision feedback equalizer](image)

3.1 Timing Constraint-Relaxed DFE

The first main challenging part of DFE design is the first-tap feedback timing constraint. Because the decision of the previous data bits are fed back and added to the current signal after
CHAPTER 3. PRIOR DFE ARCHITECTURE

multiplied with some proper tap coefficients, the previous decisions should be settled down before
the current bit comes through. Therefore, the first tap has the most stringent timing constraint that
the operations of summer and slicer must be completed within one UI which is shown as:

\[ \tau_{\text{summer}} + \tau_{\text{slicer}} \leq 1\text{UI} \]  \hspace{1cm} (3.1)

Several different DFE architectures have been presented aiming at relaxing the timing requirement of
the first feedback tap.

3.1.1 First-Tap Speculation

The most commonly used method to relax the first-tap timing constraint is first-tap spec-
ulation, which is also known as loop-unrolling or look-ahead method. As shown in Figure 3.2,
the first-tap coefficient is added on or subtracted from the current received data in advance in two
parallel paths (strong-zero path and strong-one path), assuming the previous data bit is “0” or “1”,
respectively. After the decision for the previous bit is ready, it will be fed back to select one of these
two paths by a 2-to-1 multiplexer. Therefore, the most stringent timing constraint for the first-tap
speculative DFE is expanded from 1UI to 2UI, as shown in:

\[ \tau_{\text{summer}} + \tau_{\text{slicer}} + \tau_{\text{multiplexer}} \leq 2\text{UI} \]  \hspace{1cm} (3.2)

This approach was first proposed in [8] in 1992.

Figure 3.2: Decision feedback equalizer with speculation method(Source [9])

This speculation method is often limited to the first tap, because the number of summer,
slicer and multiplexer increases exponentially with the increase of speculative taps. However, when
DFE is implemented with very high frequency signal, this method is a good choice because it can be
easily introduced to the second tap or even the third tap [10].
3.1.2 Half-Rate and Quarter-Rate Approach

Half-rate approach where the DFE operating at half the data rate is also widely used [11] [12]. The block diagram is depicted in Figure 3.3. In the architecture of half-rate DFE, the conventional full-rate one is divided into two parallel paths, which are odd and even paths. Two parallel paths work separately in different clock phases. When one path is eliminating ISI, another path is in reset phase waiting for its turn to work. It should be noted that even though half-rate DFE operates with half-rate clock signal, the requirement for first tap settling time is still 1UI, which is the same as the full-rate DFE. However, it removes the clock speed limitation of full-rate DFE where the frequency of clock is twice as high as the input signal frequency. On the other hand, it also mitigates the double data rate up-conversion multiplexer from the DFE critical timing path to a certain extent easing the stringent timing requirement [13].

![Figure 3.3: Half-rate decision feedback equalizer (Source [11])](image)

In addition, quarter-rate approach has also been introduced to further relax timing constraint when DFE is operating with higher-frequency input signal [9]. In recent designs, the half-rate method and first-tap speculation are commonly used together.

3.1.3 Soft-Decision

In [11], [9], apart from half-rate and quarter-rate approach, soft-decision method is also introduced to speed up the critical first-tap timing loop. The schematic and timing diagram for soft-decision operation is shown in Figure 3.4.

In period (i), even when latch L1 is still working on amplifying, the output of L1 is sent to summer S2 at the same time. Change at the output of L1 helps switch the corresponding differential
pair in S2 to establish the current level in the summer in advance before integration begins. Although S2 is in its reset phase during this time, its current still responds to the change in feedback signal coming from another path. Since L1 has not entered its regeneration mode, the bit decision made by the latch during period (i) is referred to as a “soft-decision”. Once latch L1 enters its regeneration mode which is shown in period (ii), a hard bit decision is made by L1. Meanwhile, summer S2 begins to integrate and the “soft-decision” made by L2 by tracking the output of S2 is sent into S1. The operation of DFE in period (iii) is the same as the one in period (i). This method effectively speeds up the first-tap feedback time [11].

3.1.4 Feed-Forward Approach

Another approach to relax the timing constraint for the first tap is to use feed-forward equalization in decision feedback equalizer. In [14], the first FFE tap feeds forward the previous 1-bit sampled voltage as shown in Figure 3.5. ISI in post-cursors is equalized by subtracting voltage which is proportional to the reversed signal of previous data bit. The application of FFE allows a full-elimination of ISI in the first post-cursor because by which the proportion is determined and part of ISI in the 2nd to 4th can be decreased at the same time. Besides, the remaining ISI are equalized by
three feedback taps of conventional DFE. Since the FFE is used for the first tap equalization where no feedback loop is required, the timing margin for feedback is relaxed from 1UI to 2UI \[14\].

![Diagram of equalization with feed-forward and decision feedback](image)

**Figure 3.5**: Equalization with feed-forward and decision feedback (Source \[14\])

### 3.2 Less Taps Involved without Sacrifice in Accuracy

It is essential to choose a proper number of DFE taps to eliminate ISI. As the increasing of channel loss and operational frequency, the DFE requires more taps to compensate the severer post-cursor ISI. However, the guarantee of result accuracy is at the cost of area and power consumption. In the following part, some methods concentrating on increasing the accuracy of DFE efficiently with less area and power are introduced.
CHAPTER 3. PRIOR DFE ARCHITECTURE

3.2.1 Floating-Tap Approach

Floating-tap DFE is suitable for channels with substantial reflections that occur far away from the main cursor. [15] shows that the DFE must cover tap positions higher than 40 UI to remove reflection-induced ISI, which is difficult to implement with conventional DFE. By introducing an extra floating-tap data engine for floating taps, the positions of these taps can be adapted to the four tap locations where greater coefficients for correction are needed. However, since the reflection peak is impossible to always locate at integer of unit interval, the 1UI-spacing DFE that only can remove the ISI exactly at kUI cannot completely remove the reflection peak in the middle of unit interval. The block diagram of floating-tap data engine is shown in Figure 3.6. It consists of a position adaptation engine, a 32bit register & tap selection logic, a data multiplexer, and a data rotator [15].

![Block diagram of floating-tap data engine](Source [15])

3.2.2 Combination with IIR Filter

For the input signal with severe post-cursor ISI, an exponentially decaying function can be utilized to represent the long “tail” after main cursor. Instead of involving a large number of feedback taps in conventional DFE, one single Infinite Impulse Response (IIR) tap in this new DFE can compensate the effects of multiple post-cursors [16], [17]. Without the sacrifice of DFE accuracy, the reduction of tap number helps decrease the DFE complexity since the adaptation for
only one coefficient (1-pole) in IIR tap is required. The architecture of DFE with IIR filter is shown in Figure 3.7.

![DFE with continuous-time IIR filter feedback tap](source)

Figure 3.7: DFE with continuous-time IIR filter feedback tap (Source [16])

However, the performance of one pole IIR filter used in DFE is very limited. Since the post-cursor ISI in most cases is very complicated, it is impossible to be fully compensated by only one coefficient. The solution for this problem is to involve more poles and zeros in IIR filter. After considering the tradeoff between the increasing complexity and the mean square error when fitting the post-cursor ISI to different pole-zero model, a 2-pole+1-zero IIR model is selected in [18]. In addition, another work concentrated on the decision of feedback taps number and IIR filter taps number is also introduced in [17].

Therefore, after the careful consideration of the factors mentioned above, this DFE architecture combined with IIR filter is a good candidate for long “tail” ISI compensation with low complexity.

### 3.3 Tap Coefficients Adaptation

For different channel and input signal, the magnitude of the current bit’s post-cursor ISI distributed at its following position is different. In order to eliminate ISI in signals transmitted through different channels properly, an extra device is needed to adapt the tap weights automatically. Two methods are going to be introduced here. One is the data-based adaptation, which is the conventional one used in most adaptive DFE. Another one is the edge-based or jitter-based adaptation. Sometimes, these two methods are combined to adapt tap weights together.
3.3.1 Data-Based Adaptation

For data-based adaptation, Least Mean Square (LMS) algorithm is the most popular one, which minimizes mean squared error between the output signal and referenced signal at the eye center. Let \( \varphi(t) \) be the single bit response of the channel and \( \varphi(t_s) \) be the referenced signal. Moreover, the output signal of DFE at the m-th data sample is represented by \( z_m \). D-DFE chooses the tap weights to minimize \( E\{(z_m - \varphi(t_s))^2\} \) which means to maximize the eye-opening voltage margin [19]. Other adaptive algorithms also can be used in DFE adaptation works. Theses are MBER algorithm, RLS algorithm, and CMA algorithm, which will not be introduced here.

3.3.2 Edge-Based Adaptation

The main architecture of edge-based and data-based adaptive DFE are nearly the same. In contrast, the edge-based adaptation concentrates on the ISI on edge samples. Because the ideal value at the edge of data transition is zero, the tap weights in E-DFE are decided to minimize \( E\{z_{m-1/2}\} \), where \( z_{m-1/2} \) is the m-th transition edge sample [19]. Therefore, the eye-opening timing margin is maximized. If Clock and Data Recovery (CDR) is involved in the circuit, the output clock of the CDR will be cleaner by reducing the timing uncertainty at the input since the edge samples are the input to the CDR [20], which is its advantage compared with data-based adaptation.

3.3.3 Edge and Data Combined Adaptation

In [20], a combined DFE (XDFE) is presented, which consists of two separated filters for data path and edge path. Because the new DFE proposed in [20] solved the problem of coupled tradeoff between voltage margin and timing margin, this new DFE can derive a better output for CDR without the sacrifice in the voltage margin of data sample. The architecture of edge and data combined DFE is shown in Figure 3.8.
Figure 3.8: Different architectures of XDFEs: Coupled data and edge DFE; (b) Separated data and edge DFE (Source: [20])
Chapter 4

Conventional DFE Composition

As introduced in Chapter 3, many methods to relax the timing margin of first feedback tap are presented in recent design. Because of the demand of increasing operation speed of devices, the combination of these methods is commonly used. Therefore, as shown in Figure 4.1, the conventional DFE composition to be introduced in this chapter is the half-rate DFE with first tap speculation method. It consists of sample-and-hold, summer, slicer, D flip-flop and multiplexer blocks. The circuit and function of each block is introduced in the following sections.

Figure 4.1: Block diagram of 3-tap half-rate DFE with first tap speculation
4.1 Summer

The most essential composition of DFE is the summer block where the subtraction of ISI is implemented. The previous three data bit decisions (3-tap DFE) are fed back with weighted tap coefficients and added together with the current data bit in the summer. The flow diagram for summer in odd path is shown in Figure 4.2. Three popular summer designs are going to be presented here.

4.1.1 Resistor-based summer

Resistor-based summer is the most conventional summer design used in DFE, which is shown in Figure 4.3. The basic idea of summer is to convert the input voltage signal to current by a differential pair and to sum it with weighted tap currents. At the same time, the differential voltage output signal is generated by resistive loads.

The operation of taps is easily understood. For example, if the decision for the previous data bit is “1”, the left one (N_{1p}) of the NMOS transistor pair to control the first tap will be turned on and the right one (N_{1n}) will be turned off, which means a specific value of current (I_{H1}) will flow through the positive path but the negative path will be blocked. This much current discharged from the positive node results in a differential output with smaller difference than before. Therefore, by correctly selecting the current value (I_{H1}), which is the first tap coefficient, the ISI in current signal produced by the previous data bit is eliminated successfully. By the same token, first tap current (I_{H1}) will be discharged at the negative node to increase the output voltage difference if the decision for the previous data bit is “0”. The settling time of resistor-based summer is determined by the load resistor (R_{L}) and load capacitor (C_{L}) at the output of summer.
4.1.2 Current-Integrating Summer

Compared to the resistor-based summer, current-integrating summer, shown in Figure 4.4 replaces the two resistor loads with active loads. These two PMOS transistors, controlled by clock signal, separate the operation of summer into reset phase and evaluation phase. In reset phase, both of the summer output nodes are pulled up to supply voltage which guarantees the zero voltage difference between two output nodes at the start of evaluation phase. Then during the following phase, current which flows through the main path and taps makes the output voltage of two nodes drop. The dropping rate of voltage at two output nodes differs from each other because of the difference in input signals and the control on taps. Therefore, by adding the tap current depending on the decisions for previous data bits to the current signal, the ISI-free output is finally derived.

To fully cancel the post-cursor ISI in different situation, alterable tap currents (tap coefficients) are determined by current Digital to Analog Converter (DAC)s. A simple 4-bit current DAC is shown in Figure 4.5. The current DAC, which is also called as IDAC, mainly consists of a current mirror. With the help of a switch array, different current values \(2^4\) for 4-bit case) can be achieved by turning on or off the switches in multiple paths with different code sequences. Apart from the IDAC block, to derive an adaptive DFE, a digital loop algorithm such as SS-LMS algorithm is needed and works with IDAC together to change tap coefficients automatically. The digital loop algorithm computes code sequences depending on the feedback decisions for previous data bits and these codes are then sent into IDAC to generate proper tap current values. Although the time for convergence differs when different algorithms are applied, stable coefficient values are finally achieved after a short period of time, which is exactly the representation of ISI from the previous bits. Current
CHAPTER 4. CONVENTIONAL DFE COMPOSITION

DAC and digital loop algorithm are not implemented in this work. The proper tap coefficients are determined depending on the simulation result of summer.

As shown in Figure 4.4 between the two active loads, an extra PMOS transistor is employed at the pull-up part of differential pair. Because the input signal for differential pair and feedback signals for taps are not zero during reset phase, the main current and tap current keep flowing. Controlled by clock signal, this extra transistor is turned on together with the two pull-up PMOS transistors to guarantee the equal of two differential output at the end of reset phase.

A comparison between resistor-based summer and current-integrating summer is presented in [11]. A summer based on current integration without settling time requirement can achieve the same desired common-mode voltage at the output using three times less bias current than a resistive summer when 5% settling accuracy requirement in the resistive summer is predicated. Therefore, current-integrating summer is adopted in this work because of its advantage of lower power consumption and no settling time requirement.

4.1.3 Switched-Capacitor Summer

Instead of summing the tap current with the main current in differential pair, the switched-capacitor summer involves the effect of taps by adding a charge either on the positive or negative node. There are two kinds of switched-capacitor summers, and they are introduced in [22] and [23]. [22] presents the first kind of switched-capacitor summer implementation. As shown in
CHAPTER 4. CONVENTIONAL DFE COMPOSITION

Figure 4.5: Current digital to analog converter (Source [21])

Figure 4.6, this design is more similar to the current-integrating summer mentioned above. Tap coefficients are added to either positive node or negative node depending on the decisions for previous data bits in the form of tap charge instead of tap current. For the same purpose that selecting proper tap coefficients, the specific tap charge value is determined by the size of capacitors with constant reference voltage or by an digitally adjustable voltage source with capacitors in constant size.

Compared to the current-integrating summer, this switched-capacitor summer design with the charge feedback method has a main advantage. For the current-integrating summer, the most stringent feedback timing margin is limited in 1UI since the decision for previous data bit has to settle down before the start of integration phase. However, in the operation of switched-capacitor summer, the correction can happen until right before the sampling instant, giving a much relaxed feedback timing margin [22].

In [23], another switched-capacitor summer design is introduced. For this summer architecture, there are two operation phases, which are sampling phase and equalize phase. During the sampling phase, switches S1d and S1 in Figure 4.7 are closed to set the voltage across $C_s$ to $V_i - V_{CM}$. In the next equalize phase, switches S1d and S1 are open. Meanwhile, S1B is turned on to connect the left terminal of $C_s$ to $V_{CM} + \alpha V_{ref}$, which represents the DFE tap. Assuming that the capacitance
CHAPTER 4. CONVENTIONAL DFE COMPOSITION

Figure 4.6: Switched-capacitor summer design A (Source [22])

$C_s$ is much larger than the input capacitance $C_i$ of next stage to ignore charge sharing effect, the new output voltage of summer in equalize phase can be expressed by

$$V_{\text{out}} = 2V_{\text{CM}} - V_i + \alpha V_{\text{ref}}$$  \hspace{1cm} (4.1)

This equation shows that the ISI can be successfully eliminated by adding the reference voltage $V_{\text{ref}}$ on positive or negative node.

Unlike the current-based summers, the switched-capacitor summer does not require a high bias current. Therefore, it is possible to achieve high power efficiency [23].

4.2 Sample-and-Hold

As the first stage of DFE, the flow diagram of sample-and-hold in odd path is shown in Figure 4.8. Because the input signal keeps changing during the evaluation phase of summer, the decrease or increase of signal amplitude can lead to an unexpected result at the output of summer. Sample-and-hold is used to hold input signal at the middle of each pulse, which helps keep the amplitude of input to be stable at its highest value in each UI during summer’s integration. As shown in Figure 4.9, transmission gate, one of the most popular sample-and-hold designs, is used in this work.

Apart from the transmission gate that consists of a PMOS and NMOS transistor in the middle, four “dummy” switches, whose source and drain are connected, are added at two sides.
CHAPTER 4. CONVENTIONAL DFE COMPOSITION

Figure 4.7: Switched-capacitor summer design B (Source [23])

Figure 4.8: Odd path flow diagram: Sample-and-Hold
Obvious output glitches can be observed every time when transmission gate is turned off due to the channel charge injection and clock feedthrough effect. The details are explained in [24]. When switch turns off, approximately half of the channel charge is injected to the left and another half to the right side, introducing an error at the output. This phenomenon is called channel charge injection. Besides, the clock feedthrough effect also introduces an error at the output voltage due to the clock transitions coupled by the gate-drain or gate-source overlap capacitance of switch. Therefore, “dummy” switches, driven by complementary clock signal, are added to absorb the injected channel charge to form its own channel. If the width and length of main transistor is expressed as $W_1$, $L_1$ and $W_2$, $L_2$ for “dummy” switches, the relationship should be $W_1 = 2W_2$, $L_1 = L_2$ to equalize the charge injected and absorbed. However, because the assumption of equal splitting of charge between source and drain is invalid, this method can only partly solve the problem caused by channel charge injection. Fortunately, the clock feedthrough effect can be totally suppressed as shown in Figure 4.10.

4.3 Slicer

The slicer used in this work is regenerative comparator as shown in Figure 4.12. The comparator is divided into two parts, which are a pre-amplification (shown in Figure 4.12 (a)) and a regenerative latch (shown in Figure 4.12 (b)). The gain of the preamplifier helps reduce the
CHAPTER 4. CONVENTIONAL DFE COMPOSITION

Figure 4.10: Clock feedthrough effect suppressed by dummy switch (Source [24])

Figure 4.11: Flow diagram: Slicer
CHAPTER 4. CONVENTIONAL DFE COMPOSITION

input-referred offset of the latch and also decrease the probability of metastability [25]. However, for comparators operating in multi-gigahertz sampling frequencies, a low preamplifier gain is required.

Figure 4.12: Conventional regenerative comparator: (a) Pre-amplification (b) Regenerative latch

The operation of pre-amplification part is divided into reset phase and operational phase, which is similar to the summer mentioned above. When clock is low, the NMOS transistor at the bottom (N4) is turned off and two PMOS transistors (P2 and P3) controlled by clock signal are turned on to pull the two output nodes up to supply voltage. In the operational phase where clock signal is high, P2 and P3 are turned off to stop the reset process. Since the initial condition is that both output nodes are at high level. For the transistors in the cross-coupled inverters, P0 and P1 are off and N0 and N1 are on. Besides, because N4 controlled by clock signal is turned on at the same time, current determined by the differential input signal $V_{in}$ starts to flow through N2 and N3 to discharge two output capacitors. Once one of the output node drops to $V_{DD} - |V_{TP}|$, where $V_{TP}$ is the threshold voltage of P0 and P1, positive feedback of cross-coupled inverters N0, P0 and N1, P1 begins [26]. The output node with a larger input signal sent in will be pull down to ground and the discharging process for another node will be stopped immediately. Finally, a small difference between the current through N2 and N3 converts to a much larger output voltage [27].

After the difference between differential output is amplified in pre-amplification stage, it is sent to a regenerative latch, which helps regenerate the low level signal to ground and the high level signal to supply voltage. The circuit is shown in Figure 4.12(b).
CHAPTER 4. CONVENTIONAL DFE COMPOSITION

4.4 Multiplexer

![Multiplexer Diagram](image)

Figure 4.13: Flow diagram: Multiplexer

There are two multiplexer blocks located in different clock paths in half-rate DFE. One is at the even path and another is at the odd path. After the decision is derived separately at the strong one path or strong zero path by assuming the previous data bits is “1” or “0”, these two decisions are then sent into a 2-to-1 multiplexer and the selection input which is the decision for the previous data bit comes from another multiplexer output at the opposite clock path. Finally, the correct result can be derived at the multiplexer output. A simple 2-to-1 multiplexer is used in this work.

4.5 D Flip-Flop

![D Flip-Flop Diagram](image)

Figure 4.14: Flow diagram: D Flip-Flop

Since the decisions for previous data bits are required to be fed back and added to the current signal after multiplying with proper coefficients, the signal for the first tap, the second and
the rest taps should be delayed by 1UI sequentially. D flip-flop is used in DFE to fulfill the delay operation.

As shown in Figure 4.15, the D Flip-Flop consists of a master stage and a slave stage, both of which have the same components but separately driven by the clock signal and its inverse. The single stage shown in the dashed box in Figure 4.15 is CMOS D-latch. This circuit contains two tri-state inverters [28], which can be treated as the combination of conventional inverters and switches.

![Diagram](image.png)

Figure 4.15: D flip-flop circuit

The basic idea of CMOS D-latch can be simplified in Figure 4.16. When the clock is low, the second tri-state inverter is at its high-impedance stage. After converted by the first tri-state inverter and a conventional inverter, the output of the first stage follows the input signal. When clock goes high, the input buffer becomes inactive, and the second tri-state inverter completes the two-inverter loop, which preserves its state until the next clock pulse [28].
CHAPTER 4. CONVENTIONAL DFE COMPOSITION

Figure 4.16: Simplified CMOS D-latch (Source [28])

After the introduction of a single stage, the whole circuit of D flip-flop will be concluded below. When clock is low, the input signal flows through the master stage which is transparent while the slave stage holds the previous value. At the clock rising edge where clock signal changes from logic low to high, the master stage starts to hold and the stored input value \( Q_m \) is passed through the slave stage. The input cannot affect the output because the master stage is disconnected from the D input [28]. Later at the falling edge of the clock, the two-inverter loop in the slave stage is turned on and the value \( Q_m \) is locked for another \( 0.5T \), where \( T \) is the period of clock signal. At the same time, the master stage starts to sample the input again. Therefore, this D flip-flop samples the input at the rising edge of clock signal. In this DFE work, since the frequency of clock is twice as high as the input signal D for D flip-flop, the output Q is the 1UI-delayed (0.5T-delayed) input, as shown in Figure 4.17.
Figure 4.17: Clocking scheme of D flip-flop
Chapter 5

Proposed Current-Integrating Summer

As introduced in Chapter 4, the half-rate DFE with first-tap speculation method consists of four paths. Two main parallel paths for half-rate operation, which are odd and even path, work at different clock phases. In each path (odd or even), another two paths are separated for adding or subtracting the first feedback tap coefficient, which are called strong-zero path and strong-one path. It shows that although first-tap speculation relaxes the first-tap feedback timing constraint, the implementation of this method is at the cost of extra area and power consumption. To apply the first-tap speculation into DFE, an additional summer, slicer and multiplexer are required.

However, the main part of summers in two speculative paths are actually redundant. Except the complementary feedback signals for the two first speculative taps, the input signals for the main differential pairs and other taps in two summers are exactly the same. Area inefficiency and extra power consumption will be more and more obvious with the increasing of unspeculative tap number. To overcome this problem, a new current-integrating summer with two stages is proposed to separate the first speculative tap from the main differential pair and other taps. The DFE architecture with new current-integrating summer is shown in Figure 5.1 where two speculative paths are available to be driven by a single summer instead of two. Besides, except the summer design, other blocks in the proposed DFE are the same as the conventional ones presented in Chapter 4.

The proposed current-integrating summer consists of two stages, which are conventional current-integrating stage and switched-capacitor stage. The switched-capacitor stage, emphasized in the dashed square in Figure 5.2 is utilized for the first speculative tap. The rest part, which is the current-integrating stage, is the same as the previous design. This stage is for the differential pair and other unspeculative taps (the second and third taps in this work). The details of these two stages, especially the operation and implementation of switched-capacitors are introduced in the following
CHAPTER 5. PROPOSED CURRENT-INTEGRATING SUMMER

5.1 Current-Integrating Stage

The first stage, current-integrating stage, is the same as the conventional one. With the active load controlled by clock signal, the operation of the first stage is divided into two phases, reset phase (CLK low) and evaluation phase (CLK high). In reset phase, the load capacitors at both of the output nodes ($P_{\text{stage1}}$ and $N_{\text{stage1}}$) are charged to supply voltage to make a preparation for the next phase. In the following evaluation phase, because of the differential input signal and effect of taps, the different summed current flowing through two differential paths discharges the output capacitors at different speed. Therefore, with the correct calibration of tap coefficients (tap current), the ISI-free differential output voltage is derived finally after integration.

What needs to be emphasized here is that the output capacitance of the first stage is the input capacitance of the second stage. To derive the differential output voltage with expected common mode voltage, not only the main current ($I_{\text{main}}$) in the first stage but also the size of the input transistors of next stage should be considered, because both of the current and load capacitance

Figure 5.1: 3-tap half-rate first-tap speculative DFE architecture with proposed current-integrating summer sections.

![Diagram of 3-tap half-rate first-tap speculative DFE architecture with proposed current-integrating summer sections.](image-url)
CHAPTER 5. PROPOSED CURRENT-INTEGRATING SUMMER

Figure 5.2: Proposed current-integrating summer with two separated stages

... can influence the discharging speed of the first stage.

As shown in the pull-up part of differential pair in Figure 5.2, two “dummy” switches are added to avoid the output glitches at clock transition, which has been explained clearly in Chapter 4.2. In addition, the size of PMOS transistors in differential pair should be larger enough than the input NMOS transistors which are always on. Due to the pull-down part, the output capacitors cannot be charged exactly to supply voltage in reset phase. Therefore, the consideration of transistor size is able to alleviate the additional influence to the result at the end of reset operation.

5.2 Switched-Capacitor Stage

The switched-capacitor stage for the first speculative tap is connected directly to the current-integrating stage. Two paths for speculation (strong-zero path and strong-one path) are split at the output of the first stage as shown in the dashed square in Figure 5.2. For a single switched-capacitor block, three switches controlled by clock signal “CLK1” and a sample capacitor are included. As shown in Figure 5.3, the simplified figure presented by switches instead of transistors clearly illustrates the operation of switched-capacitor stage.

Similar to the first stage, the operation of the second stage is also divided into reset phase and evaluation phase. In reset phase (CLK1 low), the output signal coming from the first stage is...
CHAPTER 5. PROPOSED CURRENT-INTEGRATING SUMMER

blocked by open switch S1. At the same time, the switches S2 and S3 are closed to connect the left side of capacitor $C$ to $V_{H1}$ and right side to ground, which set the voltage across the capacitor $C$ to $V_{H1}$. At the beginning of evaluation phase, switches S2 and S3 are opened to stabilize the charge stored on the capacitor $C$. Meanwhile, switch S1 is closed to send the signal $V_{in}$ coming from the first stage. Since the signal frequency is high enough, it can pass through the capacitor $C$ successfully, but has a specific voltage drop here. Therefore, the output voltage of the second stage is $V_{in} - V_{H1}$, which shows that the first tap is eliminated and ISI-free output is derived finally. For strong-zero path, where assuming the previous data bit is “0”, the switched-capacitor block with $V_{H1}$ voltage difference is added at the negative node. While for strong-one path, it is added at the positive node.

![Simplified switched-capacitor stage with clocking scheme](image)

Figure 5.3: Simplified switched-capacitor stage with clocking scheme

The operation of the whole proposed current-integrating summer will be concluded in the next section.
5.3 Operation of the proposed summer

The operation of the current-integrating stage and switched-capacitor stage consist of two phases, which are reset phase and evaluation phase. The clock signal for these two stages are nearly the same.

In reset phase, switch S1 between two stages are open to make an isolation for separated preparation. On one hand, the differential output voltage of the first stage are reset to supply voltage. On the other hand, the voltage at two sides of capacitor C in the second stage are stabilized at the same time. For the capacitor at the positive node of strong-one path and the one at the negative node of strong-zero path, the left side and right side of the capacitors are set to $V_{H1}$ and ground, respectively. However, as shown in Figure 5.2, for another two nodes in which voltage compensation is not required, both sides of capacitors C are charged to ground. (The reason for adding these two extra switched-capacitor blocks will be introduced in Chapter 5.4.1.) In the following evaluation phase, the differential output from the first stage with the second and third tap coefficients eliminated is passed through the switch S1 and drop a specific value, which is the first tap coefficient ($V_{H1}$) at the second stage. In conclusion, the effect of the second and third unspeculative taps are added in current-integrating stage. Strong-zero and strong-one paths are separated at the switched-capacitor stage where the first tap coefficient is added or subtracted. After the correct selection of the results from these two speculative paths by multiplexer, ISI in the input signal is fully removed.

However, due to the new architecture of the proposed summer and the slow discharging speed of comparator, the clock signal for the second stage has a small difference compared with the original one. The clock signal requirement will be presented in Chapter 5.4.3.

5.4 Design Considerations

For the switched-capacitor stage of the proposed summer, three essential design considerations for implementation are emphasized, which are charge sharing effect, the implementation of voltage source and clock signal requirement.

5.4.1 Charge Sharing Effect

The first effect to emphasized is charge sharing effect between the output capacitance $C_{load}$ and capacitor C. Due to this effect, the output voltage cannot be ideally $V_{in} - V_{H1}$, but can be
CHAPTER 5. PROPOSED CURRENT-INTEGRATING SUMMER

expressed as

\[ V_{od} = \frac{C(V_{in} - V_{H1})}{C + C_{load}} \]  

(5.1)

It shows that the expected output voltage is attenuated by a factor of \( C/(C + C_{load}) \). The effect will be significant if the capacitance of \( C \) can be compared with \( C_{load} \). Therefore, a proper value for \( C \) larger enough than \( C_{load} \) is required and \( C_{load} \), the input capacitance of comparator, needs to be minimized at the same time\(^{[23]}\). With \( C \gg C_{load} \), the attenuation factor can be eliminated by making \( C/(C + C_{load}) \approx 1 \). While if the input capacitance of next stage after summer (slicer) is difficult to be optimized, instead of adopting a large sample capacitor \( C \) in the switched-capacitor stage, a correct compensation can also be achieved by taking the attenuation factor into consideration. This is at the cost of smaller difference between the differential output voltage. Therefore, this is also a tradeoff between signal magnitude and area. If the smaller difference can be detected correctly by slicer after selecting a proper value of capacitance \( C \), the DFE can also has a good performance.

However, after considering the charge sharing effect, the voltage drop at capacitor \( C \) is still not exactly what is expected. Therefore, two extra switched-capacitor blocks are added at the positive node of strong-zero path and also at the negative node of strong-one path as shown in Figure\(^{[5.2]}\). Both sides of these two capacitors are set to ground in reset phase (the voltage across capacitors \( C \) is zero), which guarantees the exact difference of voltage drop \( V_{H1} \) at capacitors between positive and negative node.

5.4.2 Implementation of Voltage Source

The proposed summer requires not only the current sink for the second and third tap in current-integrating stage but also voltage source in the proposed design to implement the first tap voltage for switch-capacitors.

The current sink used in this work is the most basic one, where the reference current is applied using off-chip resistors and the value of tap currents can be altered by changing the value of resistors. Since the implementation of this basic current sink is simple, the details of which will not be introduced here. The current for the main differential pair (\( I_{main} \)) is around 300\( \mu \)A and for the second and third tap, the current (\( I_{H2} \) and \( I_{H3} \)) are 10\( \mu \)A and 5\( \mu \)A.

Apart from the current sink for the second and third tap in current-integrating stage, voltage source is also needed in the proposed design to implement the first tap voltage for switch-capacitors. What needs to be concerned is that the voltage value of the first tap coefficient \( V_{H1} \) is very small.
(around 20mV in this work), which is difficult to achieve in real circuit. Besides, the voltage source is impossible to be ideally stable, which makes it possible to introduce error to DFE through the first tap. It is desirable to add a common mode voltage $V_{CM}$ at both sides of the capacitor $C$ in each path, which guarantees that the voltage drop difference between these two differential nodes is still the first tap coefficient as expected.

The voltage source used in this work is shown in Figure 5.4, which is presented in [23]. Since the value of $V_{CM}$ is below half of the supply voltage, the voltage source is flipped over. In this circuit, the first tap coefficient is adjusted by off-chip resistors and a capacitor is added to filter out noise and kickback from the switches [23].

![Figure 5.4: The implementation of adjustable first-tap voltage](image)

5.4.3 Clock Signal Requirement

As mentioned before, the operation of the switched-capacitor stage and current-integrating stage are not exactly the same. The details will be described in the following part.

Since the output voltage of four paths in summer is $V_{CM}$ in reset phase, it will take some time for the output current from the first stage to charge the output capacitance $C_{load}$ from $V_{CM}$ once $S1$ is closed. Besides, the regenerative comparator at next stage starts to detect the summer output voltage difference at the rising edge of clock. It’s important to show enough difference between
differential outputs at that time. Therefore, the clock for the second stage CLK1 is $\Delta t_{\text{clk1}}$ earlier than the one (CLK) for other parts of DFE. For this work, where 2GHz clock signal is used, several dozens pico-seconds for $\Delta t_{\text{clk1}}$ is applied.

The value of $\Delta t_{\text{clk1}}$ is determined by the size of input capacitance of comparator, the value of main current, and common mode voltage $V_{\text{CM}}$ for the first tap. If $\Delta t_{\text{clk1}}$ is too small, errors can be introduced because the difference shown is not large enough at the rising edge of CLK. On the contrary, since CLK1 arrives earlier than CLK, it changes to low state earlier too. Although the comparator are testing the difference between outputs when CLK is high, it tests no difference after CLK1 changes to low state. The time for comparator to work properly is $t_{\text{clk}}/2 - \Delta t_{\text{clk1}}$, where $t_{\text{clk}}$ is the period of CLK signal. If $\Delta t_{\text{clk1}}$ is too large, the falling edge of CLK1 will arrive much earlier than CLK, $t_{\text{clk}}/2 - \Delta t_{\text{clk1}}$ may not be enough for comparator to pull-down successfully.

In addition, to guarantee the enough difference between summer differential output signal at the rising edge of regenerative comparator, the clock signal for comparator (CLK2) is also delayed for several dozens pico-seconds than CLK. The clocking scheme for CLK, CLK1 and CLK2 is shown in Figure 5.3.

When the proposed summer works at the frequency of 1GHz, the requirement of clock signal is not as complicated as the 2GHz case. Both of the summer and comparator work well without any problem using the original clock signal CLK since the pull-up time for switched-capacitors and the pull-down time for comparators are enough.

Assuming the previous three data bits are all “1” and the difference between clock signals can be neglected, the diagram for summer operation is specifically clarified in Figure 5.5 considering the effects mentioned above.
CHAPTER 5. PROPOSED CURRENT-INTEGRATING SUMMER

Figure 5.5: Diagram for summer operation
Chapter 6

Simulation Result

In this chapter, after characteristics of the channel employed in this work are described, the bit error rate result and eye diagram comparison will be presented. Besides, the output signal waveforms at essential nodes in DFE are shown to clearly illustrate the operation of the proposed DFE. The power consumption of each block and a comparison between the proposed DFE and conventional design are shown at the last part.

6.1 Channel Characteristics

Channel, through which signals are attenuated, should be clearly understood before evaluating the effect of DFE. In the following sections, the output signal of channel, channel loss at different frequency and post-cursor inter-symbol interference caused by channel are shown separately. The input signal before channel used in this work is 4Gb/s PRBS20 with the peak-to-peak amplitude of 700mV_{pp}.

6.1.1 Channel Output

There will be no need to use DFE if the eye diagram of channel output is wide and high enough. To test the effect of proposed DFE, a proper channel with enough channel loss is required.

The S-parameter file for channel model used here is “peters_01_0605_B1_thru.s4p”. This channel model, implemented by Intel, is an advancedTCA backplane “1 inch” short model with two connectors and line cards [29]. The stub depth for line card 1, backplane and line card 2 are 50, 10, 38 mil separately [30]. The line card material is Nelco 4000-6 and the length are both 5” [29].
CHAPTER 6. SIMULATION RESULT

Since the attenuation of input signal is not severe after transmitted through a single channel, three channels are connected in series in this work as shown in Figure 6.1. Because no information at DC is included in S-parameter file of this channel, to set a desired common mode of the channel output, a large AC coupling capacitor at the output of the B1 channel is added. The common mode of channel output is set to 900mV here. Besides, if the common mode of input signal for DFE is lower than 400mV, which is the threshold voltage of input NMOS transistors, the design of summer should be flipped over.

![Figure 6.1: Channel connection](image)

The channel input and output signal are shown in the following two figures, where the solid line is positive signal and the dot line is for negative (For each figure, lower waveform is input signal and upper one is output signal).

From Figure 6.2, we can easily find that the amplitude of sequence “101010” is much smaller than “11001100”. It indicates that as the frequency of the input signal increase, the channel loss becomes more severe, which is the same result shown later in Chapter 6.1.2.

The worst input case (worst case 1) is shown in Figure 6.3, where a long sequence consisting of twelve “0” is followed by a single “1”. The difference between two output nodes should be positive, but it is nearly zero or even negative in this case since this 2GHz “1” signal has the smallest amplitude which has been mentioned above and the post-cursor ISI from previous bits are accumulated at this “1” signal. This output data bit with such a small difference will definitely cause error at the output of receiver without equalization. Therefore, this is the most important case.
Figure 6.2: Channel output waveform (a)
to be concerned when testing the performance of DFE. In addition, compared with the worst case, the following three cases in Figure 6.3 which are “001”, “0001” and “00001” show that the output amplitude of these four single “1” bits only changed a little. Therefore, the ISI from the bit 4UI before or the bits from even farther is not so obvious, which will be clearly shown in Chapter 6.1.3. Three taps are enough for the ISI compensation of this channel.

For the DFE without adaptive algorithm, the correct choice of tap coefficients is the key of DFE performance. As mentioned above, the tap coefficients should be big enough to compensate the worst case error (worst case 1). However, the coefficients cannot be too big to overcompensate the correct input signal on the other hand. The twelve “0” signal in Figure 6.3 shows an increasing amplitude due to the accumulated ISI. Although the ISI in this case amplifies the input signal (which is good for receiver detection), DFE cannot recognize whether the ISI at current bit is a good factor or not. What DFE does is simply adding tap coefficient if previous bit is “0” or subtracting if previous bit is “1”. Therefore, another worst case (worst case 2) is shown in Figure 6.3 the fourth “0” bit in sequence “100001” will be a critical bit for 3-tap DFE because three tap coefficients should be eliminated from it and it also has the smallest amplitude compared with other case like the fourth
and fifth bit in sequence “1000001”. After compensation, the voltage at the negative node must be still bigger enough than the one at positive node for slicer to make a good decision.

In conclusion, after analyzing the output of channel, two worst cases are emphasized, which must be concentrated on when deciding the tap coefficients and testing the performance of DFE.

6.1.2 Channel Loss

The S21 plot for the channel used in this work is shown in Figure 6.4. At 2GHz of the operation frequency of DFE, the loss is 28dB.

![Figure 6.4: Channel loss](image)
CHAPTER 6. SIMULATION RESULT

6.1.3 Inter-symbol Interference

As introduced at the very beginning of this thesis, the attenuation at current data bit is the effect of accumulated post-cursor ISI produced by previous bits. To determine the tap number and tap coefficients of DFE, the magnitude of post-cursor ISI and the information of how many succeeding bits the current bit influences are needed. If the DFE coefficients can be modified automatically, only the time interval one bit will spread is important since this will affect the tap number involved in DFE. However, since there is no current DAC or adaptive algorithm introduced in this work, the amplitude of input signal is also important to determine the value of tap coefficients.

The post-cursor ISI of a differential 1V single pulse signal (shown in Figure 6.5 (a)) transmitted through the channel at 2GHz is shown in Figure 6.5 (b). As the ten vertical dot lines indicate, the pulse signal spreads nearly far to 9UI after channel and its “tail” influences the nine succeeding data bits, which indicate that to fully eliminate the ISI in current bit produced by previous bits, nine taps are required. However, area and power consumption will increase since more D flip-flops should be involved and more current will flow in summer if DFE is implemented with more taps. Therefore, due to the tradeoff between area, power consumption and accuracy of DFE, a DFE with three taps is determined. The 3-tap DFE can ideally compensate about 77% of the total post-cursor ISI.

Besides, from the time difference between the signal before channel and after channel in Figure 6.5 an additional information can be derived, which is the propagation delay of channel. The delay is $7.044\text{ns} - 0.150\text{ns} = 6.894\text{ns}$.

6.2 Eye Diagram

The comparison of the eye diagram before and after the proposed DFE is presented in Figure 6.6 (a). It is clear that eyes are nearly closed before the equalization. However, after properly calibrating the summer coefficients, the opened eye diagram after the proposed DFE is shown in Figure 6.6 (b).

6.3 Bit-Error Rate

BER, the number of bit errors divided by the total number of transferred bits during a studied time interval $[32]$, is the best visible result to evaluate the effect of DFE. In addition, to show
Figure 6.5: A single pulse signal (a) before channel (b) after channel
Figure 6.6: Eye diagram (a) before DFE (b) after DFE
the stability of DFE, clock phase is shifted and corresponding BER result is measured when clock signal with difference phase position is applied to DFE. The result is commonly shown in a bath-tub curve where x-axis is the phase position and y-axis is $\log_{10}(BER)$.

In order to test the BER result of DFE, a large amount of random data bits is needed. For example, in [14] published in ISSCC and [22] published in JSSC, the minimum value of measured $\log_{10}(BER)$ is “$-12$”, and in [11], BER $< 10^{-8}$ is derived. However, simulation with this large amount of data bits involved is impossible to be completed by Cadence in a reasonable time. Therefore, due to this limitation, the maximum value of involved data bits in this thesis is $10^6$.

To derive the BER result by comparing the output signal with input random bit stream, another two delayed (around 7.5ns, which is the propagation delay of channel plus the DFE delay) differential PRBS blocks whose amplitude is set to 1.8V are added in the circuit. This delayed differential input and DFE output signal are sent together into XOR gate, which is shown in Figure 6.7. Therefore, “0” in the XOR output indicates that the DFE output data bit is correct while the error is emphasized by “1”.

BER results when DFE is switched off or switched on are shown separately in the following sections.

### 6.3.1 BER result with DFE switched off

The BER results with DFE switched off is shown in Figure 6.8. Even when the clock transition is exactly at the middle of the input eye, the $\log_{10}(BER)$ is high, which is approximately “-2”. The slicer fails to detect the input data in the cases (emphasized in circles) shown in Figure 6.3.

### 6.3.2 BER result with DFE active

The BER results with DFE active is shown in Figure 6.9. With proper tap coefficients, the horizontal eye opening is about 40% at BER $< 10^{-6}$.

### 6.4 Output Signal Waveforms

To clearly explain the operation of the proposed DFE, the signal waveforms of essential nodes in each block are illustrated in Figure 6.10 and Figure 6.11. The signals at positive nodes are presented with solid lines and the signals in dashed lines come from negative nodes. The waveforms are shown in the order of signal transmission.
Figure 6.7: XOR gate for error detection
Figure 6.8: BER bathtub curve for 28dB channel at 4 Gb/s with DFE switched off
Figure 6.9: BER bathtub curve for 28dB channel at 4 Gb/s with DFE active
Figure 6.10: Signal waveforms of essential nodes in DFE (a)
Figure 6.11: Signal waveforms of essential nodes in DFE (b)
As the dashed lines in Figure 6.10 and Figure 6.11 show, the worst case which has been mentioned in Chapter 6.1.1 derives a good result at the output of DFE. For the single “0” signal after four “1”s, it shows nearly no difference at the channel output at the very beginning. With the help of DFE, the difference is first increased at the current-integrating stage of summer by subtracting the ISI from the two “1” bits 2-UI and 3-UI before, and then compensated further with \(+H_1\) or \(-H_1\) at the second switched-capacitor stage. The output of summer is afterward amplified and decided by slicer separately at the strong one path and strong zero path. Finally, the correct path, which is strong one path in this case, is selected by multiplexer. The comparison between output bar signal and delayed input is shown at the bottom of Figure 6.11, which shows that the potential error in the worst case is successfully recovered by DFE.

### 6.5 Power Consumption

The power consumption of the proposed DFE is 17.4mW with 1.8V supply voltage. The power consumption of each block is listed in Table 6.1, where the “Current Sources” includes all of the current sources used in this work and “Voltage Sources” represents two voltage sources used in the switched-capacitor stage in summer. In addition, a pie chart which clearly displays the ratio of power in each part is also presented in Figure 6.12.

<table>
<thead>
<tr>
<th></th>
<th>(I_{\text{ave}}) (mA)</th>
<th>Number</th>
<th>(I_{\text{tot}}) (mA)</th>
<th>Power (mW)</th>
<th>Percentage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/H</td>
<td>4.76 \times 10^{-4}</td>
<td>2</td>
<td>9.51 \times 10^{-4}</td>
<td>1.71 \times 10^{-3}</td>
<td>0.00986</td>
</tr>
<tr>
<td>Summer</td>
<td>1.35</td>
<td>2</td>
<td>2.70</td>
<td>4.86</td>
<td>28.0</td>
</tr>
<tr>
<td>Pre-amplification</td>
<td>0.922</td>
<td>4</td>
<td>3.69</td>
<td>6.64</td>
<td>38.2</td>
</tr>
<tr>
<td>Latch</td>
<td>0.346</td>
<td>4</td>
<td>1.38</td>
<td>2.49</td>
<td>14.3</td>
</tr>
<tr>
<td>multiplexer</td>
<td>0.0517</td>
<td>4</td>
<td>0.207</td>
<td>0.372</td>
<td>2.14</td>
</tr>
<tr>
<td>D Flip-Flop</td>
<td>0.373</td>
<td>4</td>
<td>1.49</td>
<td>2.69</td>
<td>15.5</td>
</tr>
<tr>
<td>Current Sources</td>
<td>0.173</td>
<td>1</td>
<td>0.173</td>
<td>0.312</td>
<td>1.80</td>
</tr>
<tr>
<td>Voltage Sources</td>
<td>5.17 \times 10^{-5}</td>
<td>1</td>
<td>5.17 \times 10^{-5}</td>
<td>9.31 \times 10^{-8}</td>
<td>0.000536</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
<td>9.65</td>
<td>17.4</td>
<td>100</td>
</tr>
</tbody>
</table>

Table 6.1: Power consumption of each block

Although there are plenty of DFE designs presented before, only few of them are implemented in CMOS 180nm technology node. Among these 180nm DFE works, none of them used exactly the same half-rate first-tap speculation method and most of them measured the power consumption with other blocks apart from DFE. Besides, many other factors also build a barrier for
Figure 6.12: Power consumption of each block in DFE
reasonable comparison. For example, different tap number, different operation frequency, different architectures . . . Three prior 180nm works are shown in Table 6.2 and the extra blocks included during power measurement are presented in “other” column.

<table>
<thead>
<tr>
<th>paper</th>
<th>supply</th>
<th>taps</th>
<th>f</th>
<th>clock</th>
<th>speculation</th>
<th>power</th>
<th>other</th>
</tr>
</thead>
<tbody>
<tr>
<td>[33]</td>
<td>1.8V</td>
<td>2</td>
<td>10Gb/s</td>
<td>half-rate</td>
<td>no</td>
<td>27mW</td>
<td>with LE</td>
</tr>
<tr>
<td>[34]</td>
<td>1.8V</td>
<td>2</td>
<td>5Gb/s</td>
<td>half-rate</td>
<td>no</td>
<td>60mW</td>
<td>with CDR and PFD</td>
</tr>
<tr>
<td>[35]</td>
<td>1.8V</td>
<td>2</td>
<td>6.25Gb/s</td>
<td>quarter-rate</td>
<td>no</td>
<td>18mW</td>
<td>with FFE</td>
</tr>
</tbody>
</table>

Table 6.2: Prior 180nm DFE works

As shown in the table above, it is really difficult to find a proper work to compare with the proposed DFE. Therefore, the power of a half-rate first-tap speculative DFE with conventional current-integrating summer is measured to make a comparison with the proposed design. For a fair comparison, the whole circuit for differential pair and tap transistors in conventional summer and proposed summer are designed in the same technology node. Besides, the main current \( I_{\text{main}} \) is also 300 \( \mu \)A and three tap current is 94\( \mu \)A, 15\( \mu \)A, 7\( \mu \)A, separately. The four summers and current sources in conventional DFE, which are the only different parts from the proposed one, consumes 6.51mW. As presented in Table 6.2, the total power consumption in proposed summer, current sources and voltage sources is 5.17mW, which shows 20.5\% power reduction compared with the conventional summer.

Moreover, the common mode of the proposed summer output is about 1V due to the reference voltage of the comparator. Therefore, the load capacitors of summer are charged to 1V, and they are discharged to about 100mV in every clock cycle. All these factors make the power efficiency of the proposed DFE quite low. It is possible to reduce the power consumption even further if the reference voltage of comparator is able to be decreased by being flipped over.
Chapter 7

Conclusion

As the requirement of high-speed transmission through channel increases, great difficulties are faced in detecting data at receiver side due to the limited bandwidth of channel. As a result, the input signal of receiver shows a small eye or even closed eye. This is mainly due to the post-cursor inter-symbol interference (ISI), which is a non-ideal “tail” after each data bit pulse and interferes with the preceding and succeeding bits. This unavoidable situation can easily lead to a large amount of errors, which is a disaster for data transmission. To overcome this difficulty, different methods for data equalization both in transmitter and receiver sides have been presented. Among these approaches, DFE surpasses other equalizers because of its advantage to compensate the post-cursor ISI without amplifying noise.

After careful review of the state-of-the-art DFE architectures such as half-rate architecture, first-tap speculation method and floating-tap method, a power and area efficient DFE is proposed in this thesis with a new current-integrating summer for the speculation method. The proposed 3-tap half-rate DFE with first-tap speculation is designed using standard CMOS 180nm technology with 1.8V supply voltage. Unlike the conventional first-tap speculative DFE that requires two summers at two parallel paths for speculation, area efficiency is improved in the proposed DFE design. By adding the switched-capacitor approach, a new current-integrating summer with first tap separated allows two speculative paths to be driven by a single summer.

The characteristics of channel are simulated and analyzed with two worst cases for DFE evaluation. From the simulation result in Cadence, the proposed DFE consumes 17.4mW with 1.8V supply voltage when equalizing 4Gb/s data passed over a channel with 28dB loss at 2GHz. It shows a significant improvement at the bit-error-rate result the horizontal 40% eye opening at BER less than $10^{-6}$ is achieved while the BER of data with DFE switched off is around $10^{-2}$ at the eye center.
CHAPTER 7. CONCLUSION

The proposed DFE with area efficient summer can be improved further in the future by modifying the regenerative comparator to decrease the input capacitance. The optimization of summer’s load capacitance can reduce the size of sample capacitor in switched-capacitors, which decreases the total area of DFE. Finally, this thesis will be a great reference if the LMS algorithm and current DAC blocks are implemented and embedded inside the proposed DFE for self-adaptation of tap coefficients. This will make it possible for the proposed DFE to be applied to different input signals or transmission line without selecting proper coefficients by uses.
Bibliography


BIBLIOGRAPHY


BIBLIOGRAPHY


[32] wikipedia, “Bit error rate,”

[33] M. Zhang and Q. Hu, “A 10 gb/s equalizer in 0.18um cmos technology for high-speed serdes,”

[34] M. Li, T. Kwasniewski, and S. Wang, “A 0.18-um cmos receiver with decision-feedback
Pacific Conference on, December 2006.

timing for high-speed backplane data communications,” in Proceedings of the 9th International
Database Engineering & Application Symposium, July 2005.
Appendix A

SPICE Netlist for poposed area effective DFE

// Library name: DFEsummer
// Cell name: channel2
// View name: schematic
subckt channel2 CH_out CH_outb CM_H CM_L IN INB

  NPORT2 (net09 0 OUT2 0 net023 0 OUT2B 0) nport interp=linear \ 
  thermalnoise=yes datafmt=touchstone \ 
  file="/home/centos/DFEsummer/channel_model/Ch_Sparam/peters_01_0605_B1_thru.s4p"

  NPORT0 (net019 0 OUT1 0 net010 0 OUT1B 0) nport interp=linear \ 
  thermalnoise=yes datafmt=touchstone \ 
  file="/home/centos/DFEsummer/channel_model/Ch_Sparam/peters_01_0605_B1_thru.s4p"

  NPORT1 (OUT2 0 net04 CM_L OUT2B 0 net026 CM_H) nport interp=linear \ 
  thermalnoise=yes datafmt=touchstone \ 
  file="/home/centos/DFEsummer/channel_model/Ch_Sparam/peters_01_0605_B1_thru.s4p"

C1 (net026 CH_outb) capacitor c=1m
C0 (net04 CH_out) capacitor c=1m
R11 (net023 OUT1B) resistor r=50
APPENDIX A. SPICE NETLIST FOR PROPOSED AREA EFFECTIVE DFE

R10 (OUT1 net09) resistor r=50
R3 (net010 INB) resistor r=50
R2 (IN net019) resistor r=50
R1 (CH_out CM_L) resistor r=50
R0 (CM_H CH_outb) resistor r=50
ends channel2

// End of subcircuit definition.

// Library name: DFE
// Cell name: SH
// View name: schematic

subckt SH CLK CLKB GND VDD out outb x xb
  M42 (outb CLK outb GND) nch tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \ ps=10.96u nrd=96m nrs=96m m=(1)*(1)
  M39 (out CLK out GND) nch tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \ ps=10.96u nrd=96m nrs=96m m=(1)*(1)
  M38 (x CLKB out GND) nch tn w=(10u) l=360n ad=4.8p as=4.8p pd=20.96u \ ps=20.96u nrd=48m nrs=48m m=(1)*(1)
  M37 (xb CLKB outb GND) nch tn w=(10u) l=360n ad=4.8p as=4.8p pd=20.96u \ ps=20.96u nrd=48m nrs=48m m=(1)*(1)
  M41 (xb CLK xb GND) nch tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \ ps=10.96u nrd=96m nrs=96m m=(1)*(1)
  M40 (x CLK x GND) nch tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \ ps=10.96u nrd=96m nrs=96m m=(1)*(1)
  M22 (out CLK out VDD) pch tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \ ps=10.96u nrd=96m nrs=96m m=(1)*(1)
  M25 (outb CLKB outb VDD) pch tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \ ps=10.96u nrd=96m nrs=96m m=(1)*(1)
  M21 (x CLK out VDD) pch tn w=(10u) l=360n ad=4.8p as=4.8p pd=20.96u \ ps=20.96u nrd=48m nrs=48m m=(1)*(1)
  M18 (xb CLK outb VDD) pch tn w=(10u) l=360n ad=4.8p as=4.8p pd=20.96u \ ps=20.96u nrd=48m nrs=48m m=(1)*(1)
  M24 (xb CLKB xb VDD) pch tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \
APPENDIX A. SPICE NETLIST FOR PROPOSED AREA EFFECTIVE DFE

\[ \text{ps}=10.96\mu \text{ nrd}=96\text{m nrs}=96\text{m m}=(1)\times(1) \]

\[ \text{M23 (x CLKB x VDD) pch_{tn} w}=(5\mu) \text{ l}=360\text{n ad}=2.4p \text{ as}=2.4p \text{ pd}=10.96\mu \]

\[ \text{ps}=10.96\mu \text{ nrd}=96\text{m nrs}=96\text{m m}=(1)\times(1) \]

ends SH

// End of subcircuit definition.

// Library name: DFE_FR
// Cell name: invX16
// View name: schematic

subckt invX16 gnd in out vdd

\[ \text{PM0 (out in vdd vdd) pch_{tn} w}=(1.76\mu) \text{ l}=180\text{n ad}=624.8f \text{ as}=884.4f \]
\[ \text{pd}=2.47u \text{ ps}=3.645u \text{ nrd}=201.705m \text{ nrs}=285.511m \text{ m}=(1)\times(4) \]

\[ \text{NM0 (out in gnd gnd) nch_{tn} w}=(880n) \text{ l}=180\text{n ad}=312.4f \text{ as}=442.2f \]
\[ \text{pd}=1.59u \text{ ps}=2.325u \text{ nrd}=403.409m \text{ nrs}=571.023m \text{ m}=(1)\times(4) \]

ends invX16

// End of subcircuit definition.

// Library name: DFE_FR
// Cell name: invX4
// View name: schematic

subckt invX4 gnd in out vdd

\[ \text{PM0 (out in vdd vdd) pch_{tn} w}=(1.7u) \text{ l}=180\text{n ad}=816f \text{ as}=816f \]
\[ \text{pd}=4.36u \text{ ps}=4.36u \text{ nrd}=282.353m \text{ nrs}=282.353m \text{ m}=(1)\times(1) \]

\[ \text{NM0 (out in gnd gnd) nch_{tn} w}=(880n) \text{ l}=180\text{n ad}=422.4f \text{ as}=422.4f \]
\[ \text{pd}=2.72u \text{ ps}=2.72u \text{ nrd}=545.455m \text{ nrs}=545.455m \text{ m}=(1)\times(1) \]

ends invX4

// End of subcircuit definition.

// Library name: DFE
// Cell name: MUX2_1
// View name: schematic

subckt MUX2_1 A B GND Q SEL IN VDD

\[ \text{NM3 (SEL_B SEL_IN GND GND) nch_{tn} w}=(1u) \text{ l}=180\text{n ad}=650f \text{ as}=650f \]
APPENDIX A. SPICE NETLIST FOR POPOSED AREA EFFECTIVE DFE

pd=3.3u ps=3.3u nrd=650m nrs=650m m=(1)*(1)
NM2 (A SEL B Q GND) nch_tn w=(1u) l=180n ad=453.333f as=453.333f \n  pd=2.24u ps=2.24u nrd=453.333m nrs=453.333m m=(1)*(3)
NM1 (B SEL Q GND) nch_tn w=(1u) l=180n ad=453.333f as=453.333f \n  pd=2.24u ps=2.24u nrd=453.333m nrs=453.333m m=(1)*(3)
NM0 (SEL SEL B GND GND) nch_tn w=(1u) l=180n ad=453.333f as=453.333f \n  pd=2.24u ps=2.24u nrd=453.333m nrs=453.333m m=(1)*(3)
PM3 (SEL B SEL IN VDD VDD) pch_tn w=(1.85u) l=180n ad=1.2025p \n  as=1.2025p pd=5u ps=5u nrd=351.351m nrs=351.351m m=(1)*(1)
PM2 (A SEL Q VDD) pch_tn w=(1.85u) l=180n ad=838.667f as=838.667f \n  pd=3.37333u ps=3.37333u nrd=245.045m nrs=245.045m m=(1)*(3)
PM1 (B SEL B Q VDD) pch_tn w=(1.85u) l=180n ad=838.667f as=838.667f \n  pd=3.37333u ps=3.37333u nrd=245.045m nrs=245.045m m=(1)*(3)
PM0 (SEL SEL B VDD VDD) pch_tn w=(1.85u) l=180n ad=838.667f \n  as=838.667f pd=3.37333u ps=3.37333u nrd=245.045m nrs=245.045m m=(1)*(3)
ends MUX2_1
// End of subcircuit definition.

// Library name: DFEsummer
// Cell name: current_sink
// View name: schematic
subckt current_sink GND Imain1 Imain2 Imain3 Imain4 Iref
  NM9 (Imain2 Iref GND GND) nch_tn w=(20u) l=360n ad=9.6p as=9.6p \n    pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*(1)
  NM7 (Imain1 Iref GND GND) nch_tn w=(20u) l=360n ad=9.6p as=9.6p \n    pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*(1)
  NM14 (Imain3 Iref GND GND) nch_tn w=(20u) l=360n ad=9.6p as=9.6p \n    pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*(1)
  NM15 (Imain4 Iref GND GND) nch_tn w=(20u) l=360n ad=9.6p as=9.6p \n    pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*(1)
  NM2 (Iref Iref GND GND) nch_tn w=(1u) l=360n ad=480f as=480f pd=2.96u \n    ps=2.96u nrd=480m nrs=480m m=(1)*(1)
ends current_sink

68
APPENDIX A. SPICE NETLIST FOR POPOSED AREA EFFECTIVE DFE

ends current_sink
// End of subcircuit definition.

// Library name: DFE_FR
// Cell name: Comparator_rev1
// View name: schematic
subckt Comparator_rev1 CLK CLKB GND RB SB VDD Vinn Vinp
  NM5 (net036 Vinn net014 GND) nch_tn w=(400n) l=180n ad=134.08f \ 
as=134.08f pd=1.096u ps=1.096u nrd=838m nrs=838m m=(3)*(15)
  NM4 (net23 Vinp net014 GND) nch_tn w=(400n) l=180n ad=134.08f \ 
as=134.08f pd=1.096u ps=1.096u nrd=838m nrs=838m m=(3)*(15)
  NM3 (RB SB net036 GND) nch_tn w=(440n) l=180n ad=118.8f as=137.28f \ 
  pd=980n ps=1.152u nrd=613.636m nrs=709.091m m=(2)*(10)
  NM2 (SB RB net23 GND) nch_tn w=(440n) l=180n ad=118.8f as=137.28f \ 
  pd=980n ps=1.152u nrd=613.636m nrs=709.091m m=(2)*(10)
  NM6 (net014 CLK GND GND) nch_tn w=(400n) l=180n ad=128.2f as=137.02f \ 
  pd=1.04u ps=1.124u nrd=801.25m nrs=856.375m m=(3)*(20)
  PM4 (RB CLK VDD VDD) pch_tn w=(220n) l=180n ad=110.2f as=119.02f \ 
  pd=1.04u ps=1.124u nrd=2.27686 nrs=2.45909 m=(4)*(20)
  PM3 (RB SB VDD VDD) pch_tn w=(440n) l=180n ad=118.8f as=128.04f \ 
  pd=980n ps=1.066u nrd=613.636m nrs=661.364m m=(2)*(20)
  PM2 (SB RB VDD VDD) pch_tn w=(440n) l=180n ad=118.8f as=128.04f \ 
  pd=980n ps=1.066u nrd=613.636m nrs=661.364m m=(2)*(20)
  PM1 (SB CLK VDD VDD) pch_tn w=(220n) l=180n ad=110.2f as=119.02f \ 
  pd=1.04u ps=1.124u nrd=2.27686 nrs=2.45909 m=(4)*(20)
ends Comparator_rev1
// End of subcircuit definition.

// Library name: MPDK_HL18G
// Cell name: rdhpo_ns
// View name: schematic
subckt rdhpo_ns_pcell_2 B MINUS PLUS
parameters segW=2u segL=10u nMcMode=1 mult_top=(1)
APPENDIX A. SPICE NETLIST FOR PROPOSED AREA EFFECTIVE DFE

R8 (PLUS MINUS B) rdhpo ns w=segW l=segL mcmode=nMcMode mult=mult_top
R7 (PLUS MINUS B) rdhpo ns w=segW l=segL mcmode=nMcMode mult=mult_top
R6 (PLUS MINUS B) rdhpo ns w=segW l=segL mcmode=nMcMode mult=mult_top
R5 (PLUS MINUS B) rdhpo ns w=segW l=segL mcmode=nMcMode mult=mult_top
R4 (PLUS MINUS B) rdhpo ns w=segW l=segL mcmode=nMcMode mult=mult_top
R3 (PLUS MINUS B) rdhpo ns w=segW l=segL mcmode=nMcMode mult=mult_top
R2 (PLUS MINUS B) rdhpo ns w=segW l=segL mcmode=nMcMode mult=mult_top
R1 (PLUS MINUS B) rdhpo ns w=segW l=segL mcmode=nMcMode mult=mult_top
R0 (PLUS MINUS B) rdhpo ns w=segW l=segL mcmode=nMcMode mult=mult_top

ends rdhpo ns pcell

// End of subcircuit definition.

// Library name: DFEsummer
// Cell name: current_source2
// View name: schematic

subckt current_source2 Iin1 Iin2 Imain1 Imain2 Imain3 Imain4 Iref VDD

PM3 (Imain1 Iref VDD VDD) pch_tn w=(20u) l=360n ad=9.6p as=9.6p \ 
  pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*(1)
PM4 (Imain2 Iref VDD VDD) pch_tn w=(20u) l=360n ad=9.6p as=9.6p \ 
  pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*(1)
PM6 (Imain3 Iref VDD VDD) pch_tn w=(20u) l=360n ad=9.6p as=9.6p \ 
  pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*(1)
PM1 (Iref Iref VDD VDD) pch_tn w=(1u) l=360n ad=480f as=480f pd=2.96u \ 
  ps=2.96u nrd=480m nrs=480m m=(1)*(1)
PM7 (Imain4 Iref VDD VDD) pch_tn w=(20u) l=360n ad=9.6p as=9.6p \ 
  pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*(1)
PM8 (Iin1 Iref VDD VDD) pch_tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \ 
  ps=10.96u nrd=96m nrs=96m m=(1)*(1)
PM9 (Iin2 Iref VDD VDD) pch_tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \ 
  ps=10.96u nrd=96m nrs=96m m=(1)*(1)

ends current_source2

// End of subcircuit definition.
APPENDIX A. SPICE NETLIST FOR PROPOSED AREA EFFECTIVE DFE

// Library name: DFEsummer
// Cell name: current_sink2
// View name: schematic
subckt current_sink2 GND Ih2_even Ih2_odd Ih3_even Ih3_odd Iref
  NM9 (Ih3_even Iref GND GND) nch tn w=(500n) l=360n ad=240f as=240f \ 
   pd=1.96u ps=1.96u nrd=960m nrs=960m m=(1)*(1) \ 
  NM7 (Ih2_even Iref GND GND) nch tn w=(1.8u) l=360n ad=864f as=864f \ 
   pd=4.56u ps=4.56u nrd=266.667m nrs=266.667m m=(1)*(1) \ 
  NM14 (Ih2_odd Iref GND GND) nch tn w=(1.8u) l=360n ad=864f as=864f \ 
   pd=4.56u ps=4.56u nrd=266.667m nrs=266.667m m=(1)*(1) \ 
  NM15 (Ih3_odd Iref GND GND) nch tn w=(500n) l=360n ad=240f as=240f \ 
   pd=1.96u ps=1.96u nrd=960m nrs=960m m=(1)*(1) \ 
  NM2 (Iref Iref GND GND) nch tn w=(5u) l=360n ad=2.4p as=2.4p pd=10.96u \ 
   ps=10.96u nrd=96m nrs=96m m=(1)*(1)
ends current_sink2
// End of subcircuit definition.

// Library name: DFEsummer
// Cell name: voltage_source2
// View name: schematic
subckt voltage_source2 GND Iin VDD Vout
  C0 (Vout GND) cmim1p1 w=15u l=15u area=225p peri=60u entrymode=1 \ 
   mcmode=1 m=1 mult=1 \ 
  PM1 (Iin Iin VDD VDD) pch tn w=(2u) l=360n ad=960f as=960f pd=4.96u \ 
   ps=4.96u nrd=240m nrs=240m m=(1)*(1) \ 
  PM0 (Vout Iin VDD VDD) pch tn w=(2u) l=360n ad=960f as=960f pd=4.96u \ 
   ps=4.96u nrd=240m nrs=240m m=(1)*(1)
ends voltage_source2
// End of subcircuit definition.

// Library name: DFEsummer
// Cell name: switchedcapacitor2
// View name: schematic
APPENDIX A. SPICE NETLIST FOR POPOSED AREA EFFECTIVE DFE

subckt _sub1 CLK CLK1 CLKB CLKB1 GND H2N H2P H3N H3P Ih2 Ih3 Imain1 Imain2 \ 
  Outn_s0 Outn_s1 Outp_s0 Outp_s1 VDD Vh1 Vh1_c VinN VinP
NM86 (Outp_s1 CLKB1 GND GND) nch tn w=8u l=360n ad=3.84p as=3.84p \ 
  pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)
NM89 (leftn2 CLKB1 Vh1_c GND) nch tn w=8u l=360n ad=3.84p as=3.84p \ 
  pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)
NM90 (Outn_s0 CLKB1 GND GND) nch tn w=8u l=360n ad=3.84p as=3.84p \ 
  pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)
NM87 (leftp2 CLKB1 Vh1_c GND) nch tn w=8u l=360n ad=3.84p as=3.84p \ 
  pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)
NM88 (Outp_s0 CLKB1 GND GND) nch tn w=8u l=360n ad=3.84p as=3.84p \ 
  pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)
NM59 (leftp1 CLKB1 Vh1_c GND) nch tn w=8u l=360n ad=3.84p as=3.84p \ 
  pd=16.96u ps=16.96u nrd=60m nrs=60m m=(1)*(1)
M44 (net06 H3N Ih3 GND) nch tn w=(1u) l=360n ad=480f as=480f pd=2.96u \ 
  ps=2.96u nrd=480m nrs=480m m=(1)*(1)
M43 (net049 H3P Ih3 GND) nch tn w=(1u) l=360n ad=480f as=480f pd=2.96u \ 
  ps=2.96u nrd=480m nrs=480m m=(1)*(1)
NM88 (Outp_s0 CLKB1 GND GND) nch tn w=(8u) l=360n ad=3.84p as=3.84p \ 
  pd=16.96u ps=16.96u nrd=60m nrs=60m nrd=60m nrs=60m m=(1)*(1)
M8 (net06 H2N Ih2 GND) nch tn w=(1u) l=360n ad=480f as=480f pd=2.96u \ 
  ps=2.96u nrd=480m nrs=480m m=(1)*(1)
M4 (net049 H2P Ih2 GND) nch tn w=(1u) l=360n ad=480f as=480f pd=2.96u \ 
  ps=2.96u nrd=480m nrs=480m m=(1)*(1)
M14 (net049 VinN Imain2 GND) nch tn w=(10u) l=360n ad=4.8p as=4.8p \ 
  pd=20.96u ps=20.96u nrd=48m nrs=48m m=(1)*(1)
M0 (net06 VinP Imain1 GND) nch tn w=(10u) l=360n ad=4.8p as=4.8p \ 
  pd=20.96u ps=20.96u nrd=48m nrs=48m m=(1)*(1)
R4 (Imain1 Imain2) resistor r=10
C13 (leftn2 Outn_s0) cmim1p1 w=14.315u l=18.96u area=271.412p \ 
  peri=66.55u entrymode=1 mcmode=1 m=1 mult=1
APPENDIX A. SPICE NETLIST FOR PROPOSED AREA EFFECTIVE DFE

C12 (leftp2 Outp_s0) cmim1p1 w=14.315u l=18.96u area=271.412p \ peri=66.55u entrymode=1 mcmode=1 m=1 mult=1
C9 (leftp1 Outp_s1) cmim1p1 w=14.315u l=18.96u area=271.412p \ peri=66.55u entrymode=1 mcmode=1 m=1 mult=1
C11 (leftn1 Outn_s1) cmim1p1 w=14.315u l=18.96u area=271.412p \ peri=66.55u entrymode=1 mcmode=1 m=1 mult=1
PM57 (net049 CLK net06 VDD) pch_tn w=(20u) l=360n ad=9.6p as=9.6p \ pd=40.96u ps=40.96u nrd=24m nrs=24m m=(1)*(1)
M45 (leftn1 CLKB1 net06 VDD) pch_tn w=(1u) l=360n ad=270f as=322.5f \ pd=1.54u ps=1.895u nrd=270m nrs=322.5m m=(1)*(8)
M36 (leftp1 CLKB1 net049 VDD) pch_tn w=(1u) l=360n ad=270f as=322.5f \ pd=1.54u ps=1.895u nrd=270m nrs=322.5m m=(1)*(8)
PM79 (net056 net058 net059 net057) pch_tn w=(35u) l=360n ad=16.8p \ as=16.8p pd=70.96u ps=70.96u nrd=13.7143m nrs=13.7143m m=(1)*(1)
PM78 (net060 net062 net063 net061) pch_tn w=(35u) l=360n ad=16.8p \ as=16.8p pd=70.96u ps=70.96u nrd=13.7143m nrs=13.7143m m=(1)*(1)
PM54 (leftn2 CLKB1 net06 VDD) pch_tn w=(1u) l=360n ad=270f as=322.5f \ pd=1.54u ps=1.895u nrd=270m nrs=322.5m m=(1)*(8)
PM53 (leftp2 CLKB1 net049 VDD) pch_tn w=(1u) l=360n ad=270f as=322.5f \ pd=1.54u ps=1.895u nrd=270m nrs=322.5m m=(1)*(8)
M1 (net06 CLK VDD VDD) pch_tn w=(50u) l=360n ad=24p as=24p pd=100.96u \ ps=100.96u nrd=9.6m nrs=9.6m m=(1)*(1)
M3 (net049 CLK VDD VDD) pch_tn w=(50u) l=360n ad=24p as=24p pd=100.96u \ ps=100.96u nrd=9.6m nrs=9.6m m=(1)*(1)

ends _sub1

// End of subcircuit definition.

// Library name: DFE
// Cell name: modified_SR_vthn_p_v1_2
// View name: schematic
subckt modified_SR_vthn_p_v1_2 GND Q QB RB SB VDD

NM33 (QB net049 net032 GND) nch_tn w=(400n) l=180n ad=163.9f \ as=194.875f pd=1.21u ps=1.4625u nrd=1.02437 nrs=1.21797 m=(3)*(8)

73
APPENDIX A. SPICE NETLIST FOR POPOSED AREA EFFECTIVE DFE

NM24 (QB Q net032 GND) nch tn w=(400n) l=180n ad=205.2f as=205.2f \ 
   pd=1.54667u ps=1.54667u nrd=1.2825 nrs=1.2825 m=(3)*(3)
NM23 (net032 RB GND GND) nch tn w=(400n) l=180n ad=188.68f as=188.68f \ 
   pd=1.412u ps=1.412u nrd=1.17925 nrs=1.17925 m=(3)*(5)
NM28 (net034 SB GND GND) nch tn w=(400n) l=180n ad=188.68f as=188.68f \ 
   pd=1.412u ps=1.412u nrd=1.17925 nrs=1.17925 m=(3)*(5)
NM30 (Q QB net034 GND) nch tn w=(400n) l=180n ad=205.2f as=205.2f \ 
   pd=1.54667u ps=1.54667u nrd=1.2825 nrs=1.2825 m=(3)*(3)
NM32 (Q net024 net034 GND) nch tn w=(400n) l=180n ad=163.9f \ 
   as=194.875f pd=1.21u ps=1.4625u nrd=1.02437 nrs=1.21797 m=(3)*(8)
NM26 (net049 SB GND GND) nch tn w=(265n) l=180n ad=191.7f as=191.7f \ 
   pd=1.54667u ps=1.54667u nrd=2.7298 nrs=2.7298 m=(3)*(3)
NM27 (net024 RB GND GND) nch tn w=(400n) l=180n ad=287.8f as=163.9f \ 
   pd=2.22u ps=1.21u nrd=1.79875 nrs=1.02437 m=(3)*(2)
PM26 (QB RB net031 VDD) pch tn w=(740n) l=180n ad=373.7f as=456.025f \ 
   pd=1.75u ps=2.1575u nrd=682.432m nrs=832.77m m=(3)*(8)
PM25 (QB Q net031 VDD) pch tn w=(740n) l=180n ad=483.467f as=483.467f \ 
   pd=2.29333u ps=2.29333u nrd=882.883m nrs=882.883m m=(3)*(3)
PM24 (net031 net049 VDD VDD) pch tn w=(740n) l=180n ad=306.36f \ 
   as=306.36f pd=1.716u ps=1.716u nrd=559.459m nrs=559.459m \ 
   m=(31)*(5)
PM29 (Q SB net033 VDD) pch tn w=(740n) l=180n ad=373.7f as=456.025f \ 
   pd=1.75u ps=2.1575u nrd=682.432m nrs=832.77m m=(3)*(8)
PM31 (net033 net024 VDD VDD) pch tn w=(740n) l=180n ad=306.36f \ 
   as=306.36f pd=1.716u ps=1.716u nrd=559.459m nrs=559.459m m=(3)*(5)
PM30 (Q QB net033 VDD) pch tn w=(740n) l=180n ad=483.467f as=483.467f \ 
   pd=2.29333u ps=2.29333u nrd=882.883m nrs=882.883m m=(3)*(3)
PM28 (net024 RB VDD VDD) pch tn w=(740n) l=180n ad=262.7f as=481f \ 
   pd=1.45u ps=2.78u nrd=479.73m nrs=878.378m m=(3)*(2)
PM27 (net049 SB VDD VDD) pch tn w=(740n) l=180n ad=262.7f as=481f \ 
   pd=1.45u ps=2.78u nrd=479.73m nrs=878.378m m=(3)*(2)

ends modified_SR_vthn_p_v1.2

// End of subcircuit definition.

74
APPENDIX A. SPICE NETLIST FOR POPOSED AREA EFFECTIVE DFE

// Library name: DFE
// Cell name: TB_DFE_3taps_2GHz
// View name: schematic
I167 (CH_out CH_outb net0136 net0131 net0156 net056) channel2
I51 (CLK CLKB 0 net020 SH_odd_s1_p SH_odd_s1_n CH_out CH_outb) SH
I0 (CLKB CLK 0 net022 SH_even_s1_p SH_even_s1_n CH_out CH_outb) SH
V20 (net0192 0) vsource dc=1.8 type=dc
V19 (net0194 0) vsource dc=1.8 type=dc
V14 (net0136 0) vsource dc=1 type=dc
V13 (net0132 0) vsource dc=1.8 type=dc
V7 (net043 0) vsource dc=1.8 type=dc
V8 (net010 0) vsource dc=1.8 type=dc
V9 (net06 0) vsource dc=1.8 type=dc
V10 (net088 0) vsource dc=1.8 type=dc
V18 (net0131 0) vsource dc=800m type=dc
V4 (net05 0) vsource dc=1.8 type=dc
V1 (net022 0) vsource dc=1.8 type=dc
V3 (net020 0) vsource dc=1.8 type=dc
V2 (vdd! 0) vsource dc=1.8 type=dc
V11 (CLKB2_IN 0) vsource dc=0 type=pulse val0=0 val1=1.8 period=1/f \ 
  delay=d_clk+d_shift+30p rise=50p fall=50p width=1/(2*f)-50p
V31 (CLKB_IN 0) vsource dc=0 type=pulse val0=0 val1=1.8 period=1/f \ 
  delay=d_clk+d_shift rise=50p fall=50p width=1/(2*f)-50p
V16 (CLK_D_IN 0) vsource dc=0 type=pulse val0=1.8 val1=0 period=1/f \ 
  delay=d_clk+d_shift-100p rise=50p fall=50p width=1/(2*f)-50p
V6 (CLK1_IN 0) vsource dc=0 type=pulse val0=1.8 val1=0 period=1/f \ 
  delay=d_clk+d_shift-80p rise=50p fall=50p width=1/(2*f)+50p
V5 (CLK_IN 0) vsource dc=0 type=pulse val0=1.8 val1=0 period=1/f \ 
  delay=d_clk+d_shift rise=50p fall=50p width=1/(2*f)-50p
V12 (CLK2_IN 0) vsource dc=0 type=pulse val0=1.8 val1=0 period=1/f \ 
  delay=d_clk+d_shift+30p rise=50p fall=50p width=1/(2*f)-50p
V46 (CLKB1_IN 0) vsource dc=0 type=pulse val0=0 val1=1.8 period=1/f \ 
  delay=d_clk+d_shift+20p rise=50p fall=50p width=1/(2*f)-150p
APPENDIX A. SPICE NETLIST FOR POPOSED AREA EFFECTIVE DFE

I118 (0 net058 net039 net05) invX16
I122 (0 net057 out_even_s1 net05) invX16
I219 (0 net059 out_even_s0 net043) invX16
I220 (0 net060 net032 net043) invX16
I241 (0 net076 out_odd_s1 net010) invX16
I240 (0 net072 net034 net010) invX16
I244 (0 net061 net044 net06) invX16
I243 (0 net070 out_odd_s0 net06) invX16
PM19 (Error IN net0147 net0192) pch_tn w=(4u) l=180n ad=1.92p as=1.92p
    pd=8.96u ps=8.96u nrd=120m nrn=120m m=(1)*(1)
PM18 (net0147 Ser_Datab net0192 net0192) pch_tn w=(4u) l=180n ad=1.92p
    as=1.92p pd=8.96u ps=8.96u nrd=120m nrn=120m m=(1)*(1)
PM17 (Error INB net0198 net0192) pch_tn w=(4u) l=180n ad=1.92p
    as=1.92p pd=8.96u ps=8.96u nrd=120m nrn=120m m=(1)*(1)
PM16 (net0198 Ser_Data net0192 net0192) pch_tn w=(4u) l=180n ad=1.92p
    as=1.92p pd=8.96u ps=8.96u nrd=120m nrn=120m m=(1)*(1)
I117 (0 net030 net058 net05) invX4
I121 (0 net031 net057 net05) invX4
I225 (0 net063 net059 net043) invX4
I226 (0 net033 net060 net043) invX4
I235 (0 net074 net076 net010) invX4
I234 (0 net075 net072 net010) invX4
I250 (0 net068 net061 net06) invX4
I249 (0 net035 net070 net06) invX4
I364 (H1_evenb H1_oddb 0 Ser_Datab CLK_D net0194) MUX2_1
I203 (H1_even H1_odd 0 Ser_Data CLK_D net088) MUX2_1
I85 (net039 net032 0 H1_evenb H1_oddb vdd!) MUX2_1
I204 (out_odd_s1 out_odd_s0 0 H1_odd H1_evenb vdd!) MUX2_1
I205 (net034 net044 0 H1_oddb H1_evenb vdd!) MUX2_1
I81 (out_even_s1 out_even_s0 0 H1_even H1_oddb vdd!) MUX2_1
I321 (0 Imain4 Imain3 Imain2 Imain1 net0166) current_sink
I349 (CLK2 CLKB2 0 SA_odd_s1_n SA_odd_s1_p vdd! CIS_odd_s1_n CIS_odd_s1_p)
    Comparator_rev1
APPENDIX A. SPICE NETLIST FOR PROPOSED AREA EFFECTIVE DFE

I350 (CLK2 CLKB2 0 SA_odd_s0_n SA_odd_s0_p vdd! CIS_odd_s0_n CIS_odd_s0_p) \ Comparator_rev1
I348 (CLKB2 CLK2 0 SA_even_s0_n SA_even_s0_p vdd! CIS_even_s0_n \ CIS_even_s0_p) Comparator_rev1
I347 (CLKB2 CLK2 0 SA_even_s1_n SA_even_s1_p vdd! CIS_even_s1_n \ CIS_even_s1_p) Comparator_rev1
NM19 (net0200 INB 0 0) nch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u \ 
  ps=4.96u nrd=240m nrs=240m m=(1)*(1)
NM18 (Error_Ser_Data net0200 0) nch_tn w=(2u) l=180n ad=960f as=960f \ 
  pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1)
NM17 (net0199 IN 0 0) nch_tn w=(2u) l=180n ad=960f as=960f pd=4.96u \ 
  ps=4.96u nrd=240m nrs=240m m=(1)*(1)
NM16 (Error_Ser_Data net0199 0) nch_tn w=(2u) l=180n ad=960f as=960f \ 
  pd=4.96u ps=4.96u nrd=240m nrs=240m m=(1)*(1)
R4 (0 vdd! net0166) rdhopos_pcell_2 m=1 segW=2u segL=860.955u nMcMode=1 \ 
  mult_top=(1)
I289 (lin1 lin2 net0165 net0157 net0154 net0153 vdd!) \ current_source2
I292 (0 Ih2_even Ih2_odd Ih3_even Ih3_odd net0134) current_sink2
I324 (0 lin1 vdd! Vh1) voltage_source2
I325 (0 lin2 vdd! Vh1_c) voltage_source2
I366 (INB) rand_bit_stream tperiod=1/(2*f) seed=seed vlogic_high=0 \ 
  vlogic_low=1.8 tdel=7.57n+d_shift trise=30p tfall=30p
I311 (net0156) rand_bit_stream tperiod=1/(2*f) seed=seed vlogic_high=A \ 
  vlogic_low=0 tdel=0 trise=30p tfall=30p
I2q (net056) rand_bit_stream tperiod=1/(2*f) seed=seed vlogic_high=0 \ 
  vlogic_low=A tdel=0 trise=30p tfall=30p
I365 (IN) rand_bit_stream tperiod=1/(2*f) seed=seed vlogic_high=1.8 \ 
  vlogic_low=0 tdel=7.57n+d_shift trise=30p tfall=30p
I320 (CLK CLK1 CLKB CLKB1 0 H1_oddb H1_odd 0 0 Ih2_odd net0152 Imain3 \ 
  Imain4 CIS_odd_s0_n CIS_odd_s1_n CIS_odd_s0_p CIS_odd_s1_p vdd! \ 
  Vh1 Vh1_c SH_odd_s1_n SH_odd_s1_p) .sub1
I314 (CLKB CLKB1 CLK CLK1 0 H1_evenb H1_even 0 0 Ih2_even net0153 Imain1 \ 

77
APPENDIX A. SPICE NETLIST FOR PROPOSED AREA EFFECTIVE DFE

Imain2 CIS_even_s0_n CIS_even_s1_n CIS_even_s0_p CIS_even_s1_p \n vdd! Vh1 Vh1_c SH_even_s1_n SH_even_s1_p) _sub1
R2 (Vh1 0) resistor r=20
R3 (Vh1_c 0) resistor r=50
R5 (vdd! net0134) resistor r=20K
R6 (net0133 0) resistor r=1K
I354 (0 net035 net068 SA_odd_s0_n SA_odd_s0_p vdd!) \n   modified_SR_vthn_p_v1.2
I351 (0 net063 net033 SA_even_s0_n SA_even_s0_p vdd!) \n   modified_SR_vthn_p_v1.2
I353 (0 net074 net075 SA_odd_s1_n SA_odd_s1_p vdd!) \n   modified_SR_vthn_p_v1.2
I352 (0 net031 net030 SA_even_s1_n SA_even_s1_p vdd!) \n   modified_SR_vthn_p_v1.2
Index

current-integrating summer, 21

decision feedback equalizer, 6

first-tap speculation, 11

switched-capacitor, 35