A NOVEL SINGLE-STAGE INVERTER TOPOLOGY

A Thesis Presented

By

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To my parents

Md Azizur Rahman Chowdhury & Mahbuba Begum

To my brothers

Afif & Monim
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# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Chapter 1</th>
<th>Introduction .................................................................</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Background ..................................................................</td>
<td>1</td>
</tr>
<tr>
<td>1.2</td>
<td>Importance of Inverters in Some Common Applications ...........</td>
<td>1</td>
</tr>
<tr>
<td>1.3</td>
<td>Inverter Classifications ................................................</td>
<td>5</td>
</tr>
<tr>
<td>1.4</td>
<td>State of the art Single Stage Inverters ............................</td>
<td>7</td>
</tr>
<tr>
<td>1.5</td>
<td>Research Objective and Outline .......................................</td>
<td>19</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Chapter 2</th>
<th>Principles of the Operation ..........................................</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>Proposed Configuration and Principles of the Operation .......</td>
<td>22</td>
</tr>
<tr>
<td>2.1.1</td>
<td>Hard-Switching Configuration .........................................</td>
<td>24</td>
</tr>
<tr>
<td>2.1.2</td>
<td>Soft-Switching Configuration ...........................................</td>
<td>27</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Chapter 3</th>
<th>Design, Analysis and Control .......................................</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Design Procedure and Analysis of the Proposed Inverter .......</td>
<td>32</td>
</tr>
<tr>
<td>3.2</td>
<td>Control of Hard Switching Configuration ..........................</td>
<td>36</td>
</tr>
<tr>
<td>3.3</td>
<td>Control of Soft Switching Configuration ...........................</td>
<td>38</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Chapter 4</th>
<th>Simulation and Experimental Results ................................</th>
<th>40</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>Simulation Results .....................................................</td>
<td>41</td>
</tr>
<tr>
<td>4.2</td>
<td>Experimental Results ...................................................</td>
<td>45</td>
</tr>
<tr>
<td>Chapter 5</td>
<td>Conclusion and Future Work</td>
<td>47</td>
</tr>
<tr>
<td>-----------</td>
<td>----------------------------</td>
<td>----</td>
</tr>
<tr>
<td>5.1</td>
<td>Conclusion</td>
<td>47</td>
</tr>
<tr>
<td>5.2</td>
<td>Future Work</td>
<td>48</td>
</tr>
<tr>
<td>References</td>
<td></td>
<td>49</td>
</tr>
</tbody>
</table>
LIST OF TABLES

4.1 Parameters of the Simulated Inverter................................. 40
4.2 Parameters of the Prototype............................................. 41
**LIST OF FIGURES**

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Use of inverters in distributed generation system</td>
<td>2</td>
</tr>
<tr>
<td>1.2</td>
<td>Use of inverter in an Electric vehicles</td>
<td>3</td>
</tr>
<tr>
<td>1.3</td>
<td>Use of inverter in UPS</td>
<td>4</td>
</tr>
<tr>
<td>1.4</td>
<td>Traditional buck inverter with line-frequency transformer</td>
<td>6</td>
</tr>
<tr>
<td>1.5</td>
<td>Multiple-stage inverter with a high frequency transformer</td>
<td>6</td>
</tr>
<tr>
<td>1.6</td>
<td>Voltage source inverter</td>
<td>7</td>
</tr>
<tr>
<td>1.7</td>
<td>Current source inverter</td>
<td>8</td>
</tr>
<tr>
<td>1.8</td>
<td>Z- Source inverter</td>
<td>10</td>
</tr>
<tr>
<td>1.9</td>
<td>Four-switch boost inverter proposed in</td>
<td>11</td>
</tr>
<tr>
<td>1.10</td>
<td>Four-switch buck-boost inverter proposed in</td>
<td>12</td>
</tr>
<tr>
<td>1.11</td>
<td>Four-switch buck-boost inverter proposed in</td>
<td>13</td>
</tr>
<tr>
<td>1.12</td>
<td>Four-switch isolated bidirectional buck-boost inverter proposed in</td>
<td>14</td>
</tr>
<tr>
<td>1.13</td>
<td>Four-switch resonant buck-boost inverter proposed in</td>
<td>16</td>
</tr>
<tr>
<td>1.14</td>
<td>Six-switch isolated buck-boost inverter proposed in</td>
<td>17</td>
</tr>
<tr>
<td>1.15</td>
<td>Six-switch buck-boost inverter proposed in</td>
<td>18</td>
</tr>
<tr>
<td>2.1</td>
<td>DC-DC Ćuk Converter</td>
<td>20</td>
</tr>
<tr>
<td>2.2</td>
<td>DC-DC Ćuk Converter when the input switch M is closed</td>
<td>21</td>
</tr>
<tr>
<td>2.3</td>
<td>DC-DC Ćuk Converter when switch M is open</td>
<td>21</td>
</tr>
<tr>
<td>2.4</td>
<td>Hard-switching configuration</td>
<td>22</td>
</tr>
<tr>
<td>2.5</td>
<td>Soft-switching configuration</td>
<td>23</td>
</tr>
</tbody>
</table>
Figure 2.6 Soft-switching configuration with galvanic isolation .......................... 23

Figure 2.7 Behavior of the proposed inverter (hard switching configuration)
during different modes of operation

Figure 2.7(a) Charging ......................................................................................... 25

Figure 2.7(b) Discharging when Vac is positive ............................................. 25

Figure 2.7(c) Discharging when Vac is negative ............................................ 26

Figure 2.8 Link current and link voltage in the hard-switching configuration... 26

Figure 2.9 Behavior of the soft-switching configuration during different
modes of operation

Figure 2.9 (a) Mode 1 when Vac is positive or negative .............................. 28

Figure 2.9 (b) Mode 2 and second stage of mode 4 when Vac is positive ...... 28

Figure 2.9 (c) Mode 2 and second stage of mode 4 when Vac is negative .... 29

Figure 2.9 (d) Mode 3 when Vac is positive ..................................................... 29

Figure 2.9 (e) Mode 3 when Vac is negative .................................................... 30

Figure 2.9 (f) First stage of mode 4 when Vac is negative or positive ......... 30

Figure 2.10 Link voltage and link current in the soft switching configuration... 31

Figure 3.1 One cycle of the link voltage ............................................................ 35

Figure 3.2 Output reference voltage, current, and power ............................ 35

Figure 3.3 Output reference voltage and duty cycle ....................................... 36

Figure 3.4 Control block diagram of the hard-switching configuration .... 37

Figure 3.5 Control block diagram of the soft-switching configuration ....... 39

Figure 4.1 Load voltage in the soft-switching configuration ....................... 41

Figure 4.2 Load current in the soft-switching configuration ....................... 42
Figure 4.3  Link voltage and current in the soft-switching configuration  ....  42
Figure 4.4  Input current in the soft-switching configuration  ..................  42
Figure 4.5  Unfiltered input voltage in the soft-switching configuration ....  43
Figure 4.6  Unfiltered load voltage in the soft-switching configuration  ....  43
Figure 4.7  Current through and voltage across the input side switch (S0) and its anti-parallel diode in the soft-switching configuration  43
Figure 4.8  Zoomed current through and voltage across the input side switch (S0) in the soft-switching configuration  ..................  44
Figure 4.9  Link voltage and current in the hard-switching configuration  ....  44
Figure 4.10  Load current and duty cycle of the input side switch over the two load  .................................................................  44
Figure 4.11  Load current (2 A/div) and voltage (50 V/div) in the hard switching configuration, time scale: 4 ms/div  ......................  45
Figure 4.12  Input current (2 A/div) in the hard-switching configuration, time scale: 10 ms/div  ......................................................  45
Figure 4.13  Link voltage (100 V/div) and unfiltered input voltage (100 V/div) in the hard-switching configuration, time scale: 40 µs/div  ....  46
Figure 4.14  Link voltage (100 V/div) and unfiltered output voltage (100 V/div) in the hard-switching configuration, time scale: 40 µs/div  ....  46
ABSTRACT

Inverters are considered key components to enable the integration of renewable energy sources into the grid. These power processing circuits convert dc voltage into ac, and are needed in numerous applications, including residential photovoltaic (PV) systems. The state of the art inverters have several shortcomings such as limited voltage gain, low power density, high failure rates, and low efficiency.

This thesis proposes a new inverter topology that can overcome the problems associated with most conventional inverters. The proposed inverter is a single stage configuration, and employs five semiconductor switches, in which one is operating at a high frequency and the rest are operating at the fundamental frequency of the load. The proposed inverter is capable of both stepping up and stepping down the voltage. This is a unique advantage over most state of the art single-stage inverters, which can either step up or step down the voltage. In the proposed inverter, a small capacitor transfers power from the input towards the output. The inverter is designed and controlled such that the required link capacitance is very low; therefore, film capacitors that have longer lifetime compared to electrolytic capacitors can be used. Unlike most conventional isolated inverters that use low frequency transformer (LFT), in the proposed inverter a high frequency transformer (HFT) can be used for providing galvanic isolation. This feature decreases the total size of the system. The proposed inverter can be modified slightly to offer soft-switching, which significantly increases the efficiency.

In this thesis, the principles of the operation of the proposed inverter is studied, and its performance is evaluated through simulation and experiment.
Chapter 1

Introduction

1.1 Background

Global electricity consumption is increasing continuously, and is expected to reach 24,673 TWh in 2025 at an average annual growth rate of 2.4% [1, 2]. With the increase of power consumption, research areas focusing on power and energy are also broadening. Nowadays electric power processing circuits are needed for almost every computer systems, industrial motor drives, home appliances, renewable energy systems, etc. Among the most common and important types of power processing circuits are the inverters that generate ac voltage from a dc power source. An inverter takes power from a dc source and makes it usable for an ac load such as a utility grid, an ac motor, or any conventional product normally powered from an ac line [3]. The applications include a wide range from small household equipment to space ships.

1.2 Importance of Inverters in Some Common Applications

With the increase of power consumption rate we need more power sources besides the fossil fuels and hydro power sources. Renewable energy sources, especially Photovoltaic (PV) and wind energy systems, are expected to play critical roles as the next generation power sources. Renewable energy sources can form Distributed Generation (DG) systems to supply local loads. In comparison to the conventional power generation system, distributed power resources are more flexible. Also, by using DG systems the electricity
can be produced at the close proximity of location where it is consumed, and the losses across the transmission lines can be lessened [4, 5]. Inverters play a vital role in DG systems. Figure 1.1 shows a distributed power system formed by solar panels, fuel cells, and wind energy system. As seen in this figure, inverters are integral parts of the system, and allow connecting renewable energy sources to grid, although these sources have different voltage amplitudes, forms, and frequencies.

Figure 1.1. Use of inverters in distributed generation system [6]
Inverters are also used in Electric Vehicles (EVs) and Hybrid Electric Vehicles (HEVs) to supply and control the traction motor. There has been demand in recent years to increase the power level and reduce the size of the inverters so that they can fit into the limited space available in these vehicles [7]. Figure 1.2 shows drivetrain of a plug-in hybrid electric vehicle. The vehicle uses an inverter to supply and control an electric motor that drives the wheels. Torque and speed of the electric motor are controlled through regulating the currents and voltages of the inverter.

Figure 1.2. Use of inverter in an electric vehicle [8]
Another application for inverters include Uninterruptable Power Supplies (UPS). Figure 1.3 shows a simplified block diagram of an UPS. In normal operation the main power supplies the load. During this period A and C are connected to supply the load while the battery of the UPS system is charged with the help of a rectifier that converts ac voltage into dc. When the main supply power is interrupted, terminals B and C get connected by a relay mechanism, and the battery supplies the load. In this case dc voltage of the battery is converted into ac through an inverter.

Figure 1.3. Use of inverter in UPS [9].
1.3 Inverter Classifications

Inverters can be classified as single-phase or three-phase according to the number phases of the ac load. In some applications inverters with more number of phases are required. In this thesis we will focus on single-phase inverters.

Inverters can also be classified as single-stage and multiple-stage inverters. A single stage inverter is defined as an inverter with only one stage of power conversion. These inverters can step-up (boost), step-down (buck), or both step-up and step-down the voltage (buck-boost) while generating sinusoidal load current and voltage. A multiple-stage inverter requires more than one power conversion stage. Most commonly used multiple-stage inverters are listed as below -

1) dc–dc–ac topologies
2) dc–ac–dc–ac topologies
3) dc–ac–ac topologies

The focus of this thesis is single-stage inverters.

Moreover, inverters can be classified based on the electrical isolation between the source and load, as isolated and non-isolated inverters. Electrical isolation can generally be achieved by using transformers. Depending on the topology, a choice can be made between uses of line-frequency transformers as shown in Figure 1.4 or high-frequency transformers as shown in Figure 1.5.
Figure 1.4. Traditional buck inverter with line-frequency transformer.

Figure 1.5. Multiple-stage inverter with a high frequency transformer.
1.4 State of the art Single Stage Inverters

In this section the state-of-the-art single-stage single phase inverter topologies are discussed.

1. Voltage Source Inverter (VSI)

Voltage source inverters are the most common inverter topology. A VSI has a voltage source and a current sink, and it is in essence a step-down (buck) inverter. Therefore, in order to step up the voltage when a VSI is used, we need to add another stage, i.e. a dc-dc converter, to the inverter or use a low-frequency transformer as shown in Figure 1.4. Adding another power processing stage requires decoupling the dc-dc converter and the inverter through large capacitors. If electrolytic capacitors are use, the reliability of the inverter will be deteriorated. Use of low frequency transformers reduces the power density, because low frequency transformers are bulky and heavy. Figure 1.6 shows the schematic of this topology.

![Figure 1.6. Voltage source inverter](image)
2. Current Source Inverter (CSI)

Current source inverters, shown in Figure 1.7, are formed by a current source and a voltage sink, and are step-up (boost) inverters. Current source is formed by placing an inductor in series with a voltage source. As seen in Figure 1.7 in this topology reverse blocking switches are needed, and this can increase conduction losses. CSIs are only capable of stepping up the voltage; therefore, similar to VSIs they have limited voltage gain. In case isolation is needed a low frequency transformer is needed to be used.

![Figure 1.7. Current source inverter](image-url)
3. Z-Source Inverter (ZSI)

As mentioned earlier, voltage and current source inverters have some constrains. In VSI the output voltage level is always lower than the input voltage, and. CSI is only capable of boosting up the input voltage. In both VSI and CSI EMI noise’s mis-gating can cause major problems. VSI will be damaged if this mis-gating leads to shoot-through, and CSI will be damaged if the mis-gating creates an open circuit [10]. To overcome the problems associated with the traditional VSI and CSI, the Z-Source Inverter (ZSI) was introduced in [10]. Figure 1.8 shows a single phase Z-source inverter, which is capable for both step up and step down conversion. The Z-source concept can be used for dc-to-ac, ac to-dc, ac-to-ac, and ac-to-dc conversion. In single phase inverter, conversion takes place with the help of five switching states. The states can be explained as two active states when either the switch pair (S1 & S4) or switch pair (S2 & S3) is turned on. In this state the output load is connected with the dc voltage. There are two zero states when the load terminals are shorted through the upper pair (S1 & S2) or the lower pair (S3 & S4) switches. Another state is shoot-through state, when the load terminals are shorted with the help of an upper switch and a lower switch on one of the legs. During shoot-through state input inductors are charged for boost operation as one of the legs of the bridge is shorted.

If galvanic isolation is required, a low frequency transformer can be used at the output of the Z-source inverter.
A non-isolated boost inverter, shown in Figure 1.9, was proposed in [11]. In this topology two identical parallel dc-dc boost converters are connected to a dc source, and the load is connected across the outputs of the two converters. Each converter is modulated to produce a unipolar dc-biased sinusoidal output with a 180 degree phase difference with the other. The load is connected differentially with the two converters; therefore, the differential dc bias voltage across the load is zero. The generation of the bi-polar voltage across the load is generated with a push-pull mechanism. When the switch S1 is closed and the switch S2 is open, diode D2 is in reverse biased and inductor L1 is charged. Therefore, the current of the inductor, $i_{L1}$, increases linearly. At this state capacitor C1 provides energy to the load, and voltage $V1$ decreases. In the next state when S1 is open and S2 is closed, current $i_{L1}$ flows through capacitor C1 and load [11]. Therefore, current $i_{L1}$ decreases while capacitor C1 is charged. For the other converter switches S3, S4 and capacitor C2 play the
role of the switches S1 and S2 and capacitor C2, respectively. Depending on the duty cycle of the switches, in this inverter the voltage can be stepped up without using bulky transformers or having additional power processing stage. However, for this inverter the switches suffer from high voltage stress when the gain is large [12]. Moreover, galvanic isolation can only be provided by a low frequency transformer.

Figure 1.9. Four-switch boost inverter proposed in [11].
5. Figure 1.10 shows another inverter topology proposed in [12] that uses a similar technique as Figure 1.9. In this topology instead of two boost converters, two buck-boost dc–dc converters are connected to generate an AC output voltage, which can be lower or higher than the dc input voltage. In this inverter, similar to four-switch boost inverter, switches suffer from high voltage stress when voltage gain is high. However, voltage stress over capacitors is lower in this inverter [12]. Similar to four-switch boost inverter galvanic isolation can only be provided by a low frequency transformer.

![Four-switch buck-boost inverter](image)

**Figure 1.10.** Four-switch buck-boost inverter proposed in [12].
6. Another transformer-less single phase buck-boost inverter, shown in Figure 1.11, was proposed in [13]. The main advantage of this inverter is that it can operate with a wide range of input voltage. A major drawback of this inverter is that it requires two dc input voltage sources. For this topology two buck-boost converters share one single output, and each operates for half cycle of the output voltage using its own supply source [13]. During one half cycle of the output voltage the switches T3 and T4 are open and the other two switches perform the power conversion process. During the other half cycle of the output voltage switches T3 and T4 are controlled to perform power conversion while switches T1 and T2 are off. The duty cycles of the switches are controlled such that the inverter can provide a sinusoidal output voltage [13]. Galvanic isolation can be provided by adding a low frequency transformer.

![Four-switch buck-boost inverter proposed in [13].](image)

Figure 1.11. Four-switch buck-boost inverter proposed in [13].
7. A dual flyback inverter was proposed in [14], which is depicted in Figure 1.12. In this topology two bidirectional flyback converters were connected to form the main circuit and the load is connected across the outputs of those two converters. Principle of the operation of this inverter is similar to that presented in [11] and [12]. This inverter can both step up and step down the voltage. Moreover, it provides galvanic isolation by two high frequency transformers [15].

![Figure 1.12. Four-switch isolated bidirectional buck-boost inverter proposed in [14].](image)

8. A full-bridge series-resonant buck-boost inverter topology, proposed in [16, 17], is depicted in Figure 1.13. In this inverter switches benefit from zero-current-switching (ZCS). This inverter uses only a single full-bridge topology with an LC resonant tank without any supplementary switches. Unlike regular VSI, which can only step down the voltage, this inverter can both step up and step down the voltage depending on the
instantaneous duty cycle. In one half cycle of the output voltage, two switches and one diode (S1, S3, and D2) operate and in the other half cycle the other two switches and the other diode (S2, S4, and D1) operate. Switches S1, S2, S3, and S4 are all unidirectional.

There are three states in each high frequency cycle. The first state begins with turn-on of switch S3 with zero current switching (ZCS). During this state switches S1 and S3 conduct, and the resonant inductor L1 charges with the input dc voltage while the resonant capacitor Cr discharges its energy to the load. The second state begins by turning off switch S3. By turning off S3, diode D2 starts to conduct, and the energy stored in the inductor L1 transfers to the capacitor Cr and the load. The third state begins when L1 is fully discharged and the diode stops conducting. At this time resonant capacitor discharges its energy to the load until switch S3 is turned on. During this half cycle of the output voltage S1 remains on while S2 and S4 remain off for the whole switching period. For the other half cycle of the output voltage, S2 remains on while S1 and S3 remain off [16]. The LC series-resonant tank allows switches S3 and S4 to be turned on at zero current, and have a low switching loss [17]. This inverter can provide galvanic isolation by adding a low frequency transformer.
Figure 1.13. Four-switch resonant buck-boost inverter proposed in [16, 17].

9. Figure 1.14 depicts an isolated buck-boost inverter, which was proposed in [18]. This inverter combines two buck-boost dc-dc converters through a four-switch bridge with two additional switches used for synchronous commutation in each half cycle of ac output. The prime advantages of this inverter include possibility of both stepping up and stepping down the voltage irrespective of the input voltage, as well as providing electrical isolation between the input source and the utility through high frequency transformers. In this PWM power inverter the two high frequency buck-boost converters operate mainly in the discontinuous conduction mode [18]. During the positive cycle of the load voltage switches Q2 and Q2’ are off, and switch Q1’ is on. The amplitude of the voltage is controlled through Q1 during this half cycle. This inverter has three operating states for the power conversion. During the first state switch Q1 is on, and the energy is stored in the inductor L at the primary side, while at the secondary side the energy stored in capacitor C during the previous state is supplied to the load. During the second state Q1 is off and the stored
energy of L is transferred to the load and capacitor C through Q1’ and diode in parallel with Q2’. During the third state none of the switches conduct, and capacitor C provides power to load. During the negative cycle of the load voltage switches Q1 and Q1’ are off, switch Q2’ is on, and the amplitude of the voltage is controlled through Q2. For the negative cycle switch Q2 is on during the first state, and it is off during the second and third states [18].

![Diagram of Six-switch isolated buck-boost inverter](image)

**Figure 1.14. Six-switch isolated buck-boost inverter proposed in [18].**

10. Figure 1.15 shows a nonisolated buck-boost inverter topology proposed in [19] that uses six switches for generating an ac voltage [15]. The performance of this inverter is similar to a buck-boost converter, and can operate in both Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). Mode of operation is determined based on the load current, size of the link inductance, and switching frequency [19]. During the negative half cycle of the output voltage switches A, D, F and the anti-parallel diode of switch E are involved in transferring power from the source to the load. During the positive
half cycle the load voltage, switches B, C, E and the anti-parallel diode of switch F are used. The main advantage of this inverter is that it can both step up and step down the voltage; however, it cannot provide galvanic isolation through high frequency transformers. Moreover, the number of required switches is more than that of topologies discussed earlier.

Figure 1.15. Six-switch buck-boost inverter proposed in [19].
1.5 Research Objective and Outline

As mentioned earlier despite having low cost and simple configuration and control, state of the art single stage inverters have limitations that can cause a compromised system performance. Among these limitations, the most commons are limited voltage gain, high voltage stress, or necessity of using bulky low frequency transformers for providing isolation [20, 21]. These limitations necessitates using multiple stage inverters in some applications. Multiple-stage inverters can address problems associated with single-stage inverters; however, they increase the cost and lower the efficiency.

This thesis proposes a novel single stage inverter topology that is capable of solving the problems associated with the state of the art single stage inverters. This inverter, which belongs to a new class of universal converters recently proposed in [22, 23], is an extension of a Ćuk converter, and is capable of both stepping up and stepping down the voltage [24]. The link capacitor, which is responsible for transferring the power from the input to the output, does not require to have a high capacitance. Therefore film capacitors that are much more reliable than electrolytic capacitors can be used, and the proposed inverter will benefit from a longer lifetime. If galvanic isolation is required a high frequency transformer can be added to the link. Moreover, to increase the efficiency of the inverter, a small inductor can be added to the link to allow the switches benefit from the soft-switching.

In chapter II of this thesis principles of the operation of the proposed inverter as well as its design, analysis, and control will be discussed in chapter III. Simulation and experimental results will be presented in chapter IV and chapter V will summarizes this thesis.
Chapter 2

Principles of the Operation

This thesis work proposes a new inverter topology, which is an extension of a Ćuk converter. Therefore, the link capacitor is responsible for transferring the power from the input towards the output. In this topology a film capacitor is used instead of an electrolytic capacitor to avoid the problems associated with lifetime and reliability of electrolytic capacitors. Figure 2.1 depicts a simple DC to DC Ćuk converter, and Figures 2.2 and 2.3 show the discharging and charging modes of the link capacitor C1 when switch M is turned ON and OFF, respectively.
The proposed inverter topology, which operates based on the working principles of a Ćuk converter, uses the combination of an input switch and a full bridge. The full bridge consists of four switches with anti-parallel diodes, and generates the positive and negative half cycles of the output voltage. In this section the working principles of the proposed inverter will be discussed.
2.1. Proposed Configuration and Principles of the Operation

The proposed inverter is shown in Figure 2.4. Similar to dc-dc Ćuk converter, the link capacitor, in the proposed inverter, is first charged from the input, and then it is discharged into the output. To increase the efficiency of the inverter, an inductor can be added to the link to allow the switches benefit from the soft-switching. This configuration is depicted in Figure 2.5. To provide galvanic isolation, a HFT can be added to the link. The schematic of the galvanic-ally isolated configuration is shown in Figure 2.6.

![Figure 2.4. Hard-switching configuration](image-url)
Figure 2.5. Soft-switching configuration

Figure 2.6. Soft-switching configuration with galvanic isolation
2.1.1 Hard-Switching Configuration

Figure 2.7 depicts the behavior of the hard-switching configuration during the charging and discharging modes. When the capacitor is being charged, the output side switches should provide a path for the link current as well as the load current, which is shown in Figure 2.7(a). During the discharging mode the input side switch is turned on to provide a path for the input current and the link current while the output side switches are controlled such that a negative current discharges the link capacitor, which is shown in Figures 2.7(b) and 2.7(c) for the positive and negative cycles of the output voltage, respectively. Link voltage is positive during both charging and discharging modes; therefore, if the load voltage is positive switches S2 and S3 will be turned on during the discharging mode; and if the output voltage is negative switches S1 and S4 will be turned on for discharging the link capacitor. Figure 2.8 depicts the link current and voltage for the hard-switching configuration. The inverter is controlled such that regardless of the operating point, it operates at the boundary of the continuous and discontinuous conduction modes. This leads to choosing a very small link capacitance to reduce the size of the system.
(a) Charging

(b) Discharging when $V_{ac}$ is positive
(c) Discharging when $V_{ac}$ is negative

Figure 2.7. Behavior of the proposed inverter (hard switching configuration) during different modes of operation

Figure 2.8. Link current and link voltage in the hard-switching configuration
2.1.2 Soft-Switching Configuration

In the soft-switching tropology a small inductor is connected in series with the link capacitor. The principles of the operation of the soft-switching configuration is depicted in Figure 2.9. In this configuration, between each power transfer mode, the link, which is formed by series capacitor and inductor, needs to be shorted to allow the switches to benefit from the zero current turn-off and soft turn-on. For both the positive and negative cycles of the output voltage, four modes are required in each cycle to transfer the entire power from the input to the output side. Similar to the hard switching configuration, the link capacitor is charged in the first mode. During this mode the input side switch (S0) is open and output side switches are closed to provide a path for the input current to charge the link capacitor through D1-D4, as illustrated in Figure 2.9(a). The second mode, as shown in Figure 2.11(b) and 2.9(c) starts by turning on the input side switch, which initiates a resonating mode to provide soft switching. During this mode the link current decreases and its polarity changes. When the current of two antiparallel diodes across the output switches (D1 and D4) or (D2 and D3) become zero, the link current becomes equal to the output current. The third mode, as illustrated in Figure 2.9(d) starts when this condition happens. During this mode the energy stored in the capacitor is delivered into the load. Again, the fourth mode, as depicted in Figure 2.9(f) is a resonating mode which starts by turning on all the switches. This results in the link current to increase to a maximum predetermined positive value, $I_{\text{max}}$, which is higher than the input current. When the link current becomes higher than the input current, switches S1 and S4 (for positive output voltage) or switches S2 and S3 (for negative output voltage) will be turned off. This initiates the second stage of mode 4, as shown in Figures
2.9(b) and 2.9(c). Figure 2.10 shows the link voltage and link current for the soft-switching configuration.

(a) Mode 1 when Vac is positive or negative

(b) Mode 2 and second stage of mode 4 when Vac is positive
(c) Mode 2 and second stage of mode 4 when Vac is negative

(d) Mode 3 when Vac is positive
Figure 2.9. Behavior of the soft-switching configuration during different modes of operation.
Figure 2.10. Link voltage and link current in the soft switching configuration
Chapter 3

Design, analysis and control

3.1 Design Procedure and Analysis of the Proposed Inverter

In this part, design and analysis of the proposed configuration is described. Figure 3.1 depicts the link voltage in the hard switching configuration. Suppose that the instantaneous output reference voltage and current, shown in Figure 3.2, are expressed as follows:

\[ v_o(t) = V_m \sin(\omega_o t) \]  \hspace{1cm} (1)

\[ i_o(t) = I_m \sin(\omega_o t + \theta) \]  \hspace{1cm} (2)

Using (1) and (2) the output power (see Figure 3.2) will be as follows:

\[ p_o(t) = \frac{V_m I_m}{2} \left[ \cos \theta - \cos(2\omega_o t + \theta) \right] \]  \hspace{1cm} (3)

The instantaneous input power is equal to:

\[ p_in(t) = V_{dc} i_{in}(t) \]  \hspace{1cm} (4)

Considering a lossless system and using (4), the instantaneous input current is obtained as follows:

\[ i_{in}(t) = \frac{V_{dc}}{2V_{dc}} \left[ \cos \theta - \cos(2\omega_o t + \theta) \right] \]  \hspace{1cm} (5)

Where \( V_{dc} \) is the dc input voltage.
According to Figure 3.1, when operating at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM), in each cycle the following key equations should be satisfied:

\[ I_{in} = C \frac{V_p}{t_c} \]  \hspace{1cm} (6)

\[ I_o = C \frac{V_p}{t_d} \]  \hspace{1cm} (7)

\[ t_c + t_d = T_{link} \]  \hspace{1cm} (8)

Where \( t_c, t_d, T_{link} \) are charging time, discharging time, and duration of one cycle, respectively. The duty cycle of the input side switch can be calculated as:

\[ d_i(t) = \frac{t_c}{t_c + t_d} = \frac{i_o(t)}{i_o(t) + i_{in}(t)} \]

\[ = \frac{I_m \sin(\omega_o t + \theta)}{I_m \sin(\omega_o t + \theta) + \frac{V_m I_m}{2V_{dc}} \left[ \cos \theta - \cos(2\omega_o t + \theta) \right]} \]  \hspace{1cm} (9)

Figure 3.3 is showing the duty cycle of the inverter. According to Figure 3.1, the input and output power can be rewritten as:

\[ P_{in}(t) = V_{dc} i_{in}(t) = \frac{1}{2} \left[ V_p(t) i_{in}(t) \frac{t_c}{T} \right] \]  \hspace{1cm} (10)
\[ p_o(t) = v_o(t)i_o(t) = \frac{1}{2} \left[ V_p(t)i_o(t) \frac{t_d}{T} \right] \]  

(11)

Using (8), (10), and (11), the link peak voltage \( V_p \) can be calculated by (12) as follows:

\[ V_p(t) = 2[V_{dc} + V_m \sin(\omega_o t)] \]  

(12)

It can be shown that the link capacitance is equal to:

\[ C = \frac{P}{2f_{\text{link}} (V_p)^2} \]  

(13)

Where \( f_{\text{link}} \) is the link frequency at the average power of \( P \), and \( V_p \) is the link peak voltage at this power.

For the soft-switching configuration, inductance \( L \) of the link can be determined as:

\[ L = \frac{1}{4\pi^2 f_{\text{link}}^2 C} \]  

(14)

In the above equations maximum link frequency is a design parameter that can be determined based on the power rating of the system; however, in practice it is limited by sampling time of the microcontroller in order to have enough number of samples in each cycle for achieving desirable performance [24]. Furthermore, since during the resonating modes no power can be transferred, it is preferred to keep these modes as short as possible, in this way link inductance in (14) is chosen such that the resonating periods are retained within a small percentage of the link cycle. Maximum current of the link \( (I_{\text{max}}) \) is another factor for controlling the resonating periods based on the energy of the link. By increasing
$I_{\text{max}}$, we will have longer resonating periods. Thus, $I_{\text{max}}$ should be considered slightly higher than the maximum peak of the input and output currents to keep the resonating modes as short as possible.

![Figure 3.1. One cycle of the link voltage](image1)

![Figure 3.2. Output reference voltage, current, and power](image2)
3.2 Control of Hard Switching Configuration

For the hard switching configuration, charging and discharging times are calculated based on the link capacitance as well as input and output reference currents and voltages using (6), (7), (12), and (13). By knowing $t_c$ and $t_d$, we can turn on and off the proper input and output switches. Depending on the polarity of the output reference voltage, the output switches S1, S4 or S2, S3 needs to be turned on. In each link cycle, before reaching the instant when time is equal to the calculated value of $t_c$, the input switch S0 is maintained to be off in the charging state. Once this happens the discharging state begins and S0 needs to be turned on. Figure 3.4 shows the block diagram of the control in hard switching configuration.
Figure 3.4. Control block diagram of the hard-switching configuration
3.3 Control of Soft Switching Configuration

The control block diagram of the soft-switching configuration is depicted in Figure 3.5. As seen in the figure, first, the reference input current can be calculated from (5) based on specification of the inverter. Then the maximum current of the link \( I_{\text{max}} \) for calculating energy of the link during mode 3 is determined. According to the mode of the operation, proper switches are turned on or off. For the proposed configuration input switch (S0) is turned on when the input actual current reaches a predetermined value which is slightly lower than the input reference current. This is the end of mode 1, and once this happens mode 2, which is a resonating mode, starts. When link current is negative and its magnitude is equal to the output current, mode 3 starts. Mode 3 is terminated when there is just enough energy left in the link to allow the link current to swing to \( I_{\text{max}} \). After that another resonating mode begins by turning on all the switches. In this resonating mode, once the link current is positive and higher than the input current, the proper output switches based on the polarity of the output reference voltage are kept on while the other output switches and the input switch are turned off.
(Vor<0) S1=1, and S4=1
(Vor>0) S2=1, and S3=1
S0=0

Yes

I_link=I_i

No

(Vor<0) S1=1, and S4=1
(Vor>0) S2=1, and S3=1

S0=1

I_link=|I_r|

Yes

No

Energy<ΔE*

Yes

No

(Vor<0) S1=1, and S4=1
(Vor>0) S2=1, and S3=1
S0=0

I_link>I_i

Yes

No

Figure 3.5. Control block diagram of the soft-switching configuration
Chapter 4

Simulation and Experimental Results

In this section the performance of the proposed inverter is verified through simulation and experimental results. A 1000 W soft-switching configuration is designed and simulated. Furthermore, a 100W hard-switching configuration is designed and fabricated to experimentally evaluate the performance of the inverter. The parameters of these inverters are listed in Tables 4.1, and 4.2

Table 4.1

Parameters of the simulated inverter-

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>dc Voltage</td>
<td>200 V</td>
</tr>
<tr>
<td>ac Voltage</td>
<td>170 V</td>
</tr>
<tr>
<td>Link inductance</td>
<td>10 µH</td>
</tr>
<tr>
<td>Link Capacitance</td>
<td>100 nF</td>
</tr>
</tbody>
</table>
Table 4.2

Parameters of the prototype -

<table>
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<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>dc Voltage</td>
<td>60 V</td>
</tr>
<tr>
<td>ac Voltage</td>
<td>100 V</td>
</tr>
<tr>
<td>Link Capacitance</td>
<td>1.2 µF</td>
</tr>
</tbody>
</table>

4.1 Simulation Results

Figures 4.1 and 4.2 depict the output voltage and current. Figure 4.3 shows the link voltage and the link current for soft switching configuration. The input side current is shown in Figure 4.4. Figures 4.5 and 4.6 demonstrate unfiltered input and output voltages, respectively. The soft turn-on and turn-off of the input side switch (S0) are verified in Figures 4.7 and 4.8. Figure 4.9 shows the link voltage and link current for hard switching configuration and the figure 4.10 depicts the duty cycle.

![Figure 4.1. Load voltage in the soft-switching configuration](image-url)
Figure 4.2. Load current in the soft-switching configuration

Figure 4.3. Link voltage and current in the soft-switching configuration

Figure 4.4. Input current in the soft-switching configuration
Figure 4.5. Unfiltered input voltage in the soft-switching configuration

Figure 4.6. Unfiltered load voltage in the soft-switching configuration

Figure 4.7. Current through and voltage across the input side switch (S0) and its anti-parallel diode in the soft-switching configuration
Figure 4.8. Zoomed current through and voltage across the input side switch (S0) in the soft-switching configuration

Figure 4.9. Link voltage and current in the hard-switching configuration

Figure 4.10. Load current and duty cycle of the input side switch over the two cycles
4.2 Experimental Results

Figures 4.11-4.14 represent the experimental results corresponding to the hard-switching configuration. Figure 4.11 illustrates the output voltage and current. The input current is depicted in Figure 4.12. Link voltage along with unfiltered input and output voltages are shown in Figures 4.13 and 4.14.

![Figure 4.11](image1.png)

**Figure 4.11.** Load current (2 A/div) and voltage (50 V/div) in the hard-switching configuration, time scale: 4 ms/div

![Figure 4.12](image2.png)

**Figure 4.12.** Input current (2 A/div) in the hard-switching configuration, time scale: 10 ms/div
Figure 4.13. Link voltage (100 V/div) and unfiltered input voltage (100 V/div) in the hard-switching configuration, time scale: 40 μs/div

Figure 4.14. Link voltage (100 V/div) and unfiltered output voltage (100 V/div) in the hard-switching configuration, time scale: 40 μs/div
Chapter 5

Conclusion and Future Work

5.1 Conclusion

In this thesis work, a novel single-phase single-stage inverter has been proposed. The proposed inverter is an extension of a Ćuk converter which is capable of stepping up or stepping down the voltage and operates at the boundary of the continuous conduction mode (CCM) and discontinuous conduction mode (DCM), resulting in a very small link capacitance and eliminating the need for an electrolytic capacitor. In this regard, a small film capacitor can be used as the main component for transferring the energy from input side to the output side, placing emphasis on reduced size and increased reliability of the proposed converter compared to the conventional ones. A small inductor can be added to the link to reinforce all the utilized switches in the inverter with soft switching technique, giving raise to negligible switching losses, and minimized current/voltage stress over the switches. Another merit of the proposed strategy is that galvanic isolation can be readily provided by adding a single-phase high frequency transformer (HFT) to the link due to the fact that the link current and voltage are of high frequency of operation. Therefore, the proposed inverter presents a compact design with a good performance-cost ratio compared to the conventional inverters with line-frequency transformers. The principles of operation, analysis, and design procedure of the proposed configuration is studied in this thesis work. A prototype has been built, with which its experimental results were verified with the theoretical and simulation results.
5.2 Future Work

1. For renewable energy systems the input voltage source fluctuates very often, so to stabilize the inverter with variable source input more robust control method should be applied.

2. The soft switching topology should be analyzed with more experiments.

3. The proposed configuration can be extended to have bidirectional flow of power.
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