ELECTRON TRANSPORT MECHANISM OF TITANIA CHAINS IN THE FRAMEWORK OF TITANOSILICATES ETS-4 AND ETS-10

A Thesis Presented

By

Önnaz Özkanat

to

The Department of Chemical Engineering

In partial fulfillment of the requirements
For the degree of

Master of Science

In the field of

Chemical Engineering

Northeastern University
Boston, Massachusetts

February 20, 2009
first steps... on the way of 300m deep
ACKNOWLEDGEMENTS

I would like to thank to my advisor Prof Albert Sacco, Jr for his trust and freedom he has provided. I also thank my committee members, Professor Nicole McGruer and Dr Bilge Yilmaz for their time and directions. I especially want to thank Dr Juliusz Warzywoda for his guidance, intelligent questions and helping me to handle my frustration throughout this work.

I would like to thank to Prof Güniz Gürüz to encourage me to start a master degree in Cammp lab; her support and encouragement have a significant influence on my career path.

My special thanks go to Peter Ryan who helped me with the probe station measurements and showed me how to be “super careful”. I would like to also thank to my labmate, Mariam Ismail for all her support.

Furthermore, I would like to thank my cousin, Begüm Ünsal, for all her support and motivation, especially during thesis write-up. Also, thanks to Yasin Celik for his encouragement and his close follow-up with the project.

Finally, I would like express my special heartfelt gratitude to my parents. Without their encouragement, 7/24 support, patience and open-minded advices; this work would have never been possible. Thank you so much for all their trust, support and the freedom you gave me.
ABSTRACT

Current techniques for preparation of low-dimensional devices present technical difficulties and concomitant costs. This is especially true in the fabrication of aligned quantum wire arrays. Microporous crystalline titanosilicate materials, ETS-4 and ETS-10, are hypothesized to have naturally occurring quantum wires in their framework. They contain monatomic titania chains (...Ti-O-Ti-O-Ti...) isolated from each other by a highly siliceous matrix. These titania chains (~ 6.7 Å in diameter) in ETS-4 run in only the $b$ direction, while they run in both $a$ and $b$ directions in ETS-10. Electron transport properties of titania chains –as hypothesized quantum wires- in the framework of individual ETS-4 and ETS-10 crystals were studied. Current-voltage performance (I-V curves) of both ETS-4 and ETS-10 were investigated at room temperature by placing 2 microprobes on the surface of the individual crystal. It was verified that conduction occurs through the defects in titania chains. Furthermore, the main feature of the current-voltage curve was identified as a current peak due to resonant electron tunneling between titania chains through the insulating layer. *Peak to Valley Ratio* (PVCR) for 15µ interval was determined as 3.4 and 5.4 for ETS-4 and ETS-10, respectively. It was observed that the PVCR’s are decreasing with increasing intervals in the direction of titania chains and for intervals larger than 150µ (ETS-4 only) these current peaks disappeared. Current-voltage curves were also obtained in the dimension/direction where there are no titania chains. The observed current jumps with a higher PVCR supports the hypothesis of resonance electron tunneling through insulating layer of SiO$_4$. Low temperature current-voltage behavior of ETS-4 was investigated by performing the device integration of large individual crystal. Non linear I-V behavior at low voltages was observed. These nonlinear
curves were attributed to electron transport through discrete titania chains via tunneling. Current values were observed to be decreasing with decreasing temperatures as expected for bulk semiconductors. However, at higher voltages, similar to the results obtained by probe station at room temperature, current jumps followed by negative differential resistance was observed. PVCR of the peaks were observed to be increasing and peaks shifted to higher resonance voltage values with decreasing temperature. Increase in PVCR upon decreasing temperature also supports the hypothesis of resonance tunneling through insulating siliceous matrix. These results taken in total provide a basis for electron transport mechanism of the monatomic titania chains in ETS crystals which can be utilized in future’s optoelectronic devices.
# TABLE OF CONTENTS

List of Figures........................................................................................................vi

List of Tables........................................................................................................xiv

1.0 Introduction.........................................................................................................1

2.0 Background.........................................................................................................4

2.1 Titanosilicates....................................................................................................5

2.1.1 Structure of Engelhard TitanoSilicate-4 (ETSk4).................................8

2.1.2 Structure of Engelhard TitanoSilicate-10 (ETSk10).........................11

2.2 Quantum Size Effect .......................................................................................16

3.0 Critical Literature Review..................................................................................20

3.1 Quantum Based Devices and Fabrication Methodologies.........................20

3.2 Electrical Transport Properties of Nanostructures and Quantum Confined
Devices.................................................................................................................34

3.3 Low Dimensional Resonant Tunneling.........................................................42

4.0 Experimental Methodologies..........................................................................56

4.1 Sample Preparation.........................................................................................56

4.1.1 Device integration of ETS-4.................................................................56

4.1.2 Samples for Probes on Crystal Surface..............................................65

4.2 Semiconductor Parameter Analysis of ETS-4 and ETS-10.....................68

5.0 Results and Discussion.....................................................................................69

5.1 Room temperature current-voltage characterization by placing
microprobes........................................................................................................69
5.2 Low temperature current-voltage characterization of ETS-4 device……..81

6.0 Conclusions……………………………………………………………………………90

7.0 Recommendations…………………………………………………………………91

8.0 References……………………………………………………………………………93

9.0 Appendices……………………………………………………………………………99

Appendix A……………………………………………………………………………100

Appendix B……………………………………………………………………………105

Appendix C……………………………………………………………………………106
LIST OF FIGURES

Figure 1: First integrated circuit: a sliver of germanium, with protruding wires, glued to a glass slide [2]………………………………………………………………….1

Figure 2: Polyhedral representation of (a) the a, b plane of Zorite showing chains of Ti octahedral, and 12 membered ring channels, (b) the a, c plane showing 8 membered ring channels [17]…………………………………………………………………………….7

Figure 3: SEM micrograph of crystalline titanium-silicate material from the unit cell composition of Na₈(Ti₂₄Si₁₂)Oₓ [17]………………………………………………..8

Figure 4: a) ETS-4 framework; octahedral titanium atoms are indicated by green. Silicon and oxygen atoms are shown in yellow and red, respectively. The a±b slice (left) shows the 12-ring opening while the a±c slice (right) shows the 8-ring opening. Pore connectivity along the a direction is through 6 ring channels [11]. b) ETS-4 crystal grown at 448 K from mixed Na⁺/K⁺; initial pH = 12.9 [7].......................10

Figure 5: a) TEM image of an ETS-10 crystal at a magnification of 250000. Inset I: The corresponding fast Fourier transform (FFT) image, which shows that the TEM image was taken perpendicular to the (110) face of the crystal. Inset II: An enlargement of the designated area in the TEM image. Inset III: Illustration of the ETS-10 structure viewed along the [110] axis. b) TEM image of the crystal at a
magnification of 600000; circle shows the defect resulting in double-sized pore
[33]..........................................................................................................................13

Figure 6: a) Na-ETS-10 structure generated by chains of cornersharing TiO$_6$
orbitahedra (gray sticks) running along two perpendicular directions (indicated by
arrows), and which are linked by corner-sharing SiO$_4$ tetrahedra. The charge
compensating cations are located in the open spaces of the framework [34]. b) FE-
SEM images of ETS-10 crystals synthesized hydrothermally at 473 K;
5.5SiO$_2$:xNa$_2$O:yK$_2$O:1-TiO$_2$:300H$_2$O and x/y ratio of 1.0, (c) 0.6 .................15

Figure 7: Categorization of quantum structures; a) Quantum Well, b) Superlattice,
c) Quantum Wire, d) Quantum Dot [40].................................................................18

Figure 8: Semiconductor device technology trends [3].................................21

Figure 9: Differential conductance versus applied voltage in a superlattice at four
specified temperatures [46].................................................................................23

Figure 10: Initially proposed quantum wire structure; field induced edge quantum
wires [49]....................................................................................................................25
Figure 11: Cross-sectional TEM micrograph of the top part of the facet structures. GaAs (black) ridge quantum wires are formed between AlGaAs (dark gray) and AlAs (bright gray) barriers [52].................................26

Figure 12: Cross sections of GaAs/AlGaAs quantum wire heterostructure a) schematic illustration; b) dark-field transmission electron micrograph [53]........28

Figure 13: Schematic illustration of a methodology; templating against step edges [39]........................................................................................................................................29

Figure 14: The AFM images of a GaAs layer grown on a vicinal (1 1 1) B surface are shown in (a) with height mode and (b) with derivative mode, where multiatomic steps with an average period of 22 nm are seen. Their cross section at the solid lines in (a) and (b) is shown in (c). The cross-section of an n-AlGaAs/GaAs heterojunction grown on the step structure is illustrated in (d) and potential profiles at A and B in (d) are drawn in (e) [55]..................................................................................................................30

Figure 15: Wire preparation by cleaved edge overgrowth of GaAs-AlGaAs by molecular-beam epitaxy [56].................................................................32

Figure 16: Cross section of the resonant tunneling transistor containing (a) 1, (b) 2 or (c) 3 quantum wires [57]......................................................................................33
Figure 17: (a) Scanning electron microscope micrograph of a coupled quantum wire device. (b) Schematic diagram of the resonant tunneling measurement for this device [58].

Figure 18: Current-voltage characteristics of the Te clusters in the cages of zeolite A at room temperature (295 K). First, second, third, fourth and fifth measurements are represented by (a), (b), (c), (d), and (e). (f) exhibits the current after the sample was annealed under 20 V bias voltage for one hour [62].

Figure 19: Current-voltage curves measured at 295, 310, 335 and 365 K respectively [62].

Figure 20: Current-voltage curves for several gate voltages in case of (a) 1, (b) 2 or (c) 3 parallel quantum wires at 4.2 K [57].

Figure 21: Tunneling conductance diagrams are sample configurations for region III (bottom wire only), region II (both wires) and region I (top wire only) [58].

Figure 22: Current-voltage behavior of the ETS-4 crystal [63].

Figure 23: Current–voltage behavior of ETS-4 obtained from consecutive measurements; inset demonstrates Current-voltage behavior of the ETS-4 crystal obtained using the double sweep mode [63].
Figure 24: Basic concept of the RTD. The subband energy $E_o$ is approximately inversely proportional to the square of the well thickness. The peak in the I-V curve occurs when the incident electrons match the energy of the subband and the electrons resonantly tunnel from the source to the drain [65]..................44

Figure 25: Measured characteristics of a tunnel diode [66]........................................45

Figure 26: a) Natural log of transmission coefficient vs electron energy in eV for the case of double, triple and quintuple barrier [68]. b) Current and conductance characteristics of a double barrier structure of GaAs between two GaAlAs as shown in the energy diagram. The arrows indicate the observed singularities corresponding to these resonant states [46].......................................................48

Figure 27: a) Fabricated diode structure; top view of Ga-FIB scanned area. b) Current-voltage characteristics of diodes with various unimplanted areas ($L_x \times L_y$). The arrows indicate the calculated voltage positions of the discrete states to be compared with the fine structures [75].......................................................50

Figure 28: Current-voltage behavior at different temperatures for the temperatures varying between 0-15 K [17]..........................................................51

Figure 29: Experimental and theoretical source-drain currents as a function of the source-drain voltage $V_{GS}$. The vertical lines above the experimental curves indicate
the peaks corresponding to the three peaks obtained in the theory. The vertical scale applies to experiment as well as theory, with curves vertically offset for clarity. The inset shows a schematic diagram of the CEO structure in side view [76]..............53

Figure 30: Room temperature I-V characteristics of a double barrier resonant tunneling diodes fabricated with γ-Al₂O₃/epi-Si heterostructures with 2 nm thick barrier and a) 1-nm thick well, b) 2-nm thick well, c) 3-nm thick well, d) 4-nm thick well [79]...........................................................................................................................................55

Figure 31: Schematic of the device pattern obtained with the mask..................61

Figure 32: Optical image of prototype micro-device of large ETS-4.................65

Figure 33: Optical image of ETS-4 crystal on non-conducting surface with 2 probes landed on its surface.................................................................66

Figure 34: Optical image of ETS-10 crystal on non-conducting surface with 2 probes on its surface.................................................................67

Figure 35: Current-voltage performance of Si/SiO₂ wafer. Inset is the enlarged scale of the same I-V curve.................................................................70

Figure 36: Noise of the instrument obtained by measuring the current between two disconnected lines.................................................................71
Figure 37: Current-voltage characteristics of individual a) ETS-4 and b) ETS-10 crystal obtained with 2 probes landed.................................................................73

Figure 38: Current-voltage characteristics of individual ETS-4 crystal obtained with 2 probes placed, forward bias (solid line), reverse bias (dashed line).........................74

Figure 39: Current-voltage characteristics of ETS-4 crystal at different distances of probes; a) ~15µm, b) ~50µm, c) ~150µm.................................................................75

Figure 40: Current-voltage performance of individual ETS-10 crystal with increasing separation between the probes.................................................................76

Figure 41: Current-voltage performance of individual ETS-10 crystal with the probe separation of 15µ (a) and 50µ (b).................................................................77

Figure 42: Current-voltage characteristics of individual ETS-4 crystal through a dimension. Inset is framework of ETS-4 [11].........................................................79

Figure 43: Current-voltage performance of individual ETS-10 crystal through c dimension. Inset is the framework of ETS-10 structure [34] where small arrows indicate the chain directions and large arrows show the applied voltage direction..81
Figure 44: Current-voltage behavior of the ETS-4 device at temperatures of 298K (a), 180K (b), 92K (c)…………………………………………………………………...83

Figure 45: Current peaks observed on current-voltage behavior of the ETS-4 device obtained at 298 K……………………………………………………………………….85

Figure 46: Current peaks observed on current-voltage behavior of the ETS-4 device from 2 consecutive measurements at 180 K; circles 1\textsuperscript{st} run, triangles 2\textsuperscript{nd} run……...85

Figure 47: Current peak and non linear behavior observed on current-voltage behavior of the ETS-4 device obtained at 15 K for (a) forward and (b) reverse current…………………………………………………………………………………..86

Figure 48: Temperature dependency of ETS-4 device; inset - exponential fit of temperature dependency curve………………………………………………………..88

Figure 49: 54’ degree tilted SEM image of prototype micro-device of large monolithic ETS-10 utilizing FIB for etching the gold…………………….........................92
LIST OF TABLES

Table 1: Exposure and developing times for different types of photoresist........62

Table 2: Soft Baking and Post Exposure Baking durations for negative photoresist
SU-8, 2010..........................................................62
1.0 INTRODUCTION

The twentieth century will be characterized by the fact that science and technology have made substantial progress, including the establishment of quantum mechanics, the development of semiconductor devices with the invention of the transistor and the evolution of computers/telecommunications [1]. The first integrated circuit, better known as the silicon chip (7/16 by 1/16 inches in size), was invented by Bill Kilby (Texas Instruments) in 1958, as seen in Figure 1. Three years after the invention of the first silicon chip (containing only 4 transistors) it became available on the market in 1961.

![Figure 1: First integrated circuit: a sliver of germanium, with protruding wires, glued to a glass slide [2].](image)

Over the following years, complex circuits have been fabricated where feature sizes were halved almost every year [3]. Today, it is possible to squeeze 2 billion transistors on a single chip, which yields faster devices that consume less power. It has been stated that this miniaturization trend will continue until the bits are size of atoms and quantum behavior hold dominance [4]. It has also been suggested that fabrication
of novel devices by using a quantum mechanical approach will help the evolution of the future industries [5].

There has been great interest in investigating the electron transport mechanism of low dimensional systems. Quantum structures with nanoscale dimensions (<10nm) have attracted wide attention since the mid 1970’s, because of their potential in advanced device applications, such as planar superlattices field-effect transistors (FETs), quantum wire FETs, and quantum wire/quantum dot lasers [6]. Nevertheless, current techniques for preparation of low-dimensional devices present technical difficulties and concomitant costs; therefore, investigations are not plentiful, and functional devices are limited in number. Investigations of quantum wires—especially aligned quantum wire arrays—are even more rare, due to size and geometry limitations.

It has been proposed [7] that ETS-4 and ETS-10 naturally contains quantum wire arrays in their framework. Titanosilicate ETS-4 and ETS-10 are microporous crystalline materials. They contain monatomic …O-Ti-O-Ti-O… chains isolated from one another by siliceous matrix in their framework. These monatomic titania chains (~ 6.7 Å in diameter) are hypothesized to exhibit quantum confinement effects where electrons are confined in two dimensions; therefore, ETS-4 and ETS-10 crystals are suggested to have naturally occurring quantum wires in their framework. In the framework of ETS-4, titania chains run in only the b direction, while they run in both a and b directions in ETS-10.

Large ETS-4 and ETS-10 crystals have been synthesized to test their potential as quantum wire arrays [7a, 8]. Electrical transport properties of these ETS compounds need to be investigated in detail. This can be achieved by observing their current-voltage (I-V) characteristics. In order to minimize the contact issues, measurements can be carried out
by placing 2 microprobes on the surface of an individual crystal. Also, measurements
need to be performed through the dimensions orthogonal to the titania chains.
Furthermore, because electrons more easily illustrate confinement at low temperatures,
due to their lower energy separations electronic transport properties are expected to be
dominated by the wave-like behavior of these electrons. Therefore, I-V curves need to be
performed at low temperatures. Consequently, these results taken will help to provide a
basis for understanding the electron transport mechanism of naturally occurring quantum
wires in ETS-4 and ETS-10 materials.
2.0 BACKGROUND

Classically, zeolites are defined as 3 dimensional crystalline frameworks composed of interlocked tetrahedrons of silicon \([\text{SiO}_4]\) and aluminum \([\text{AlO}_4]\). Due to the crystalline nature of the framework, they form intracrystalline pores and channels of molecular dimensions [9]. These pores show regular spatial arrangements and the pore dimensions are characteristic for each particular structure type. The channels allow the easy movement of ions and molecules into and out of the structure.

There are 50 naturally occurring zeolites present in nature and more than 150 zeolite types have been obtained synthetically [10]. Natural zeolites form in nature as a result of the chemical reaction between volcanic glass and saline water in the temperature range of 300-328 K, at a typical pH of 9 and 10 [10]. At this low temperature, 50 to 50,000 years are required for nature to complete the reaction. Naturally occurring zeolites are not appropriate for commercial applications due to impurities and contamination by many different materials. Also, these long crystallization times, as well as uncontrollable size and geometry make naturally occurring zeolites difficult to use in industrial applications. On the other hand, synthetically obtained zeolites make it possible to control the crystals’ purity, size and morphology, which make them ideal for commercial applications.

The specific properties of zeolites and related crystalline microporous oxides, tetrahedrally coordinated atoms linked into a porous framework, make them useful as size and shape selective catalysis, and in gas separation applications due to their porous structure [10]. These zeo-type materials have also found applications ranging from adsorption to ion exchange, purification [11]. Currently, considerable efforts have also
been made in order to utilize zeolites in sophisticated areas such as molecular electronics, nonlinear optics, chemical sensors, optoelectronics and photochemistry [12].

Silica and alumina, which are among the most abundant mineral components, are generally used to manufacture zeolites. Recently, combination of tetrahedral and octahedral units with uniform pores and distinct molecular sieving properties has been suggested as a prospective structure in the search for new zeo-type structures [13]. Octahedrally coordinated transition metal atoms in the crystalline structure in addition to tetrahedrally coordinated silicon atoms make it possible to realize a large number of different framework types. Molybdenumphosphates or MoPO’s [14], zirconosilicates, vanadosilicates, stanosilicates [15] and titanosilicates (e.g., ETS materials) [16, 17] are some of the most remarkable structures of this prospective family.

2.1 Titanosilicates

Microporous titanosilicates are three-dimensional crystalline solids with a well defined framework containing titanium, silicon and oxygen atoms [18]. Titanium, Group IVA metal has a great tendency for octahedral coordination where it can form six coordinated octahedron, TiO$_6$. These materials have a regular crystalline framework formed by a three-dimensional combination of tetrahedral and octahedral building blocks connected with each other by shared oxygen atoms. Each TiO$_6$ octahedron in the titanosilicate structure carries a -2 charge; so, at least 2 extra-framework cations (usually Na$^+$ and K$^+$) are required to balance the charges. These compensating species, as well as water molecules or other adsorbed molecules, are located in the channels of the structure and can be replaced by others.
These mixed crystalline structures can be utilized in certain applications similar to those of conventional zeolites, in the fields of gas separation [11], different types of catalysis [19-21], membranes for pervaporation [22]; they might also have possible applications in nonlinear optics due to the semiconducting nature of titania chains [23]. These mixed tetrahedral-octahedral materials provide possibility of obtaining novel properties different from those of conventional zeolites, owing to their mixed structure.

Titanosilicate minerals can be found in nature, and have been named as Zorite. Zorite was first discovered in Siberia, Russia by Mer’kov and Nedorezova in 1973 [24]. Zorite’s two dimensional chain system and the cleavage which separates the chains [25] suggested that this material can be utilized for optoelectronic applications [26]. Polyhedral representation of zorite can be found in Figure 2.
Figure 2: Polyhedral representation of (a) the a, b plane of Zorite showing chains of Ti octahedra, and 12 membered ring channels, (b) the a, c plane showing 8 membered ring channels [17].

During the 1970’s, a variety of novel microporous titanosilicate structures were synthesized [27, 28]; however, these early synthetic titanosilicates were too dense, and their tetrahedral coordination limited their possible uses. The structure of synthetic titanosilicates has been reported by Chapman & Roe [17] in the beginning of 90’s; the synthesized materials were ~ 30 µm in length and they were highly intergrown as shown in Figure 3. They also calcined the as-synthesized material at 823 K and based on 15% of weight loss after the calcinations, they claimed that it contains interstitial water.
At about the same time (in the beginning of 90’s), Kuznicki [16] had independently revealed the structure of crystalline molecular sieve, classified as Engelhard TitanioSilicate (ETS). ETS-4 and ETS-10 represent two of the earliest discovered members of this family [13], both of which include monatomic well-defined titania chains separated from each other by a highly insulating siliceous layer.

2.1.1 Structure of Engelhard TitanioSilicate-4 (ETS-4)

One of the most interesting mixed tetrahedral-octahedral materials is the titanosilicate Engelhard TitanioSilicate-4 (ETS-4), patented in 1989 [16], whose structure was thought to be analogous to mineral zorite [25]. The difference between these two structures was the high levels of defect groups in ETS-4 and/or from the growth of
various titanosilicate phases [15]. ETS-4 contains octahedral and square-pyramidal titanium units, in addition to the tetrahedral silicate units.

Figure 4a represents the framework of ETS-4 crystal where titania atoms (green) are all connected to each other through oxygen atoms (red) resulting in the formation of …O-Ti-O-Ti-O… chains which have a diameter of ~6.7 Å (i.e., the diagonal of the TiO$_6$ octahedron). These titania chains (semiconductor, > 3eV) run in the $b$ direction and are connected to each other by silicate tetrahedra (insulator, 12eV) in the $c$ direction and by titanosilicate ‘bridging units’ in the $a$ direction [11]. Each titania chain is separated from another by highly insulating siliceous matrices (yellow). The effective pore size of ETS-4 as determined by absorption measurements is 3.7 Å, which is comparable to the pore size for small pore zeolites [13]. Consequently, this material contains monatomic well-defined -…O-Ti-O-Ti-O…- chains that are hypothesized to exhibit quantum confinement effects [7, 29]. Figure 4b is the FE-SEM image of individual ETS-4.
Figure 4: a) ETS-4 framework; octahedral titanium atoms are indicated by green. Silicon and oxygen atoms are shown in yellow and red, respectively. The a±b slice (left) shows the 12-ring opening while the a±c slice (right) shows the 8-ring opening. Pore connectivity along the $a$ direction is through 6 ring channels [11]. b) ETS-4 crystal grown at 448 K from mixed Na$^+$/$K^+$; initial pH = 12.9 [7].
In the absence of lattice defects, the chains would have the same length as the crystals: however, real crystals often have some Ti vacancies so that the chains are broken at random points [30, 31]. Utilizing high resolution electron microscopy studies [30], \([\text{TiO}_n]\) chains in ETS-10 are hypothesized to have an approximate chain length of 150 titanium atoms (i.e., the average chain length is assumed to be greater than 25 nm).

This material as other zeo-type materials contains loosely bound water that may be removed by heating without destroying the crystal structure. However, in addition, there is chemically bound water, critical to the structure. It was shown that after the loss of this bound water the structure collapses rapidly between the temperatures of 453 K and 573 K, and the crystalline material becomes completely amorphous at 773 K [15]. Ion exchange with certain type of ions has been shown to increase thermal stability; for example strontium ion exchanged ETS-4 was determined to be thermally stable up to 623 K [11].

2.1.2 Structure of Engelhard TitanoSilicate-10 (ETS-10)

Owing to its wide-pore nature and thermal stability, ETS-10 is arguably the most important mixed octahedral/tetrahedral framework microporous titanosilicate to be synthesized to date [18]. In 1994, Anderson et al [30], reported the basic structure of ETS-10 and the full description came from the same group in the following year [32]. Similar to ETS-4, ETS-10 also contains monatomic \([\text{TiO}_3]^2\) chains surrounded by a siliceous matrice with a pore size of 7.6 x 4.9 Å [7]. Again, these titania chains are broken at random points due to defects or missing atoms, which occur possibly during crystal growth; therefore titania chains do not run continuously from one end to the other.
end of the crystal. In highly crystalline ETS-10, the lengths of molecular wires are hypothesized to be greater than 25 nm [29, 30]. It should be noted that the defects in ETS-10 result in doubled-size pores, which can be seen on the transmission electron micrographs in Figure 5b.
Figure 5: a) TEM image of an ETS-10 crystal at a magnification of 250000. Inset I: The corresponding fast Fourier transform (FFT) image, which shows that the TEM image was taken perpendicular to the (110) face of the crystal. Inset II: An enlargement of the designated area in the TEM image. Inset III: Illustration of the ETS-10 structure viewed along the [110] axis. b) TEM image of the crystal at a magnification of 600000; circle shows the defect resulting in double-sized pore [33].
Different from ETS-4, as illustrated on Figure 6a, $[\text{TiO}_3]^{2-}$ molecular wires run in 2 orthogonal directions of ETS-10 crystal ($a$ and $b$) [16, 31, 33]. These titania chains, in both directions, are well insulated from each other by a silica matrix, and they never intersect. Figure 6b shows the SEM image of the large (~80x80x22µm) individual crystals. Another advantage of ETS-10 over ETS-4 is its higher thermal stability, where crystallinity of ETS-10 increases up to 623 K; some structural destruction occurs up to 753 K and the structure collapses at 923 K [15].
Figure 6: a) Na-ETS-10 structure generated by chains of cornersharing TiO$_6$ octahedra (gray sticks) running along two perpendicular directions (indicated by arrows), and which are linked by corner-sharing SiO$_4$ tetrahedra. The charge compensating cations are located in the open spaces of the framework [34]. b) FE-SEM images of ETS-10 crystals synthesized hydrothermally at 473 K; 5.5SiO$_2$:xNa$_2$O:yK$_2$O:1-TiO$_2$:300H$_2$O and x/y ratio of 1.0, (c) 0.6.
2.2 Quantum Size Effect

In the early part of the century, physical phenomena such as electron’s motion or a photon’s behavior had been encountered for which classical mechanics (Newtonian physics) could not provide an adequate explanation. This prompted the development of quantum mechanics [35]. In 1900’s, Max Planck developed a quantum theory in order to explain the observed distribution of radiation emitted by heated body. Until Planck’s explanation, all the work performed by utilizing classical electrodynamics and classical statistical mechanics resulted in open disagreement with the reported experiments [36]. De Broglie, Werner Heisenberg, Erwin Schrödinger and Paul Dirac are among the important scientists following Planck, in the establishment of quantum mechanics.

In semiconductors, the energy gap, also called the band gap, refers to the energy difference (in electron volts) between the top of the valence band and the bottom of the conduction band. The only available carriers for conduction are the electrons, which have enough thermal energy to be excited across the band gap; therefore the conductivity of an intrinsic semiconductor is strongly dependent on the band gap. Therefore the band gap is considered to be one of the most important parameters used when defining/characterizing a semiconductor. For macroscopic bulk semiconductors, the value of the energy gap determined by the material’s chemical structure is a fixed parameter, and the energy levels of both valence and conduction band are continuous. As the dimensions of the material shrink, quantum size effects can be seen and discrete energy levels are observed. Particles with at least one dimension smaller than De Broglie wavelength (~10nm), for which the spatial extent of the electronic wave function is comparable with the particle/carrier size, exhibit particle-wave duality as hypothesized by De Broglie [37].
Thus electrons, confined in such extremely small dimension, begin to respond by adjusting their energy. This phenomenon is known as the quantum size effect [38]. Peculiar properties of these materials such as band gap conductance are different from those of both molecules and bulk materials and originate mainly from the quantum confinement of electrons. The effects of quantum confinement leads to energy levels called "energy subbands", which means the carriers can only have discrete energy values. It is generally accepted that quantum confinement of electrons may provide a powerful means to control the electrical, optical, magnetic, and thermoelectric properties of a solid-state functional material [39]. Quantum mechanical tunneling is of interest because it may be utilized in structures which are far too small to operate as conventional transistors. Three different types of confinement have been identified. As illustrated in Figure 7, these 3 types of confinement are called quantum wells (2-D), quantum wires (1-D) and quantum dots (0-D).
A quantum well is a 2 dimensional system where originally free carriers are confined in one dimension; however they freely move in a thin film of macroscopic width and length. Therefore, in a quantum well system, the electrons exhibit wave-like properties in one dimension, but behave as free electrons in the other two macroscopic dimensions. These structures can be obtained by molecular beam epitaxy or chemical vapor deposition with control of the layer thickness down to monolayer. As a result, quantum wells are in wide use in diode lasers, specifically blue lasers. They are also used to make HEMTs (High Electron Mobility Transistors), which are used in low-noise...
electronics. Figure 7 b illustrates the superlattice which was first proposed by Esaki and Tsu, in which electrons were confined in 10nm thick quantum well films to form resonantly coupled states. Superlattices found their applications in infrared laser [41], photodetectors and novel light emitting devices [40].

Quantum wires, which are confined in two dimensions, can be thought as nanometer-sized cylinders that can measure up to several microns in length. This result in a 1-dimensional system called as quantum wire. As shown in Figure 7 c, carriers are confined in 2 dimensions where they exhibit wave-like properties but they can freely move along the axis of the wire, which is much larger compared to the wavelength of the particle. In condensed matter physics, a quantum wire is an electrically conducting wire, in which quantum effects are affecting the transport properties [37]. Quantum wires have been proposed to be utilized mainly in novel non-linear devices, quantum wire Field Effect Transistor (FET) and injection lasers [37].

A quantum dot is a unidirectional nanometer-sized sphere and confined in all three dimensions where the carriers exhibits wave-like properties. Each dimension of a quantum dot is smaller than the de Broglie wavelength of thermal electrons, which is

\[
\lambda = \frac{h}{p} = \frac{h}{(2meE)^{1/2}} = \frac{h}{(2me kT)^{1/2}} \approx 7.6 \text{ nm} \quad \text{Eqn 1.}
\]

where \(me\) is chosen to be equal to \(9.1\times10^{-31}\) kg. An important property of a quantum dot is its large surface to volume ratio. The consequence of this feature is that quantum dots have pronounced surface-related phenomena. They have been utilized in transistors, solar cells, LEDs, and diode lasers [37].
3.0 CRITICAL LITERATURE REVIEW

ETS-4/10 have been hypothesized to contain ordered and aligned quantum wire arrays [7a-c, 29]. Current-voltage characteristics of the material can give information about the electron transport mechanism. There have been many different methodologies to obtain quantum structures such as molecular beam epitaxy (MBE) [42], electron beam lithography, Focused Ion Beam (FIB) implantation [12] and so on. These structures need to be characterized electrically to see if they behave in a quantum confined way. Often this is performed by characterizing them as resonant tunneling devices.

3.1 Quantum Based Devices and Fabrication Methodologies

Over the last several decades, semiconductor based electronics and photonics have made remarkable progress, and have revolutionized the way our society operates [43]. Numbers of the transistors placed on an integrated circuit at a fixed cost has increased exponentially, doubling approximately every two years as suggested by Gordon Moore, in 1965 [3], and as illustrated on Figure 8. This increase in the number of transistors has yielded faster devices consuming less power. While decreasing the number of transistors, feature size has decreased to 100nm in around 2000, which is assumed to be the start of nanotechnology era. In 2008, Intel produced an integrated circuit containing 2 billion transistors on a single chip, where the feature size went down to 45nm. This miniaturization trend by 2015 is assumed to lead to feature sizes which are subject to the effects of quantum mechanics. In such small systems, electron states take on discrete set of energies (subbands). It is possible to conceive of devices that utilize transmission through these atomic-like states as a basis for quantum effect devices [45].
Fabrication of one dimensionally confined quantum wells are achieved by growing a thin layer of semiconductor sandwiched between thin layers of different semiconductor material. Crucially, the middle semiconductor layer is only a few atoms thick, in order to enable the confinement of the electrons. Quantum wells are fabricated by utilizing molecular beam epitaxy (MBE), metalorganic chemical vapor deposition (MOCVD) and the other variations of modern epitaxial growth techniques [42]. In addition to epitaxial growth techniques, electron beam lithography, Focused Ion Beam
(FIB) implantation, impurity induced interdiffusion, pattern transfer and reactive ion etching are also utilized to fabricate one dimensionally confined devices [39].

Esaki and Tsu achieved the realization of one dimensional (1D) system in 1974, for the first time, using molecular beam epitaxy [46]. Their structure composed of a thin GaAs sandwiched between two GaAlAs barriers, which was comprised of fifty alternating bi-layers of GaAs and AlAs [46]. The thickness of each GaAs layer was 45 Å and 40 Å for AlAs, resulting in 85 Å for a bi-layer. A potential barrier was provided by AlAs with a height of 0.4-0.5 eV [46]. On the other hand, neither detailed information nor the image of the device is presented by the authors. They observed oscillatory current peaks in the conductance-voltage curves (Figure 9), which were more dominant with decreasing temperature. They hypothesized the peaks occur due to overlap of the energy difference between the quantized states or bands [46]. However, their superlattice was strongly coupled, and the low-field transport occurred in the lowest minibands rather than by resonant tunneling.
Figure 9: Differential conductance versus applied voltage in a superlattice at four specified temperatures [46].

Fabrication of quantum wires, especially aligned quantum wires arrays is even harder compared to the quantum well due to size and geometry limitations. Early quantum wires with the large dimensions exhibited peculiar features of low dimensional structures only at low temperatures due to their small energy spacing of a few to several meV [40]. By shrinking the confined dimensions of the carriers to 10nm (De Broglie wavelength) or even less, energy spacing can be enlarged to tens of meV [40] and these peculiar features can be observed even at room temperatures; such as resonant tunneling peaks with smaller and broader current peaks. Moreover, examples of molecular wires are still very rare, and there is no method of synthesizing them in uniform diameters and controlled lengths [33]. Therefore, it has been strongly desired to develop new techniques,
by which 10 nm scale or even smaller dots and wires are formed, so as to enlarge the energy spacings to tens of meV [40].

Some of the main approaches used for the fabrication of quantum wires of 10nm scale can be categorized as following: the selective growth of sharp facet structures on patterned substrates, selective growth along the step edges on the freshly grown GaAs, the overgrowth of a second QW or a selectively doped n-AlGaAs layer onto the freshly exposed edge of undoped QW structures [40]. However these methodologies were not very useful in developing quantum wires arrays suitable for testing or applications. An overview of some of the various proposals and techniques used in fabrication of quantum wires can be summarized as follows.

The first proposal on quantum wire structures came from Sakaki et al. [47, 48]. They proposed the planar superlattice (P-SL) structure, in which an array of quantum wires (QWRs) or quantum dots (QDs) are periodically placed in a planar or linear geometry to control both quantum states and transport properties of one or zero dimensional electrons [47, 48]. Following this work, in 1980, Sakaki and coworkers proposed the edge quantum wire (E-QWR), where the edge surface of pre-grown QW structure is first exposed and then a barrier structure with positive charges is formed onto it to induce and confine 1D electrons along the edge plane by electrostatic fields [49]. This structure is illustrated in Figure 10. Although, these proposals were innovative and enlightening; they were theoretical and the realization of such devices with feature sizes of about 10nm took another 10 years, due to the technical difficulties in fabrication of such small size structures.
In the late 1980s, advances in the lithographic patterning on MBE-grown quantum wells enabled the fabrication of 100nm-scale quantum wires and quantum dots [50, 51]. One of the methodologies is the selective growth of sharp facet structures on patterned substrates in which selective AlAs (barrier), GaAs (wire), AlGaAs (barrier) and GaAs (cap) were deposited onto mm-scale stripe region of a (100) GaAs substrate. This methodology resulted in the formation of a very sharp roof-like structure consisting of two side facets of (111) B orientation and a very narrow top stripe of (100) orientation [52]. Figure 11 is a cross-sectional TEM micrograph of the top part of the facet structures in which GaAs (black) ridge quantum wires 9 nm thick and 18 nm wide are formed between AlGaAs (dark gray) and AlAs (bright gray) barriers. By using this facet-selective growth process, high-quality ridge QWR structures have been formed on various stripe structures defined either by etching or by a selective masking process. Using these techniques, unique properties such as the laser action of 1D electrons and holes have been demonstrated [52]. However, this methodology was not suitable for the fabrication of ordered arrays of quantum wires; this is because ordered quantum wire
array requires a certain orientation for each wire and also distance between each quantum wires to be kept uniform.

![Cross-sectional TEM micrograph](image127x413.png)

**Figure 11: Cross-sectional TEM micrograph of the top part of the facet structures.**

GaAs (black) ridge quantum wires are formed between AlGaAs (dark gray) and AlAs (bright gray) barriers [52].

In another example of this approach, the facet selective growth dominates the QWR formation process inside the V-shaped groove which would normally be defined by facet selective etching and a subsequent overgrowth [53]. This structure was grown by organometallic vapor deposition on a (100) GaAs substrate patterned with (011) oriented V grooves. The AlGaAs cladding layers grew to form a very sharp corner between two (111) crystal planes. That was followed by GaAs quantum well growing in (100) direction. These authors [53] claimed that lateral tapering in a quantum well resulted in a 2D potential well which confines the electrons and holes to a quasi-1D quantum wire.
Figure 12 exhibits the cross sections and dark field electron emission micrograph of GaAs/AlGaAs quantum wire heterostructure. The figure of the device and preparation method was not enough to convince whether this structure exhibits 1D confinement; however, these authors [53] also made an evaluation using a perturbation approach, which supported their quasi-1 dimensional confinement hypothesis. However, even if their hypothesis is correct, the facet selective growth methodology, V-groove technique is not a suitable technique for device integration of ordered arrays.
Another methodology utilized for quantum wire growth was templating against step edges on a highly oriented, pyrolytic graphite using electrodeposition [39]. Figure 13 exhibits the schematic of this methodology. In this work, two different types of material
have been studied; noble metals and electronically conductive metal oxides. These wires were found to grow at the step edges on a graphite surface. However the size of the narrowest wire they obtained was 50nm which is still too large to exhibit confinement properties.

Figure 13: Schematic illustration of a methodology; templating against step edges [39].

Sakaki et al [55] studied the structure grown by MBE on a vicinal (111) B (facet surface on (111) plane) substrate with a disorientation angle of 2° toward the [110]. Figure 14a and Figure 14b shows the atomic force microscope (AFM) images of the surface on a 0.6 mm thick GaAs layer grown at 590 °C, displayed in the height image and the derivative image mode, respectively. Potential profiles can be seen on Figure 14e. Atomic states can be clearly seen on Figure 14 and it can be claimed that device preparation is reasonable; however these authors characterize their device only by AFM images and the potential profile, but they haven’t reported any characterization regarding
electron transport properties; so conclusive statement regarding to this device can not be made.

Figure 14: The AFM images of a GaAs layer grown on a vicinal (1 1 1) B surface are shown in (a) with height mode and (b) with derivative mode, where multiatomic steps with an average period of 22 nm are seen. Their cross section at the solid lines in (a) and (b) is shown in (c). The cross-section of an n-AlGaAs/GaAs heterojunction grown on the step structure is illustrated in (d) and potential profiles at A and B in (d) are drawn in (e) [55].
Yacoby et al. [56] developed another interesting technique in which the quantum wires are obtained at the edge of a two dimensional electron gas by the overgrowth of a second QW or a selectively doped n-AlGaAs layer onto the freshly exposed edge of undoped QW structures to form edge QWR structure. Figure 15 summarizes the steps of this technique. First, doped GaAs quantum well is embedded between two thick AlGaAs layers and doped from the top as seen on Figure 15a. The quantum wire itself is fabricated by cleaving the specimen in ultrahigh vacuum and overgrowing the smooth cleavage plane with a second modulation doping sequence (Figures. 15a and 15b). This introduces electrons at the edge of the quantum well (Figure 15d) creating one or more confined edge states along the cleave. The crucial point of the methodology is to control the electrons while introduced at the edge, because this determines the properties of quantum structure. In this respect, it is necessary to develop a methodology to verify the thickness of the layer at the edge.
Figure 15: Wire preparation by cleaved edge overgrowth of GaAs-AlGaAs by molecular-beam epitaxy [56].

Etching and regrowth is another way to prepare quantum wire structure. One of the examples of this type of growth methodology came from Ertl and co-workers [57]. Their samples were fabricated by means of cleaved edge overgrowth method to provide atomically precise 1D quantum wires adjacent to 2D electron reservoir [57]. They reported nonlinear equilibrium transport measurements as a function of Fermi energy of 2 dimensional (2D) to one dimensional (1D) resonant tunneling transistors. Figure 16 illustrates the cross section of the resonant tunneling transistor containing various number of quantum wires. They were able to produce only 3 aligned quantum wires connected to 2D reservoirs and upon observation of their measurements, it can be concluded that observed I-V behavior is due to 2D-1D tunneling, instead 1D-1D tunneling. Therefore, this structure can not be considered as a successful example of aligned quantum wires.
A recent interesting structure is the one fabricated by Reno et al. [58]. They prepared a high quality parallel double quantum well heterostructure: a GaAs/AlGaAs electron bilayer with a 10 nm AlGaAs barrier between the two GaAs quantum wells grown using molecular beam epitaxy (MBE), shown in Figure 17. Electron beam lithography is used to pattern metallic gates above and below the electron layers. Figure 17 illustrates the image of the device where the dark regions are the semiconductor and the bright regions are metallic gates. This configuration allow for the study of 2D-2D, 2D-1D and 1D-1D behavior [58]. However, again, in this study, clear 1D-1D transitions were not observed. Other than 1D-1D, again in the previous work [57], 2D-1D transition was dominant. Therefore their structure can be considered as a successful example of quantum confined structure, but not a pure quantum wire system.
Figure 17: (a) Scanning electron microscope micrograph of a coupled quantum wire device. (b) Schematic diagram of the resonant tunneling measurement for this device [58].

Aligned quantum wire arrays require each quantum wire to run in a certain direction and also to be isolated from each other with an insulator. On the other hand, handling and manipulating nano-size/quantum size structures into a device stays as another challenge. Furthermore, because the band gap of quantumly confined structures is directly related to the length of the quantum wire [33], wide size distribution of the wires is not acceptable; otherwise it is not possible to predict the device performance. Techniques mentioned above are ineffective to prepare such quantum wire arrays.

3.2 Electrical Transport Properties of Quantum Confined Devices and Nanostructures

As the critical dimension of an individual device becomes smaller and smaller, carriers become confined, and the electron transport properties become an important issue to study [39]. Current-voltage behavior of a particular device may give information about
the electron transport mechanism in terms of conductivity or resistivity. Current-voltage curves are obtained, by recording the current values corresponding to gradually increasing voltage values. There has been great interest in the electron transport mechanism of low dimensional systems; however, transport mechanism of 1D system (quantum wires) has been studied much less due to the difficulties in fabrication processes. Some of the investigations on the electron transport mechanism and current-voltage performance of one dimensional systems are summarized as follow.

Wang et al. [62] studied the current-voltage (I–V) characteristics of tellurium (Te) cluster superlattice in Linde type-A (LTA) zeolite. The Na-type LTA crystals were grown by reacting sodium metasilicate with sodium aluminate, and then placed in an electric oven at 80 °C for 2-3 weeks. The resulting crystal size was about 100 µm. They reported that most of the product was polycrystalline and single crystals were selected to be tested. However, they did not report on their characterization of the product nor did they present images of the samples they obtained. The electrical measurements were performed by clamping the selected single crystal between a tungsten needle and an indium electrode. As shown on Figure 18, they observed similar current peaks with the gradually increasing voltage; but not with gradually decreasing voltage, called a current loop. Based on these observations, Wang et al [62] hypothesized that rearrangement of Te clusters due to electric field resulted in extra energy through Te – Te atom collision. The sharp decrease in the current upon increasing voltage above ~2.5V was explained with the decrease in the barrier width due the detachment of Te atoms [62]. As a result, current peaks were explained by the rearrangement of Te atoms in the cluster under an external electric field rather than the resonant tunneling transitions.
Figure 18 exhibits the current-voltage behavior of Te clusters at room temperature. As a part of this study, Wang et al [62] also performed the I-V characteristics of tellurium (Te) cluster superlattice in zeolites A at various temperatures i.e. 295, 310, 335 and 365 K. Before each measurement, the sample was in its nature state in which Te atoms were adsorbed on the inner surface of supercages. Peak to Valley Current Ratio (PVCR) of I-V curves for Te cluster superlattice were reported to be increasing upon increasing temperature (Figure 19) which supports their hypothesis of rearrangement of Te atoms rather than the resonant tunneling transition. If this current voltage peaks were due to resonant tunneling, the PVCR would be decreasing with increasing temperature due to quantum confinement of the Te atoms.

![Figure 18: Current-voltage characteristics of the Te clusters in the cages of zeolite A at room temperature (295 K). First, second, third, fourth and fifth measurements are represented by (a), (b), (c), (d), and (e). (f) exhibits the current after the sample was annealed under 20 V bias voltage for one hour [62].](image)
Ertl and co workers [57] reported nonlinear equilibrium transport measurements as a function of Fermi energy of 2D to 1D resonant tunneling transistor. Their samples were fabricated by means of cleaved edge overgrowth method to provide atomically precise 1D quantum wires adjacent to 2D electron reservoir [57]. They were able to produce only 3 aligned quantum wires connected to 2D reservoirs. All samples were characterized by recording the current voltage curves at a temperature of 4.2 K as shown in Figure 20. They observed that current peak broadens with decreasing number of parallel quantum wires [57]. On the other hand, they observed the resonant voltage shifts to lower values with the increasing number of quantum wires [57], However, in their system, considerable voltage drop occurs over the first barrier at 2D-1D transition and only a small amount at the 1D-1D transition [57], so that the decrease in the resonant
voltage may be due to the 2D-1D transition instead 1D-1D transition. They also stated that 1D-1D transition would result in increasing the bias voltage with increasing number of quantum wires [57]. However, the theory behind it is not given clearly.

Figure 20: I–V curves for several gate voltages in case of (a) 1, (b) 2 or (c) 3 parallel quantum wires at 4.2 K [57].

Bielejec et al. [58] studied tunneling in a double quantum wire device. They prepared a high quality parallel double quantum well heterostructure: a GaAs/AlGaAs electron bilayer with a 10 nm AlGaAs barrier between the two GaAs quantum wells, which were grown using molecular beam epitaxy (MBE) shown in Figure 17. Electron beam lithography was used to pattern metallic gates above and below the electron layers. They performed conductance-voltage curves in the voltage range of ±20mV. The active tunneling areas of their device consists of two small 2D-2D coupled areas joined by 1D-1D; so both 2D-2D tunneling and 1D-1D tunneling signatures were expected [58].
have observed resonance at 2.8 mV as 2D-2D tunneling signature from the pair of 1 µm × 2 µm 2D areas (Figure 21) [58]; however, the authors revealed that they have not observed a clear 1D-1D transition which would appear in the I-V curve as an additional smaller peak. While moving from region I to II, doubling of the peak tunneling conductance is observed and this is attributed to a doubling of the 2D-2D tunneling area as moving from only one wire occupied (region I) to both wires occupied (region II). The peak tunneling conductance is halved as moving from region II to region III for a similar rational [58]. The origin of the decrease in the tunneling conductance (> 0) is not clearly given in this article; the authors referred to the previous studies in which similar decrease in the tunneling conductance has been observed.

![Tunneling conductance diagrams](image)

*Figure 21: Tunneling conductance diagrams are sample configurations for region III (bottom wire only), region II (both wires) and region I (top wire only) [58].*
Yilmaz et al. [63] studied the current voltage performance of titania chains in the framework of ETS-4 material, for the first time. They performed device integration of ETS-4 by embedding it between two metal contacts utilizing photolithography, metal deposition and lift-off; they performed the measurements by placing 2 probes on metal electrodes. They observed nonlinear I-V behavior and no current peaks were observed (Figure 22). They stated that a Schottky barrier (due to Coulomb blockade) can be expected to form at the contact and suggested that Schottky barrier at the metal-semiconductor junction was dominant in the reported nonlinear I-V behavior [64]. Because their measurements were taken through the gold contact at the edges and on the top of the ETS-4 crystal, it is quite probable that these measurements were mainly affected by the large contact area. Also, Yilmaz et al. [64] performed the current-voltage curves for consecutive measurements and for double sweep mode as shown in Fig 23. They observed that the conductivity of the 3rd consecutive voltage sweep was low compared to the 1st and 2nd voltage sweeps. Also from the double sweep mode measurements (inset Figure 23), the conductivity was observed to be higher for the increasing voltage sweep compared to the decreasing voltage sweep. Based on these findings, Yilmaz and co-workers hypothesized that applied voltages result in the deformation of the conducting medium. Because ETS compounds are observed to lose structural water on heating, high current values (in the order of $\mu$A vs nA) measured [64] may have resulted in the deformation of conducting medium.
Figure 22: Current-voltage behavior of the ETS-4 crystal [63].

Figure 23: Current–voltage behavior of ETS-4 obtained from consecutive measurements; inset demonstrates current-voltage behavior of the ETS-4 crystal obtained using the double sweep mode [63].
There have been many attempts to investigate the electron transport properties of quantumly confined structures. Current-voltage (I-V) behavior is mostly used to investigate this property; resonant peaks or nonlinear behavior were the features observed in the I-V behavior. However, because of the difficulties in performing the measurements on these quantum size structures, there are few experiments, and few still detailed statements on the electron transport mechanism.

3.3 Low Dimensional Resonant Tunneling

Tunneling of a particle through a barrier is one of the most extensively studied phenomena in quantum mechanics and it has no analogy in classical mechanics. Resonant tunneling is a quantum mechanical concept that refers to tunneling in which the electron transmission coefficient through a structure is sharply peaked about certain energies [64]. For electrons with an energy corresponding approximately to the virtual resonant energy level of the quantum well, the transmission coefficient is close to unity. That is, an electron with this resonant energy can cross the double barrier without being reflected. Therefore, electrons tunnel through a sequence of classically forbidden regions sandwiching a classically allowed region [64].

Resonant tunneling devices (RTDs) have demonstrated numerous applications and potential markets including digital to analogue converters (DACs), shift registers (commonly used for conversion between serial and parallel interfaces) and ultralow power Static Random Access Memory (SRAM). The RTDs can be designed for much higher speeds than Complementary Metal–Oxide–Semiconductor (CMOS) for DACs,
typically in the speed range 10 to 100 GHz, or for much lower power than CMOS such as the SRAM technology [65].

The operation of resonant tunneling can be explained conceptually [47, 68, 69] by examining Figure 24. In equilibrium the lowest discrete energy level in the quantum confined structure lies higher than Fermi’s lake of electrons and no electrons exist in the band gap. Due to the conservation of energy, no electrons can tunnel in the discrete energy level of the quantum structure (Figure 24a). In quantum mechanics, the transmission coefficient or the tunneling probability is always less than unity; however at certain energies the transmission coefficient becomes equal to unity. If a bias voltage is applied, electron injection occurs only when one of the quantum levels of the quantum wires coincides with the conduction band energy level of the incident electrons. When the incident electrons match the energy of the subband and the electrons resonantly tunnel through the potential barrier (i.e., transmission coefficient is unity) and a current peak in the I-V curve is observed as shown in Figure 24b. With increasing applied voltages, the energy level in the quantum confined structure changes and the current decreases abruptly. Consequently, a negative differential resistance is observed. At a certain bias voltage, however, the conduction band of the emitter lies higher than the discrete level of the quantum well and the electrons can not tunnel anymore (Figure 24c).
Figure 24: Basic concept of the RTD. The subband energy $E_o$ is approximately inversely proportional to the square of the well thickness. The peak in the I-V curve occurs when the incident electrons match the energy of the subband and the electrons resonantly tunnel from the source to the drain [65].

The classically forbidden region must be thin enough so that particles can tunnel through it and classically allowed region should be thick enough to allow the existence of eigen energy states, referred to as quasi-bound states [64]. Therefore, at certain energy levels, carriers can penetrate through the sequence of classically forbidden regions. In the framework of ETS crystals, semiconductor titania chains are insulated from each other by highly insulated siliceous layers, thickness of which can be roughly approximated as the pore thickness. The effective pore size of ETS-4 and ETS-10 determined as to be 3.7 Å [13] and 7.6 x 4.9 Å [33], respectively. Thus, it can be assumed that classically forbidden
region in ETS material, which is insulating siliceous matrix (with the thickness in the order of Å), is thin enough to be considered as a candidate for resonant tunneling device. In fact there is no precise information in the literature regarding the thickness of the insulating siliceous matrices between the titania chains; so it might be roughly estimated in the order of 4-5 Å. In addition to that, highly insulating silica layer with a band gap of 12eV stands as a high barrier between titania chains. Owing to these properties, it is hypothesized that silica layer can be considered as thin and high barrier, proper for resonant tunneling devices. Classically allowed region, semiconductor titania chains (wide band gap of > 3eV) with the diameter of 6.7 Å -atomic size- can be considered to be thick enough for the existence of eigen energy states.

In particular, the tunnel diode first discovered by Esaki in 1958 involves a heavily doped (degenerate) Germanium p-n junction, in which heavy doping results in a conduction band electron states on the n-side are more or less aligned with valence band hole states on the p-side which allows the electrons tunnel through the very narrow p – n junction. With the increasing voltage applied to the system, misalignment of the valence and conduction band is observed. As a result, this tunneling manifests itself in I-V curve as a current peak as seen on Figure 25 [66]. This structure, called as Esaki diode, is the first structure exhibiting negative differential resistance. The other feature in this measurement is the temperature effect; as expected from a quantumly confined structure, conduction increases with decreasing temperature and this results in a higher PVCR value.
Through the following years, Esaki and Tsu proposed the fabrication of an artificial periodic structure consisting of alternate layers of two dissimilar semiconductors with layer thicknesses of the order of nanometers [67]. In this proposed superlattice structure tunneling occurs into quantum wells confined by the double-barrier potentials and results in a negative differential resistance in the I–V characteristics. In 1973, again Tsu and Esaki computed the transport properties for a double triple and multiple barrier [68], as seen on Figure 26a [68]. They showed negative differential resistance (NDR) in a
superlattice, for the first time. Since then, superlattices have been at the heart of semiconductor physics. During the same period (1970’s), the first realization of resonant tunneling came from the same group; resonant tunneling was observed in double barriers of semiconductors, made of GaAs-GaAlAs grown by molecular beam epitaxy [69]. Their structure composed of a thin GaAs well of 50 Å sandwiched between two Ga\textsubscript{0.3}Al\textsubscript{0.7}As barriers of 80 Å as shown inset of Figure 26 [69]. Figure 26b exhibits current – conductance characteristics of this device in the energy diagram. They claimed that the resonant manifest itself as peaks or humps in the I-V curves. This observation is correlated to their computational work in terms of current peaks; furthermore the increase in the conduction with decreasing thickness of the confined dimension is reasonable because it is expected that the better the confinement, the higher the conduction. In this respect, the temperature dependency measurements performed by Esaki and Tsu in the same work, also confirms this argument; in which they observed that the current peaks become more visible with decreasing temperature -increasing confinement. This experiment is the first demonstration of man-made quantum states formed in ultra thin semiconductor heterosturctures.
In spite of the progressive fabrication methodologies and following miniaturization trend, it took another 10 years to fabricate high quality quantum wells [1]. They exhibited fast tunneling response [70] which gave a rise to high frequency devices utilizing quantum wells. On the other hand, fabrication of superlattice using epitaxial growth methods required significant advances in material sciences, so its realization took another 3 years. In 1987, Choi and coworkers first investigated resonant tunneling in a weakly coupled superlattice, and found very regular negative conductance oscillations (conductance peaks) resulting from a periodic alignment of the two lowest quantum well
states [71]. However, detailed investigation (such as sweeping voltage at different rates and or 4 probe measurement) is necessary to confirm if these oscillations are due to the quantum confined behavior. This was followed by Sibelle et al. [72] with the fabrication of superlattice using epitaxial growth methods; that the realization of the superlattice exhibiting NDR was successfully achieved. Much theoretical and experimental work has been performed on these weakly coupled superlattices since then. Grahn et al. [73] found an increasing plateau current and a shift of the current resonances to higher electric fields in a magnetic field parallel to the superlattices layers. Kastup et al. [74] observed hysteresis between up and down sweeps of the source-drain voltage due to the charge trapped in one quantum well at the boundary between the high and the low field domain. Most of the works as mentioned above are on 2D confined quantum well and/or arrays of quantum well, superlattice; because handling and/or synthesis of 1D and 0D structures are even more difficult. For this reason, until the beginning of 90’s resonant tunneling of 1D or 0D confined structures had not been investigated to any depth.

Tarucha and coworkers were the first to study the effect of resonant tunneling on 1D-0D structures (quantum wire and quantum dots) [75]. Their device was a conventional resonant tunneling diode, which they confined laterally by gallium focused ion-beam implantation. First, an initial epitaxial structure was grown by molecular beam epitaxy, depositing GaAs and AlGaAs layers. Then Ga-FIB was scanned onto the epitaxial structure leaving a single space of unimplanted area which is utilized for the measurements as an implementation area. They observed a series of resonant tunneling current peaks corresponding to the one dimensional levels superimposed on the ground state confined by the heterojunction. Figure 27 illustrates the current voltage behavior of
diodes with various unimplanted areas, in which current peak is observed at 0.4V with a 9nA max current. Based on these measurements performed by Tarucha et al. [75] it can be seen that the PVCR decreases with decreasing area and oscillatory behavior in the I-V curve becomes to be visible with the decreasing implementation area. Also the oscillations become visible with decreasing implementation area at low temperature of 4K. This is expected because electrons can confine well at low temperatures due to their low energy separations.

![Diode Structure and I-V Characteristics](image)

**Figure 27:** a) Fabricated diode structure; top view of Ga-FIB scanned area. b) Current-voltage characteristics of diodes with various unimplanted areas ($L_x \times L_y$). The arrows indicate the calculated voltage positions of the discrete states to be compared with the fine structures [75].
In 1990, Weisshaar and coworkers [76] theoretically studied the negative differential resistance in a resonant quantum wire structure. They stated that the occurrence of the resonant peak can only be attributed to electron tunneling in the two narrow constrictions, similar to that in RTD's. The influence of increasing temperature on the current-voltage characteristic of the quantum waveguide structure is indicated in Figure 28, in which PVCR is observed to be increasing with the decreasing temperature. With the decreasing temperature, carriers can confine better and their wave-like properties begin to be dominant so that this increase in conduction (or PVCR) is expected. Nevertheless, in their work, the shift in the resonant voltage is not so clear; therefore conclusive statement cannot be made.

![Figure 28: Current-voltage behavior at different temperatures for the temperatures varying between 0-15 K [76].](image)

Dignam et al. [77] investigated 2D-1D-2D tunneling in a sample prepared by cleaved-edge overgrowth. GaAs/AlGaAs material system was fabricated by Molecular Beam Epitaxy (MBE) with an internal in situ sample cleavage. Their device was a single
quantum wire of 5nm width with the barriers of 6 nm and 7.5 nm AlGaAs on each site (see inset, Figure 29). This structure can be considered as similar to that of ETS framework in terms of 2D confinement; however, ETS crystal has billions of wires with 1 order of magnitude smaller dimensions. For the single wire, Dignam et al. showed that tunneling proceeds from the edge of a source through the bound states of the quantum wire into the edge of a drain. They found resonance peaks in the tunneling current, which they attribute to a resonance between the edges bound states in the 2D system and the first three bound states in the wire [77].
Figure 29: Experimental and theoretical source-drain currents as a function of the source-drain voltage $V_{GS}$. The vertical lines above the experimental curves indicate the peaks corresponding to the three peaks obtained in the theory. The vertical scale applies to experiment as well as theory, with curves vertically offset for clarity. The inset shows a schematic diagram of the CEO structure in side view [77].

Another interesting example came from Mosammat et al. [80]. They performed current–voltage characteristics of the Double Barrier Resonant Tunneling Devices (DBRTDs) in order to determine the relationships between the peak-to-valley current ratio (PVCR) and the quantum well thicknesses and also between the peak current density and the barrier thickness for the maximum PVCR at room temperature [80].
Epitaxial Al₂O₃ films were fabricated on n-type Si (111) substrates. The epitaxial Al₂O₃ films were formed then an epitaxial Al₂O₃ film was grown by mixed source MBE. To perform the electrical measurements, electrodes of different areas were patterned by photolithography. Al electrodes were deposited on the top of the Al₂O₃ film and at the bottom of the Si substrate, using a conventional evaporation system. They attributed the current peaks to the resonance tunneling through the quantum well, and they determined that good performance is obtained for the device with a quantum well (epi-Si) thickness of 2nm and a barrier (γ-Al₂O₃) thickness of 2 nm. In addition, they observed a very high PVCR of 26 for the device with a quantum well thickness of 3nm (Figure 30). The striking part of this study is that resonance peaks were observed at room temperature with a very high PVCR of 26; because, in most of the previous works, current jumps were observed only at low temperatures; so practical application was not possible. However, in the work of Mosammat et al. [80], current peaks (resonant tunneling) were observed even at room temperature making possible its application to practical devices.
Figure 30: Room temperature I-V characteristics of a double barrier resonant tunneling diodes fabricated with $\gamma$-Al$_2$O$_3$/epi-Si heterostructures with 2 nm thick barrier and a) 1-nm thick well, b) 2-nm thick well, c) 3-nm thick well, d) 4-nm thick well [80].

Studies on quantum structures have been continuing since 1950’s. Many approaches including growth with Molecular Beam Epitaxy (MBE), cleave edge, overgrowth techniques have been studied in order to be able to find a convenient way to fabricate quantum structures. There have been some experimental studies on the electrical transport characteristics of these structures, but mostly theoretical studies, due to the difficulty in handling these extremely small structures. In our work, we utilized the ETS crystals containing ordered aligned semiconductor chains which have been hypothesized as quantum wires [7, 29].
4.0 EXPERIMENTAL METHODOLOGY

Current-voltage curves of ETS crystals were obtained for the single ETS-4 crystal at various temperatures changing in the range of 15-273 K, by performing device integration. The temperature dependency of large ETS-4 was investigated. Also, these curves were obtained at room temperatures for several ETS-4 and ETS-10 crystals, by positioning two microprobes on the top of the individual crystals. Current-voltage behavior of ETS-10 was investigated at room temperature only using the two probe method.

4.1 Sample Preparation

Samples were mainly prepared in two ways in order to test the different properties of the crystals. First, device integration was performed in order to investigate the electrical behavior of ETS-4 crystal. Then, another sample was prepared in order to test the electrical properties of chains by positioning the probes with the tip diameter of 1.0 μm directly on individual crystal.

4.1.1 Device Integration of ETS-4

Current-voltage curves of ETS-4 crystals were obtained for the single crystal, containing titania chains in the order of billions, by performing device integration at both room temperature and lower temperatures. Device integration of ETS-4 crystals was performed utilizing photolithography based microfabrication methodology. Large individual ETS-4 crystals were embedded between two gold electrodes. A new microfabrication methodology was introduced in order to improve the previous
methodology developed by Yilmaz et al. [63]. The main steps of this new methodology are substrate preparation, attachment of the crystal onto substrate, special mask design, photolithography with negative photoresist, metal deposition followed by another photolithography and metal etching. This methodology makes the device integration of ETS-4 crystal possible and repeatable.

4.1.1.1 Substrate Preparation

Substrate preparation was performed in two main steps; substrate cleaning and dehydration of substrate. Substrate preparation is one of the crucial steps in the development and microfabrication of semiconductor devices in terms of eliminating contamination from the surface and obtaining uniform coating.

Substrate cleaning was performed by using two different methodologies: solvent cleaning and RCA cleaning. The latter was performed when solvent cleaning is not enough to clean the contamination from the surface of the wafer.

4.1.1.1.1 Solvent Cleaning

Initially, Si/SiO$_2$ wafer was cut into smaller square pieces with the dimensions of 1 cm x 1 cm. Then, substrate preparation was performed to improve the adhesion of the photoresist to the substrate. First step of the preparation was substrate cleaning in order to remove the contamination, which can take the form of particulates or films and cause defects in the photoresist pattern and poor adhesion. Substrate cleaning was performed by ultrasoncating the wafer 5 minutes in an acetone (cleanroom grade, Air Products) bath, then soaking it in a methanol (cleanroom grade, Air Products) bath followed by rinsing
with isopropanol (2-propanol, clean room grade, Air Products). The Si/SiO₂ wafer was then blow dried with pressurized N₂ gas (>99%).

4.1.1.2 RCA cleaning

RCA cleaning, one of the most effective ways of wafer cleaning, is a procedure for removing organic residue and films from wafers. The basic procedure of RCA Cleaning was first developed by Werner Kern in 1965 while working for Radio Corporation of America (RCA) and it includes three basic steps: organic cleaning, oxide stripping and ionic cleaning.

First, organic cleaning was performed to remove the insoluble organic contaminants. It is performed by soaking the wafer in a 5:1:1 H₂O:H₂O₂:NH₄OH solution at 348 K for 15 minutes. When finished, the wafer was transferred to a container with overflowing deionized water (18 MΩ•cm) from a tap to rinse. Then, in order to remove any thin silicon dioxide layer where metallic contaminants may accumulated as a result of the organic cleaning, oxide stripping was performed by soaking the wafer in a diluted 50:1 H₂O:HF solution at room temperature for 15 seconds. It is important to keep the wafers in the solution no more than 30 seconds, because this could cause a new oxide layer to form. Ionic and heavy metal atomic contaminants were then removed by using a solution of 6:1:1 H₂O:H₂O₂: HCl. The wafer was soaked into the solution and kept at 348 K for 15 minutes. When finished, the wafer was transferred to a container with overflowing deionized water (18 MΩ•cm) from a tap to rinse. Then it was blow dried with pressurized N₂ gas (>99%).
4.1.1.3 Dehydration of the wafer

Solvent cleaning was followed by dehydration to remove water from the substrate. To dehydrate the substrate, Si/SiO\(_2\) wafer was kept at 473 K for 5 minutes on a hot plate in ambient air and cooled down to room temperature in ambient air.

4.1.1.2 Crystal Attachment

Prior to crystal attachment, in order to promote adhesion, the wafer surface was spin coated using an adhesion promoter hexamethyldisilizane (HMDS, ultra pure grade, HP Microprime, ShinEtsu-MicroSi) primer layer which react chemically with surface silanol and replace the -OH group with an organic functional group that, unlike the hydroxyl group, offers good adhesion to photoresist. An HMDS coating was performed at a speed of 2000 rpm for 30 seconds with a ramp time of 5 seconds. Then, the wafer was coated with positive photoresist Microposit PR S 1805 (Rohm and Haas) which made the ETS-4 crystals sink onto the wafer and helps them to attach to the surface. The a two-step photoresist coating was performed: first, in order to disperse the photoresist onto the wafer, a slow spin was performed at a speed of 500 rpm for 5 seconds with a ramp time of 5 seconds. This spin was followed by a fast spin which was at 4000 rpm for 40 seconds with a ramp time of 1 second. Soft baking was performed at 388 K for 2 minutes on a hot plate in ambient air in order to evaporate the solvents in the photoresist. After soft baking, the wafer was cooled down to room temperature in ambient air.

As a next step, previously synthesized large [7a], monolithic, ETS-4 crystals were suspended in hexamethyldisilizane (HMDS) and sparsely dispersed on the wafer via spin coating. The importance of dispersing the crystals “sparsely” is to make the integration of
a “single” crystal possible. Once again, a two-step process was performed; slow spin at a speed of 500 rpm for 5 seconds with a ramp time of 5 seconds followed by fast spin at 4000 rpm for 40 seconds with a ramp time of 1 second. Positive photoresist coating itself was not sufficient to hold the crystals on the wafer surface. In order to have full attachment, gradual hard baking was performed starting at 348 K on a hot plate in ambient air. After 1 minute, the temperature was increased gradually with the ramp of 20 K/min for 5 minutes and kept at 448 K for 4 minutes. It has previously been determined that ETS-4 framework is expected to be thermally stable up to 473 K, and thermal deformation of its framework is expected to begin at higher temperatures than 473 K [11]. Because the maximum temperature in gradual hard baking process was kept below that temperature, it can be deduced that this process does not damage the ETS-4 framework. Following the gradual hard baking, the wafer was again cooled down to room temperature at ambient air.

4.1.1.3 Photolithography

In order to perform photolithography, wafers with crystals on them were coated with negative photoresist, SU-8 2010 (MicroChem). Initially, a two-step photoresist coating was performed: first, slow spin was performed at a speed of 500 rpm for 5 seconds with a ramp time of 5 seconds in order to disperse the photoresist on the wafer surface. This was followed by a fast spin which was at 3000 rpm for 30 seconds with a ramp time of 8 second. At this point, it is important to disperse the negative photoresist with a slower ramp than that of positive photoresist, due to the higher density of negative photoresist, SU-8. After the resist has been applied to the substrate, it was soft baked at
388 K for 2 min on a level hot plate in order to evaporate the solvent and densify the film. A two-step contact hot plate process was performed: first, the substrate was kept at 338 K for 1 minute and then taken to another hot plate at 368 K for 2 minutes. In order to prevent the cracks at the surface of the wafer due to SU-8 coating, slow cooling down was performed in air by setting the hot plate temperature at room temperature, 293 K and leaving the sample on the hot plate till room 293 K was reached. In order to develop the device design UV exposure was next performed. In order to perform UV exposure, a special mask which allows the openings of 30 µm, 50 µm and 70 µm was designed to form the device pattern. Schematic of this device pattern is illustrated in Figure 31.

![Figure 31: Schematic of the device pattern obtained with the mask.](image)

Utilizing this device pattern, UV exposure was performed with the intensity of 65 Wm/cm² and wavelength of 405 nm for a set of three 8 second exposures, 24 seconds in total. Exposure and developing times used for different photoresists can be seen on Table 1. Alignment of the mask around single ETS-4 crystal was performed by mask aligner system (AB-M Inc). Following the UV-exposure, a two-step post exposure bake was
performed: first, the substrate was kept at 338 K for 1 minute and then taken to another hot plate at 368 K for 2.5 minutes. For slow cooling, again the sample was left on the hot plate by decreasing its temperature to 298 K (RT). Both soft baking and gradual hard baking processes were performed on level hot plate in an ambient air. Summary of the soft baking and post exposure baking durations for negative photoresist SU-8, 2010 is presented on Table 2. Then, in order to remove the unexposed parts, developing was performed using Propylene Glycol Methyl Ether Acetate (PGMEA, Baker BTS-220). Sample was gently shaken in a container filled with PGMEA for 3 minutes and then rinsed with isopropanol (2-propanol, clean room grade, Air Products) for 30 seconds.

Table 1: Exposure and developing times for different types of photoresist.

<table>
<thead>
<tr>
<th>Photoresist Type</th>
<th>Exposure Time (s)</th>
<th>Developer</th>
<th>Developing time (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SU-8 2010</td>
<td>24</td>
<td>PGMEA</td>
<td>3</td>
</tr>
<tr>
<td>1813</td>
<td>20</td>
<td>CD-30</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Table2 : Soft Baking and Post Exposure Baking durations for negative photoresist SU-8, 2010.

<table>
<thead>
<tr>
<th>Hot Plate Temperature</th>
<th>338 K</th>
<th>368 K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft Baking Duration (min)</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Post Exposure Baking Duration (min)</td>
<td>1</td>
<td>2.5</td>
</tr>
</tbody>
</table>
4.1.1.4 Metal Deposition

A thermal evaporator (Sharon) was used for metal deposition of chromium and gold. First, a thin layer of chromium was deposited on the sample by placing the chromium source with 0° angle with the sample; thus, it can be predicted that there was no chromium at the edges of the ETS-4 crystal. The rate of Cr deposition was set at 0.5 Å/s and applied for 200s resulting in 10nm film thickness of Cr. Then, gold deposition was carried out by placing two gold sources (Alfa Aesar, 99.99%) at both ends of the source holders in the thermal evaporator; thus, angled gold deposition was achieved. The average angle between the metal source and the sample was 20°, the rate of Au deposition was set at 0.9 Å/s and a film thickness of Au deposited from each side was 70 nm, and the resulting film thickness was 140 nm.

4.1.1.5 Metal Etching

An additional photolithography step was carried out in order to keep the gold on the pattern during gold & chromium etching process. Positive photoresist of Microposit PR S 1813 (Rohm and Haas) was dispersed on the crystal utilizing two-step photoresist coating. First, in order to disperse the photoresist homogenously onto the wafer, slow spin was performed at a speed of 500 rpm for 5 seconds with a ramp time of 5 seconds. This spin was followed by a fast spin which was at 4000 rpm for 40 seconds with a ramp time of 1 second. Soft baking was performed at 388 K for 2 minutes on a hot plate in ambient air in order to evaporate the solvents in the photoresist. After soft baking, the wafer was cooled to room temperature in ambient air. The same mask used in the first photolithography with negative photoresist was utilized to match the previous pattern and
the alignment was performed using mask aligner (AB-M Inc). After matching the previous device pattern with mask’s pattern, UV exposure was performed with the intensity of 65 Wm/cm² and wavelength of 405 nm for set of two 10 seconds, 20 seconds in total. Development was then performed to remove the exposed parts after UV-exposure. The sample was then gently shaken in a container filled with microposit developer CD-30 (Rohm and Haas) for 90 seconds, and rinsed with deionized water (18 MΩ•cm) for 60 seconds; so that the positive photoresist was able to be placed on the pattern to hold the gold during etching.

In order to remove the gold and chromium outside the device pattern, etching was performed. First, gold etching was carried out by diluting 20 ml of Gold etchants (TFA, Transene Company, Inc) with 40 ml of deionized water (18 MΩ•cm) and then sample was gently shaken in the solution for 50 seconds followed by rinsing with deionized water for 30 seconds. Chromium etching was performed by diluting 20 ml of chromium etcher with 40 ml of deionized water (18 MΩ•cm). Again the sample was shaken in the container filled with the diluted solution for 30 seconds and then rinsing with deionized water (18 MΩ•cm) for 20 seconds.

4.1.1.6 Final Cleaning

As a last step, in order to remove the photoresist residue on the surface of the sample, especially on the device pattern, the sample was gently placed in a static acetone bath for 15 seconds and then methanol bath for 15 seconds followed by isopropyl alcohol for 10 seconds and blow dried with pressurized N₂ gas (>99%). Removing the photoresist residue from the pattern surface helps the contacting with the gold during the electrical
measurements; otherwise, the photoresist may prevent the contacting probes from directly touching the gold pattern. A typical device is illustrated in Figure 32. A detailed step by step procedure is presented in Appendix A.

![Image](image1.png)

**Figure 32: Optical image of prototype micro-device of large ETS-4.**

### 4.1.2 Samples for Probes on Crystal Surface

Two microprobes (Signatone), 1µm in diameter were landed on the top of the crystal a distance of 10-15µm away from each other. Figure 33 and 34 exhibits optical images of ETS-4 and ETS-10 with these two probes positioned on ETS-4 and ETS-10, respectively.

The 2cm x 2cm Si/SiO$_2$ wafer was prepared as described in section 4.1.1.1. Then, crystal attachment was achieved -as explained in 4.1.1.2- by coating with
HMDS primer and positive photoresist of 1813 which melts during Gradual Hard Baking (GHB) and makes the crystals attached.

Figure 33: Optical image of ETS-4 crystal on non-conducting surface with 2 probes landed on its surface.
Current-voltage performance was also determined for the direction where there is no titania chains; $a$ dimension for ETS-4 and $c$ dimension for ETS-10. This means that voltage is applied only across the siliceous matrices SiO$_4$. In order to do that, first of all, 2cm x 2cm Si/SiO$_2$ wafer was prepared as described in 4.1.1.1. Right after cleaning and dehydration of the wafer, chromium and gold layers were deposited using thermal evaporation as described in 4.1.1.4. Large ETS crystals were sparsely dispersed on gold coated wafer using a spatula.
4.2 Semiconductor Parameter Analysis of ETS-4 and ETS-10

Current-voltage (I-V) characteristics were obtained using Micromanipulator Model 6000 Electrical Probe Station utilizing Signatone SE-10T tip which has a 1µm diameter tip. Sample was placed on a grounded sample holder. Then, two probes were gently placed on the top of a large individual crystal. Distance between the two probes was kept as ~15, 50 and 150 µm for different measurements. For non-chain measurements, crystals were dispersed on gold covered substrate. Then, one probe is placed on gold covered substrate and the other one is placed on the top of the crystal; so that, current flow through dimension $a$ of ETS-4 and dimension $c$ of ETS-10 was obtained. Data was acquired with a step of 0.5V/s and 5s of hold time at each voltage.

For low temperature measurements, crystal embedded between 2 gold electrodes (see Fig 32) was utilized and wire bonding was used to attach the device to the sample holder. After placing the sample holder in the vacuum chamber, liquid Nitrogen was used for cooling down the chamber for the measurements down to 92 K and liquid Helium was used for the measurements down to 15 K. Current-voltage measurements were performed at temperatures varying in the range of 15-298 K at various voltages ranging up to 15 volts with a step of 0.02V was applied.
5.0 RESULTS AND DISCUSSION

Current-voltage performance of crystalline titanosilicate ETS-4 and ETS-10 were investigated. I-V performance was investigated at room temperature for both ETS-4 and ETS-10 crystal, by positioning microprobes on the top of the individual crystal. Current-voltage curves were performed for ETS-4 crystals at various temperatures in the range of 15-298 K, by performing device integration of single monolithic crystal. Current-voltage behavior of ETS-10 was investigated at room temperature only. It was hypothesized that electron transport occurs through monatomic discrete titania chains and the current peak due to resonant tunneling between the titania chains is the main feature of the current-voltage behavior of ETS material.

5.1 Room temperature current-voltage characterization by placing microprobes

Current-voltage (I-V) characteristics were performed by positioning microprobes on the surface of an individual crystal. The measurements were obtained only at room temperature due to the lack of a vacuum chamber around the sample holder of the probe station.

Before performing the measurement, the tool was tested on Si/SiO$_2$ wafer to ensure little or no contribution of the substrate Si/SiO$_2$ to the conductance. As shown in Figure 35, which illustrates the I-V characteristics of Si/SiO$_2$ wafer, conductance of wafer was 3 orders of magnitude less than that of the measured current on the crystal samples. The inset exhibits the same I-V curve on enlarged scale; therefore, it was assumed that wafer has no significant contribution to the conductance.
Figure 35: Current-voltage performance of Si/SiO₂ wafer. Inset is the enlarged scale of the same I-V curve.

The instrumentation noise is specified at 50-fA by the manufacturer Micromanupulator. It was experimentally determined as on the order of 5-10 pA based on the measurement of 2 disconnected lines, as illustrated on Figure 36. Therefore, it was concluded that noise of the instrument made no contribution to the conductance of the crystal.
Figure 36: Noise of the instrument obtained by measuring the current between two disconnected lines.

Room temperature I-V curves of individual ETS-4 and ETS-10 were obtained over the potential voltage range of ±20V voltages, with 15µm separation of the probes. Figure 37 shows the room temperature I-V performance of crystalline ETS-4 and ETS-10. When the potential of -20V is applied with a hold time of 5s, current value sharply decreased and then stayed at lower values (in the order of pA) as potential is increased to 0V.

While increasing the potential from 0 to 20V, current jump was observed followed by negative differential resistance (NDR) for voltages higher than 3V. Resonant voltages were located at 5±0.5V for ETS-4 and 7±0.5V for ETS-10. This characteristic in the I-V curve can be explained with resonant tunneling phenomenon which was first established by Esaki and Tsu [47, 68, 69]. When the electric field is applied, the lowest energy levels of the titania chains coincides with the Fermi energy of
the electrons injected to the crystal, and the thin insulating SiO$_4$ layer between the titania chains allows the current flowing through; therefore, the sharp peak was observed in the I-V curve at a specific voltage, as it can be followed in Figure 24 which represents the general resonant tunneling mechanism. While increasing the voltage gradually, the top of the quantum level of titania chains’ lines up with the emitter Fermi energy where the top of the peak is observed. After this point, current decreases suddenly, so negative differential resistance is observed. Finally, the top of the energy level of the titania chains match with the emitter conduction band and insulating layer of SiO$_4$ doesn’t allow the current flow anymore. These phenomena [47, 68, 69] taken together result in the observed current jump in the I-V curve of the ETS material. Peak-to-valley current ratio (PVCR) was determined for ETS-4 and ETS-10 with the 15µ separation of the probes on as 3.4 and 5.4, respectively. These measurements were performed on at least 10 different crystals and the resonance peaks were located at the similar values with the error of ±0.5V. The difference in the PVCR can be explained with the titania chains lying parallel between 2 probes in ETS-10. Different from ETS-4, the titania chains run in 2 dimension in ETS-10 and when 2 probes were placed on the surface of the individual ETS-10, parallel titania chains also contribute conduction differently from ETS-4. This may result in the higher PVCR of ETS-10 crystal.

In the previous report by Yilmaz et al. [63], no current peaks were observed and it was stated that a Schottky barrier (due to Coulomb blockade) can be expected to form at the contact. In the recent work, contact area is decreased by utilizing the tungsten probes with the tip diameter of 1µm; Schottky barrier at the contact is still expected due to the
difference in the conductivities of tungsten and semiconductor titania chains; however it can be suggested that I-V behavior is not dominated by Schottky barrier.

![Current-voltage characteristics of individual a) ETS-4 and b) ETS-10 crystal obtained with 2 probes placed.](image)

Figure 37: Current-voltage characteristics of individual a) ETS-4 and b) ETS-10 crystal obtained with 2 probes placed.

When the voltage was dropped from +30 V to 0V, again similar behavior was observed (Figure 38); that is, no current peak was observed with decreasing voltage. Furthermore, while following this measurement (from 0 to -30V), mirror image of current jump is observed upon increasing the potential. At present it is not clear why there is no resonance while decreasing the potential; however, it can be thought that the system reaches saturation with decreasing potential, and then it becomes conducting with the
increasing potential. ETS material also contains cations (Na\(^+\) and K\(^+\)) other than the titania chains [33] and these cations balance the charges in the material or cations might be immigrating from one side to the other side with decreasing potential and then this allows to the system to conduct resonantly while increasing the potential. As a result, cations might have contributed to the observed peaks with the increasing potential.

![Current-voltage characteristics of individual ETS-4 crystal obtained with 2 probes placed, forward bias (solid line), reverse bias (dashed line).](image)

**Figure 38:** Current-voltage characteristics of individual ETS-4 crystal obtained with 2 probes placed, forward bias (solid line), reverse bias (dashed line).

Figure 39 shows the I-V curves performed on ETS-4 by increasing the distance between 2 probes. While separation goes from 15 µm to 150 µm, PVCR was observed to diminish and the peaks to broaden with increasing potential. These experiments were
performed on 7 different crystals and similar behavior was observed for each of them, that is diminishing current peak with increasing distance between 2 probes. This decrease in the PVCR might be expected; because, by enlarging the separation between probes, conduction along titania chains through defects becomes less effective due to the decreasing electric field.

Figure 39: Current-voltage characteristics of ETS-4 crystal at different distances of probes; a) ~15µm, b) ~50µm, c) ~150µm.

Figure 40 illustrates the I-V performance of ETS-10 with the increasing separation of the probes. Because ETS-10 crystals were smaller than ETS-4, measurements were performed with only two different separation of ~15 µm to 50 µm.
While increasing the separation between the probes, PVCR was observed to increase from 5.4 to 7. While increasing the separation between probes, more titania chains-siliceous matrix parallel to each other but orthogonal to the probes’ locations begin to be involved in the conduction; owing to the titania chains running in 2 directions. Such increase in the number of titania chains between two probes may results in the higher conduction with a higher PVCR. The observation of higher current with increasing number of parallel titania chains may also support the hypothesis that there is conduction between the chains through the thin SiO$_4$ layers.

Figure 40: Current-voltage performance of individual ETS-10 crystal with the probe separation of 15µ (a) and 50µ (b).
Current-voltage performance was also performed on the different direction of individual ETS-10 crystal. First, 2 microprobes were positioned on the crystal, then one of the probes kept stable and the other moved to an orthogonal position relative to the first. The distance was kept the same as the first one (~15µ). As seen on Figure 41, there is no significant difference between the two measurements. This behavior can be expected because by relocating the probes orthogonal to each other on ETS-10 surface, nothing should be changed structurally due to the titania chains running in the \(a\) and \(b\) orthogonal directions.

![Figure 41: Current-voltage performance of ETS-10 while 2 probes are vertical (solid lines), parallel (dashed lines).](image)
In addition to those findings, I-V performance was determined through the dimension where the …O-Ti-O-Ti-O… chains are parallel to each other and separated by siliceous matrices (a dimension for ETS-4 and c dimension for ETS-10). In these dimension for each respective crystal, titania chains are parallel to each other, with an insulating siliceous layer between. Figure 42 shows only the ETS-4 I-V performance. In these measurements, current values were so small (in the order of pA) up to resonance voltage and no nonlinear behavior of I-V curve was observed. Then, a current peak was observed with a PVCR of 9 (higher than observed for the b direction), and the voltage threshold for resonant tunneling also shifted to a relatively higher value of 9.5V (with the measurements taken on the top of the crystal). First of all, conduction through the dimension where titania chains are parallel to each other and separated by siliceous matrices, supports the hypothesis of tunneling of the carriers through the siliceous matrices. Secondly, Tarucha et al [75] and Ertl et al. [57] observed that high PVCR (sharper peak) is directly proportional to the increasing implementation area (titania chain – siliceous matrix layers). The measurement through a direction of ETS-4 gives a higher PVCR with the increasing implementation area; this also supports the hypothesis of resonant tunneling through the siliceous matrices.

Furthermore, existence of nonlinear I-V behavior at low voltages for the measurements through chain direction but not through non-chain direction might reveal that electron transport occurs through the titania chains. Because titania chains are discrete with defects [33], it can also be hypothesized that tunneling occurs between the broken chains via tunneling and device performance is preserved. Cations (Na\(^+\) and K\(^+\))
in the framework of ETS material fundamentally lower the barrier between broken titania chains and therefore increase the probability of tunneling through discrete chains.

![Figure 42: Current-voltage characteristics of individual ETS-4 crystal through a dimension. Inset is framework of ETS-4 [11].](image)

Similar I-V performance was also obtained for individual ETS-10 crystal in which titania chains run in 2 dimensions without crossing each other. Orthogonal $c$ dimension of ETS-10 is ~20µm while it is only ~10µm for an individual ETS-4 crystal. Similar to ETS-4, again the current peak was observed with a much higher intensity compared to the measurements performed with 2 probes placed on the top of the crystal. PVCR was determined as 10.5, which was observed to be much higher compared to ETS-4. This can
be explained with the increasing number of layers (titania chains – siliceous matrices) involved in the resonance. Resonance voltage has been observed to be shifted to higher values for the measurements performed through non chain directions for both ETS-4 and ETS-10. Ertl et al. also reported the current-voltage curves of different number of quantum wires and adjoining the 2D electron reservoirs [57]. In their study, current peak broadens with the decreasing number of parallel quantum wires, which is consistent with our reported observation; because while taking the measurement through non chain direction of ETS material, voltage is applied through all the titania chains siliceous layer running from top to the bottom of the crystal. Ertl and coworkers also suggested that, in case of 1D transition, resonance voltage would increase with increasing implementation area (titania chains - silceous layer).
Figure 43: Current-voltage performance of ETS-10 crystal through the vertical dimension. Inset is the framework of ETS-10 structure [34] where small arrows indicate the chain directions and large arrows show the applied voltage direction.

5.2 Low temperature Current-voltage characterization of ETS-4 device

Current-voltage curves of titaniosilicate ETS-4 were obtained at various temperatures varying in the range of 92-298 K, by performing the device integration of individual ETS-4. Device integration should be performed in order to be able to perform the low temperature measurements, because low temperature measurements have to be performed in a vacuum chamber where it is not possible to land the probes on the surface. In order to eliminate the contact issues, which might affect the resulted I-V behavior; new device integration methodology was performed utilizing gold etching instead of the
typical lift off step, in order to eliminate the residue left at the edges of the crystal. Figure 44 shows the I-V performance of the individual ETS-4 crystal at temperatures of 298, 180 and 92 K. These I-V curves exhibited all smooth and nonlinear behavior at each temperature up to specific voltages. As seen, at room temperature, current increased nonlinearly up to 2V; with the decrease in the temperature from 180 K to 92 K, it stayed smooth nonlinear up to ~7V and 10V, respectively. Up to these values of voltages, lower current values were observed at lower temperatures, resulting in higher resistance at lower temperatures. This behavior of I-V curves is consistent with both semiconductor behaviors, where current increases nonlinearly with gradually increasing voltage; and tunneling effects where the probability of tunneling decreases with the decreasing temperature.
With the voltages higher than these values, current became increasing steeply with gradually increasing potential, similar to the room temperature measurements. Again current jump followed by negative differential resistance was observed. The current values were much higher compared to that of room temperature; so that current peaks were observed with a much higher PVCR, as expected. This is because carriers can confine better at low temperatures, and it is expected to see current peaks with higher PVCR at lower temperatures. Sakaki [40] stated that early quantum wires with the dimensions of 100nm exhibited resonance peaks only at low temperatures due to their
small energy spacing of few to several meV. By shrinking the confined dimensions of the carriers to 10nm or even less (it is less than 1 nm for the titania atoms in ETS material), energy spacing can be enlarged to tens of meV [40] and resonance peaks with higher current values can be observed. Weisshaar et al. [76] reported a calculated current–voltage performance of resonant quantum wire structure in which similar increase in PVCR with the decreasing temperature was predicted to occur. Resonance voltages were observed to be shifting to higher values with decreasing temperature. While applying the gradually increasing (0.2 V/s) potential of 20V, the current peak positioned was observed at around 5.5±0.5V at room temperature. At 180 K, more than one current peak were observed at voltages higher than ~7.8V. At 15 K, with the applied forward bias (from 0 to 15V), the resonant voltage was observed at around 11.5V where the current jumped up from 20nA to 35nA, then stayed at these higher voltages with some fluctuation. Then reverse bias (from 15 to 0V) was applied and non linear I-V behavior was observed. Figure 45 - 47 exhibits this I-V performance of ETS-4 crystal performed at 298, 180 and 15 K.
Figure 45: Current peaks observed on current-voltage behavior of the ETS-4 device obtained at 298 K.

Figure 46: Current peaks observed on current-voltage behavior of the ETS-4 device from 2 consecutive measurements at 180 K; circles 1st run, triangles 2nd run.
Figure 47: Current peak and non linear behavior observed on current-voltage behavior of the ETS-4 device obtained at 15 K for (a) forward and (b) reverse current.

The separation between the gold electrodes of ETS-4 device used for the measurements was 50µm. As seen from Figure 45, the I-V performance of ETS-4 device at room temperature is similar to the one obtained by landing microprobes on the surface of single crystal with the separation of 50µm (Figure 39 b). At 180 K, multiple resonant peaks were observed with much higher current values of ~250nA, as seen on Figure 46. At 15 K, current increased nonlinearly first, then jumped from 20µA to 35µA and stayed at higher current values with multiple fluctuations. At low the temperature of 15 K, resonant tunneling between the chains is observed at larger potentials. Up to the resonant voltage, electron transfer can be hypothesized to occur through the randomly broken titania chains in which carriers are confined better due to the low temperature values. Then at the resonant voltage, current jumps up to the higher values.
The effect of temperature of the ETS-4 device was performed under an applied voltage of 0.5 V. While decreasing the temperature from room temperature (298 K) to 82 K; initially, first sharp a nonlinear smooth decrease in the current is observed down to 230 K, then the current stayed at these low values with further decrease in temperature. Based on the observations above (Figure 38 & 39), resonance voltage for ETS-4 material is around 4.5V; resonance has never been reached due to the low voltage (0.5V) applied. It turns out to be that no resonance tunneling through siliceous layer has occurred during this measurement and electron transport might be controlled only through the chains on the surface. Such a decrease in the current with decreasing temperature is consistent with semiconductor behavior. Furthermore, this measurement was only performed on one ETS-4 device, so reproducibility of this specific measurement needs to be verified. Figure 48 illustrates the temperature dependency of ETS-4 device and inset is the exponential fit of temperature dependency curve.
Therefore, it can be suggested that electron transfer in ETS material occurs through the titania chains via tunneling, where these chains are randomly broken at certain points due to the defects. And the cations present in the pores decreases the barrier between the discrete chains; therefore increases the probability of tunneling from one chain to the other. The current-voltage behaviors performed at lower temperatures reveals that resonant tunneling occur with a very high PVCR at higher resonant voltage values. This supports the hypothesis that electron transfer also occurs between titania chains through siliceous layer via resonant tunneling.

Based on these results, an electron transport mechanism is hypothesized as follows; electrons tunnel through insulating SiO₄ layer due to matching of the energy levels. These electrons which tunneled through insulating layer also run along the titania

Figure 48: Temperature dependency of ETS-4 device. Inset is exponential fit of temperature dependency curve.
chains ($b$ direction for ETS-4 and $a$ or $b$ direction of ETS-10). Because these titania chains were previously hypothesized as discrete chains, electrons may also tunnel between discrete chains; which allows the current pass through the other probe. Tunneling between discrete chains is quite probable for two reasons; first, electron mobility in quantum wires is in the order of $10^7$-$10^8$ cm$^2$/Vs [59] which is 3 orders of magnitude larger compared to nanowires (e.g. electron mobility is 3100 cm$^2$/Vs for GaN/AlN/AlGaN nanowire [81] or 2000-6000 cm$^2$/Vs for InAs nanowire [82]); secondly, the cations in the framework fundamentally decreases the potential barrier between discrete titania chains [64] and this increases the probability of tunneling along the discrete chains. Tunneling through siliceous layer occurs only at certain voltages (resonance voltage) and manifests itself as current peak in the I-V behavior. Tunneling between discrete chains might occur anytime and manifest itself as non-linear I-V behavior which overlaps with the current peak at resonance voltage.
Ordered aligned titania chains isolated from one another by highly insulating siliceous layer in ETS material is hypothesized to be utilized as quantum wires arrays. In order to be able utilize these ETS materials, current-voltage performance of the titania chains as hypothesized quantum wires were studied. Current-voltage curves of individual ETS-4/10 were carried out at room temperature by placing probes on the surface of a crystal. Current-voltage performance of ETS-4 was also performed at lower temperature via device integration of individual crystal. Current peaks were observed both at room temperature and low temperature for both materials. It was expected a Schottky barrier to form at the contact for both measurements performed by probe station and device integration, but not dominating the I-V performance due to small contact area for the probe station measurement. **Peak to valley current ratio (PVCR)** was observed to increase with increasing number of layers (titania chains – siliceous matrix) involving in the conduction, and also to increase with decreasing temperature. Based on the various measurements performed on each individual crystal, it was hypothesized that conduction occurs through monatomic discrete titania chains via tunneling, and cations present in the structure decreases the potential barrier which increases the probability of tunneling through broken chains. On the other hand, observed current peaks were attributed to resonant tunneling between 2D confined titania chains through the insulating silica layer.
7.0 RECOMMENDATIONS

1. Current – Voltage curves of ETS-4 should be performed at low temperatures to confirm the reproducibility of the data obtained in this work.

2. Current – Voltage curves should be performed by sweeping at different speeds.

3. Four-probes measurements should be performed to verify that there is no contact resistance.

4. Current – Voltage curves should be performed on ETS-4 and ETS-10 when set up to run orthogonal to the direction of the chains, then on the top while keeping one probe fixed and moving the other radically various distances (10um, 20um, 50 um, 80 um) then moving original position and performing the measurements again.

5. Current - Voltage curves should be performed after removing the absorbed water in the pores of ETS materials to verify that water in the pores has no effect on the I-V curves. This can be done by placing the probes on the crystal in the vacuum chamber. Temperature is increased to 323 K and kept at that temperature for about 1 hour to remove the water. Then without removing the vacuum, temperature is decreased to room temperature and I-V measurement can then be performed. It is important not to remove the vacuum before completing the I-V measurement; because ETS crystals (generally zeolites) can absorb the water/humid in the air immediately.

6. In order to optimize the device integration of a single crystal –which is necessary for low temperature measurements-, gold etching can be done by utilizing Focused Ion Beam (FIB). This can be done as follows; substrate is cleaned and crystals are dispersed on the substrate, as mentioned in the text. It is followed by angled metal deposition; in which, orientation of the single crystal to be utilized in the device should
be determined precisely. Then, FIB is used for metal etching. The advantage of this method is two fold; first, it eliminates the use of photolithography so the possible photoresist residue at the contact; secondly, makes it possible to keep the distance between two electrodes in micron range.

Figure 49: 54’ degree tilted SEM image of prototype micro-device of large monolithic ETS-10 utilizing FIB for etching the gold.
8.0 REFERENCES


[60] Li Y.; J. Xiang; F. Qian; S. Gradecak; Y. Wu; H. Yan; D.A. Blom; C.M. Lieber, Nano Lett. 6, pp.1468, 2006.


APPENDICES
Appendix A

Step by step procedure for the device integration of ETS crystal
• Si/SiO₂ wafer was cut into smaller square pieces with the average dimensions of 2cm x 2cm.

• Si/SiO₂ wafer preparation was performed to improve the adhesion of the photoresist.
  o Wafer was cleaned to remove the contamination;
    ▪ Solvent Cleaning
      • 5 minutes in ultrasonic acetone bath
      • 5 minutes in static methanol bath
      • 1 minute rinsing with isopropyl alcohol
      • Blow drying with pressurized nitrogen gas
    ▪ RCA Cleaning
      • Organic Cleaning
      • Oxide Strip
      • Ionic Cleaning
  o Clean wafer was dehydrated;
    ▪ 5 minutes hard baking at 473 K
    ▪ Cooling down to room temperature in ambient air
  o Spin coating with adhesion promoter hexamethyldisilizane (HMDS) was performed at speed of 2000rpm for 30 seconds with the ramp time of 5 seconds.
  o Spin coating with positive photoresist (PR S 1805) was performed;
- Coating at speed of 500 rpm for 5 seconds with a ramp time of 5 seconds; then at speed of 4000 rpm for 40 seconds with a ramp time of 1 second.
- Soft baking at 388 K for 2 minutes in ambient air
- Cooling down to room temperature in ambient air

- Large monolithic ETS-4 crystals were sparsely dispersed onto the wafer via spin coating.
  - ETS-4 crystals were suspended in hexamethyldisilizane (HMDS)
  - Spin coating was performed at speed of 500 rpm for 5 seconds with a ramp time of 5 seconds; then at speed of 4000 rpm for 40 seconds with a ramp time of 1 second.
• Photolithography was carried out using negative photoresist SU-8, 2010;
  o Spin coating first at 500 rpm for 5 seconds with a ramping time of 5 seconds, then at 3000 rpm for 30 seconds with a ramping time of 8 seconds.
  o Two-step contact soft baking at 338 K for 1 min, then at 368 K for 2 min.
  o Slow cooling down by setting the hot plate temperature at 293 K (RT) in ambient air.
  o UV-exposure of 24 seconds with an intensity of 65 mW/cm².
  o Two-step post exposure baking at 338 K for 1 min, then at 368 K for 2.5 min
  o Slow cooling down by setting the hot plate temperature at 293 K (RT) in ambient air.
  o Development of the unexposed parts;
    ▪ Gently shaking in PGMEA bath for 3 minutes
    ▪ Rinsing with isopropyl alcohol for 30 seconds

<table>
<thead>
<tr>
<th></th>
<th>Slow Spin</th>
<th>Fast Spin</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Speed (rpm)</td>
<td>Time (s)</td>
</tr>
<tr>
<td>HMDS</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PR-S 1805</td>
<td>500</td>
<td>5</td>
</tr>
<tr>
<td>Crystal Dispersing</td>
<td>500</td>
<td>5</td>
</tr>
<tr>
<td>SU-8 2010</td>
<td>500</td>
<td>5</td>
</tr>
<tr>
<td>PR-S 1813</td>
<td>500</td>
<td>5</td>
</tr>
</tbody>
</table>

• Angled metal deposition was performed utilizing thermal evaporator
  o 10 nm of Chromium deposition
- 140 nm of Gold deposition with an angle of 20° (700 from each side)

- Photolithography was carried out using positive photoresist PR-S 1813;
  - Spin coating at 500 rpm for 5 seconds with a ramping time of 5 seconds, then at 4000 rpm for 40 seconds with a ramping time of 1 second.
  - Soft baking at 388 K for 2 minutes in ambient air
  - Cooling down to room temperature in ambient air
  - UV exposure of 20 seconds with the intensity of 65mW/cm²
  - Development of the exposed parts;
    - Gently shaking in CD-30 bath for 90 seconds
    - Rinsing with deionized water for 30 seconds

- Metal etching was performed to remove metal outside the device pattern
  - Gently shaking the sample in diluted (1 etcher / 2 deionized water) gold etcher solution for 50 seconds
  - Rinsing with deionized water for 30 seconds
  - Gently shaking the sample in diluted (1 etcher / 2 deionized water) chromium etcher solution for 30 seconds
  - Rinsing with deionized water for 20 seconds

- Sample was washed to remove the photoresist on the top of the surface
  - 15 seconds in a static acetone bath
  - 15 seconds in a methanol bath
  - 10 seconds in a isopropyl alcohol bath
  - Blow dried with pressurized N₂ gas
APPENDIX B

Step by step procedure for the placing the probes on ETS crystal

• Substrate preparation involving solvent cleaning and dehydration
• Crystal attachment
  o HMDS and 1813 coating
  o Crystal dispersion
  o Gradual Hard Baking (details can be seen in Section 4.1.1.2)
APPENDIX C

Calculation of *Peak to Valley Current Ratio* (PVCR)

*Peak to Valley Current Ratio* = Current Value at the Peak / Current Value at the Valley
Önnaz Özkanat  
3 Smitsteeg, 2611 BH, Delft, The Netherlands  
31 (6) 444 78775, onnazozkanat@gmail.com

EDUCATION

October 2012 (expected)  
Technology University of Delft, Delft/Netherlands  
PhD in Material Science

May 2009  
Northeastern University, Boston, MA/USA  
M.S. in Chemical Engineering  
GPA: 3.89/4.00

May 2006  
Middle East Technical University (METU), Ankara/TURKEY  
B.S. in Chemical Engineering

WORK EXPERIENCE

Oct 2008 - Current  
Department of Mechanical Maritime and Materials Engineering,  
Technical University of Delft, Delft, The Netherlands  
Surface and Interface Group,  
PhD Researcher  
Study adhesion mechanism between Aluminum alloys and organic coatings

Sep 2006 - Sep 2008  
Department of Chemical Engineering, Northeastern University, Boston, MA  
Center for Advanced Microgravity Materials Processing (CAMMP, NASA)  
Research Assistant  
Study zeolites and quantum wires  
Collaborate with Harvard University, Center for Nanoscale Facilities

INTERNSHIPS

June – July 2005  
Alkim Paper Industry and Commerce Company, Izmir / TURKEY  
Process Control Dept. and Research & Development Dept. Intern  
Participated in research on paper technology and perceived process control

February 2004  
Dalan Chemical Incorporation, Izmir / TURKEY  
Production Process – Laboratory Intern  
Performed field and laboratory tests, analyzed the data

SKILLS


Language: Turkish as a native tongue, English (Fluent in all skills), Dutch (Beginner)
PROFESSIONAL AFFILIATIONS:
Lean Six Sigma, White Belt, 2008-current
Member of American Institute for Chemical Engineers (AICHE), 2007-2009
Member of American Chemical Society (ACS), 2007-2008

CONFERENCES:
• "Quantum Wires in the Framework of ETS-4 and ETS-10" Onnaz Ozkanat, Jiangdong Deng, Albert Sacco Jr., Annual American Institute of Chemical Engineers Meeting Salt Lake City, UT USA, November 2007.
• "First Unseeded Synthesis of Large-Pore Vanadocilicate AM-6 Crystals" Mariam N. Ismail, Onnaz Ozkanat, Zhaoxia Ji, Juliusz Warzywoda, Albert Sacco Jr., American Chemical Society, 234th National Meeting & Exposition, Boston, MA USA, August 2007.

VOLUNTARY WORKS
May 2009 Aluminum Surface Science and Technology Symposium (ASST)
5th International Symposium
Session aide and program book design
February 2008 The American Association for the Advancement of Science (AAAS)
Annual Meeting, Boston/MA
Session aide
Session monitoring which includes evaluating audience interest, session content, and speaker performance; and providing audio-visual assistance
August 2005 UNIVERSIADE 2005, Izmir/TURKEY
Athlete’s Villages Delegation Information Center
Dealt with any problems of head of delegations of the participant countries
July 2004 Youth Services Center (YIB), Ankara/TURKEY
Participated in Voluntary Workcamp in France
Renovated an old station with a team
Fall 2001 AIESEC, Ankara/TURKEY
Interns Matching Office
Corresponded with the students abroad for arranging proper internships

INTERESTS & HOBBIES
• Astronomy, Modern Physics, Gliding (Received Certificate from Turkish Aeronautical Association for having attended the glider flight course.)
• Getting to know new cultures and countries
• Photographing, Traveling, Reading, Philosophy