Fully Integrated On-Chip Switched Capacitor
DC-DC Converters for Battery-Powered
Mixed-Signal SoCs

A Dissertation Presented
by
Heungjun Jeon
to
The Department of Electrical and Computer Engineering

in partial fulfillment of the requirements
for the degree of

Doctor of Philosophy
in the field of

Electrical Engineering

Northeastern University
Boston, Massachusetts

October 2012
Abstract

To prolong the life of the battery, the analog and digital modules in modern mixed-signal SoCs are designed to consume extremely low power (<10mW). Since each module requires its own supply voltage, a large number of linear regulators have conventionally been used as on-chip DC-DC converters to support the local powers from the global power supply. However, as the voltage drops between the global power supply and the local power supplies increase, the collective power loss from the linear regulators becomes significant. Due to its higher efficiency, an on-chip switched-capacitor (SC) DC-DC converter is a promising alternative to an on-chip linear regulator.

In this dissertation, a new 4-to-3 step-down topology for on-chip SC DC-DC converters, which efficiency is less sensitive to increasing bottom-plate capacitance ratio ($\alpha$) than the conventional topologies, is proposed. In addition, two different implementations of on-chip SC DC-DC converters using the new 4-to-3 step-down topology are presented.

For the first implementation, the on-chip SC DC-DC converter supports a programmable regulated load voltage ranging from 2.6V to 3.2V out of 5V input power supply. Only MOS capacitors ($2.7fF/\mu m^2$, $\alpha=6.5\%$; $\alpha$ is the bottom-plate capacitance ratio) are used as flying capacitors (900pF) and load capacitor (400pF) for the minimum area/cost. To maximize the load current driving capability while minimizing the bottom-plate capacitance loss, the proposed 4-to-3 step-down topology utilizes two conventional 2-to-1 step-down topologies; each of them (2-to-1$_{up}$ and 2-to-1$_{dw}$) has a different flying capacitance. As the control circuits operates at a low power supply (1.6V), which is provided by a small internal LDO connected to the internal load voltage ($V_L'$) from the 2-to-1$_{dw}$, and the internal load voltage ($V_L'$) is used to generate low swing level-shifted gate-driving signals, the proposed implementation reduces control circuit and switching losses as well. The proposed converter achieves the peak efficiency of 74% while it delivers the load current between 1mA and 10mA. 10-phase interleaving technique enables the maximum voltage ripple in the load voltage to be less than 1% of the average load voltage (@ 3.2V).

For the second implementation, the on-chip SC DC-DC converter that supports two regulated load voltages (2.2V and 3.2V) from 5V input supply and delivers the maximum load currents up to 8mA is proposed. The entire converter
utilizes two conventional 2-to-1 converter blocks. The upper output voltage (3.2V) is generated from the 2-to-1_up converter and the lower output voltage (2.2V) is generated from 2-to-1_dw converter. Since the efficiency of the 2-to-1_up converter is less sensitive to increasing $\alpha$, it is implemented with MOS capacitors while the bottom-plate capacitance loss sensitive 2-to-1_dw converter is implemented with MIM capacitors ($1fF/\mu m^2$, $\alpha=2.5\%$). The proposed implementation saves the area and quiescent currents for the control blocks since each converter block shares required analog and digital control circuits. Over the wide output power ranges from 5.4mW to 43.2mW, the converter achieves the average efficiency of 70.0% and the peak efficiency of 71.4%. 10-phase interleaving technique enables the maximum voltage ripples in the both loads less than 1% of the load voltages.

The two SC DC-DC converters presented in this dissertation are designed and simulated using high-voltage 0.35$\mu$m BCDMOS technology and demonstrate higher than 70% peak efficiencies. Efficiencies of the both converters are less sensitive to increasing $\alpha$ than the conventional SC topologies. This work shows that the on-chip SC DC-DC converters can outperform the linear regulators in terms of efficiency, at least 10% higher efficiency, with a little expense of area/cost. Since the merits of the SC converters have be increasing with technology scaling, SC DC-DC converters are promising alternatives of linear regulators for low power (<50mW) on-chip DC-DC converters’s applications in the modern portable SoCs.
Acknowledgements

I sincerely thank my advisor and mentor Professor Yong-Bin Kim for his continuous guidance, support, encouragement, and motivation throughout my years of graduate studies. I would also like to thank my committee members, Professor Fabrizio Lombardi and Professor Marvin Onabajo for their advice on my dissertation.

I would like to thank my parents, younger sister, and other family members for the love and support they have given me.

A special thank you must go to all past and present HPVLSI members Kyungki Kim, Youngbok Kim, Kwonjae Shin, Hojun Lee, Inseok Jung, Moonseok Kim, Yongsuk Choi, and Kyuin Sim. Without their support and encouragement, I would not have completed this dissertation.
# Contents

List of Figures vi

List of Tables ix

1 INTRODUCTION 1

1.1 Power Management for a Modern SoC 1

1.2 Thesis Objectives and Contributions 5

2 OVERVIEW OF ON-CHIP DC-DC CONVERTER ARCHITECTURES 10

2.1 Linear Voltage Regulators 10

2.2 Inductor based Switching DC-DC Converters 13

2.3 Switched Capacitor DC-DC Converters 15

3 DESIGN CHALLENGES IN ON-CHIP SC DC-DC CONVERTERS 19

3.1 Core Design 19

3.1.1 Multiple Voltage Generation 19

3.1.2 Load Current Driving Capability & Output Resistance Analysis 22

3.1.3 Loss Mechanisms 25

3.1.3.1 Conduction loss (Charge transfer loss) 26

3.1.3.2 Bottom-plate and parasitic capacitors loss 27

3.1.3.3 MOSFET gate-drive switching loss 29

3.1.3.4 Control circuit loss 30

3.2 Voltage Regulation Techniques 31

3.2.1 Pulse Frequency Modulation (PFM) Technique 31

3.2.2 Switch Width Modulation Technique 36

3.2.3 Flying Capacitor Modulation Technique 37

3.3 High-Speed Low-Power Low-Offset Comparator 37
## CONTENTS

3.4 Summary ................................................. 38

4 PROPOSED ON-CHIP SWITCHED-CAPACITOR DC-DC CONVERTERS 40

4.1 Single Output On-Chip SC DC-DC Converter Design ............ 41

4.1.1 Core Design ............................................ 41

4.1.1.1 Operating principle ................................. 41

4.1.1.2 Charge Transfer and Loss Mechanisms ............. 44

4.1.2 Architecture .............................................. 51

4.1.3 Simulation Results ...................................... 53

4.2 Dual Output On-Chip SC DC-DC Converter Design ............ 58

4.2.1 Core Design ............................................ 58

4.2.1.1 Charge Transfer and Loss Mechanisms ............. 58

4.2.2 Architecture .............................................. 63

4.2.3 Simulation Results ...................................... 65

4.3 Major Sub-Circuits ......................................... 70

4.3.1 Bandgap Voltage Reference ............................. 70

4.3.2 Current Reference ....................................... 73

4.3.3 Linear Regulator ......................................... 75

4.3.4 Dynamic Comparator ..................................... 77

5 PROPOSED LOW-POWER, LOW-OFFSET, AND HIGH-SPEED CMOS DYNAMIC LATCHED COMPARATOR 81

5.1 Background .................................................. 81

5.2 Prior Arts ................................................... 83

5.3 Operation Principles of Proposed Comparator ................. 86

5.4 Offset Analysis of Proposed Comparator .................... 89

5.4.1 Offset Voltage in Differential Input Gain Stage ....... 91

5.4.2 Offset Voltage in Regenerative Output Latch Stage .... 96

5.5 Offset Calibration Techniques ............................. 101

5.6 Simulation Result ........................................... 105

6 CONCLUSION ............................................... 106

6.1 Summary of Contributions ................................ 106

6.1.1 On-Chip Switched Capacitor DC-DC Converter ........ 106
## List of Figures

1.1 (a) Typical circuit blocks in a smartphone and how they are powered (b) Functional block diagram of PMIC .......................... 2
1.2 Power regulation method in modern mixed-signal SoCs in Portable Devices [18, 56] ................................................................. 3
1.3 Future direction of a smartphone chip set ................................. 5

2.1 Typical representation of Low-dropout regulators: (a) Low drop-out (LDO) voltage regulator (b) High drop-out (HDO) voltage regulator .......................................................... 10
2.2 Typical representation of Inductor-based Buck converter ............ 13
2.3 Switched capacitor DC-DC converters (a) 1-to-1 Topology (b) 2-to-1 Topology (c) 1-to-2 Topology (d) 1-to(-1) topology ............ 16

3.1 Typical set of step-down switched capacitor DC-DC converter topologies when the total capacitance of the flying capacitors is kept 6C; (a) 1-to-1 topology (b) 4-to-3 topology (c) 3-to-2 topology (d) 2-to-1 topology (e) 3-to-1 topology .......................... 20
3.2 Maximum attainable efficiencies of five different SC DC-DC converter topologies in Fig.3.1 and for the ideal linear regulator with different load voltages while the input supply voltage $V_{IN}$ is 5V. 21
3.3 Simple equivalent circuit model for SC DC-DC converter; $N$: topology dependent constant explained in Eq.3.1 $R_{out}$: output resistance arising from the series resistance of the switches, $R_{par}$: shunt losses resulting from switching the parasitic capacitances of the flying capacitors and power switches, and $R_L$: load resistance which is $V_L/I_L$ ........................................... 22
3.4 2-to-1 step-down topology with bottom-plate parasitic capacitor ($\alpha C_{fly}$), where $\alpha$ is the bottom-plate parasitic capacitance ratio. 23
LIST OF FIGURES

3.5 Voltage Regulation Techniques of SC DC-DC Converter (a) Pulse Frequency Modulation (PFM) Techniques and Typical Load Voltage Waveforms (b) Switch Width Modulation (c) Flying Capacitor Modulation .................................................. 32

4.1 (a) Conventional 2-to-1 step-down topology (b) Level-shifted non-overlapping gate-driving signals for conventional 2-to1 topology (c) Simplified block diagram of 2-to-1 (step-down) topology (d) Proposed 4-to-3 (step-down) topology .................. 41

4.2 Transistor level implementation of one-phase of 4-to-3 converter core; (a) 2-to-1 dow and 2-to-1 up (b) One of 10 phases of level shifted non-overlapping gate-driving signals ............... 44

4.3 (a) 2-way interleaved structure for the proposed 4-to-3 step-down topology (b) Equivalent circuit for Fig.3(a) ......................... 45

4.4 Efficiency of proposed SC DC-DC converter with a different bottom-plate capacitance ratio ($\alpha$) while delivering the load current of 10mA at the load voltage of 3.2V ($C_{up}$=600pF and $C_{dw}$=300pF) 50

4.5 Efficiency of proposed SC DC-DC converter with a different $C_{up}$ at a constant $C_{fly}=C_{up}+C_{dw}=900pF$ ......................... 51

4.6 Architecture of proposed 10-phase interleaved 4-to-3 step-down switched capacitor DC-DC converter ......................... 52

4.7 Efficiency of proposed SC DC-DC converter with change in load voltage while delivering a load current of 10mA ............... 53

4.8 Efficiency of proposed SC DC-DC converter with change in load current while delivering a load voltage of 3V from 5V input supply 54

4.9 Transient response of $V_L$ with varying load current $I_L$ (1mA to 10mA and vice versa) .................. 54

4.10 (a) 2-way interleaved structure for the proposed dual output topology which provides voltages of $V_L' (=2.2V)$ and $V_L (=3.2V)$ out of $V_{IN} (=5V)$ input. (b) Equivalent circuit for Fig.4.10 ........... 59

4.11 Efficiency drop dependencies with respect to increasing bottom-plate parasitic capacitance ratio ($\alpha$=0% to 7%); Black (Grey) represents the efficiency drop with increasing $\alpha_{up}$ ($\alpha_{dw}$) while $\alpha_{dw}$ ($\alpha_{up}$) is kept constant at 0% .............. 61

vi
## LIST OF FIGURES

4.12 Architecture of dual output switched capacitor DC-DC converter system ........................................ 64
4.13 Efficiency versus $I_L$ while $I_L'$ is varying between 1mA and 8mA .............................................. 65
4.14 Transient response of $V_L$ ($V_L'$) with varying load current $I_L$ (1mA to 8mA and vice versa) while $I_L'=8mA$ .................................................. 67
4.15 Schematic of the bandgap voltage reference ................................................................. 70
4.16 Reference voltage ($V_{rref0}$) variation (Max-Ave-Min) with respect to the temperature variation obtained from 100 times of transient Monte-Carlo device mismatch simulation ........................................ 73
4.17 Reference voltages ($V_{rref0}$-$V_{rref4}$) with respect to the supply voltage variation ($V_{IN}$) ......................... 74
4.18 Schematic of the current reference ......................................................................................... 74
4.19 Schematic of the linear regulator .......................................................................................... 76
4.20 Schematic of the dynamic comparator [30, 31, 32, 33] ......................................................... 77
4.21 Input referred offset voltage before and after optimization from 1000 samples of transient Monte-Carlo Simulation ...................................................... 79

5.1 Typical block diagram of a high-speed voltage comparator ..................................................... 82
5.2 (a) Conventional dynamic latched comparator [37, 83] (b) Comparator1 [60] (c) Comparator2 [45] .............................................................................. 83
5.3 (a) Schematic of proposed comparator (b) Signal behavior of proposed comparator ($\Delta V_{in}=50mV$ (Grey), 5mV (Black) with $V_{DD}=1V$, $f_{Clk}=3GHz$, $C_{load}=7fF$, Temp.=25°C and $V_{com}=0.6V$). ........................................ 87
5.4 (i) Detailed waveforms of Fig.5.3(b) (ii) Absolute values of the voltage differences at between $Di$, $Di'$, and $Sw$. .................................................. 88
5.5 Offset voltage contributions of each stage before (Grey) and after (Black) optimization. ............................. 92
5.6 Simplified schematic of the dynamic differential input gain stage. ............................................ 92
5.7 Simplified schematic of the output stage combined with latch when $Di'$ node voltages ($V_{Di'}$) are reaching around $V_{tn12(13)}$ during evaluation phase. .................................................. 96
5.8 (a) Proposed offset voltage calibration technique using $Di$ node capacitance compensation. (b) Offset voltage calibration logic. (c) Signal waveforms of the proposed offset calibration process with the intentional $V_{OS}$ of +20mV and $f_{CLK}=3$GHz. 

5.9 Input referred offset voltage before and after offset calibration obtained from 1000 samples of transient Monte-Carlo.
# List of Tables

4.1 (a) Load voltages ($V_L$) and (b) overall efficiency variations with PVT variations .................................................. 56

4.2 Comparison with Recently Published SC DC-DC Converters 1 . 57

4.3 Percent variations and average recovery times of load voltage $V_L$ (or $V_L'$) with the step changes in the load current (a) $I_L'$ (or (b) $I_L$) ................................................................. 68

4.4 Load voltages ($V_L$ and $V_L'$) and overall efficiency variations with PVT variations ...................................................... 69

4.5 Comparison with Recently Published SC DC-DC Converters 2 . 70

5.1 Performance Comparison .................................................. 105
Chapter 1

INTRODUCTION

1.1 Power Management for a Modern SoC

Recently, the popularity of portable smart devices such as smart phones and tablet PCs continues to increase. Since most of the portable electronic devices are powered by a battery, the battery-life time of smart devices has been drawing a lot of attention in recent years. Among the different kinds of batteries, lithium-ion (Li-ion) batteries have become popular for a variety of portable electronics such as smart devices and laptops due to the advantages such as high energy density, a large number of recharge cycles, no memory effect, relatively high output voltage, and a slow discharge when not in use. However, due to the physical limits of electro-chemistry, the advance in battery technology has not kept pace with the increasing demand for integrating more functions in the portable electronic devices [54].

Fig. 1.1 shows typical circuit blocks in a smartphone and its power management integrated circuit (PMIC). The complex functionality within a smartphone
1.1 Power Management for a Modern SoC

Figure 1.1: (a) Typical circuit blocks in a smartphone and how they are powered (b) Functional block diagram of PMIC

consists of a variety of different circuits and blocks. Since each circuit block commonly has a different functionality, each needs a specific load requirement such as a DC voltage level, current driving characteristic, regulation precision, noise level, and dynamic characteristic to operate properly. Especially, there are certain blocks such as the power amplifier and application processor (AP) which consume the majority of the power within a smartphone. These blocks are commonly supplied by the individual inductor-based DC-DC converters in PMIC to get more than 90% efficiency. Those high efficient global voltages are shared by other voltage regulators to provide power to the other sub-blocks within the smartphone. Every block cannot have its own dedicated inductor-based DC-DC converter because of the limited number of pins, cost, and volume penalty imposed by these converters. Hence, most of the local supply voltages
are generated from linear regulators mostly due to the small areal size. They are also called as low-dropout regulators (LDOs) if the linear regulators can operate with a very small dropout voltage (∼0.2V), which is defined as a voltage difference between the input supply voltage and regulated output voltage. However, since the efficiency of the linear regulators decreases linearly with the increasing dropout voltage, if a large number of linear regulators are used as on-chip voltage regulators, the collective power loss from them can be significant.

Figure 1.2: Power regulation method in modern mixed-signal SoCs in Portable Devices [18, 56]

A typical modern mixed-signal SoC, as shown in Fig.1.2, exploits two high efficiency off-chip inductor based switching regulators which operate directly from the Li-Ion battery (nominal voltage of 3.6V) to generate two global power supplies; one for the analog supply and the other one for the digital supply used...
1.1 Power Management for a Modern SoC

by DSP. These two switching regulators are typically implemented in a separate chip using a high voltage technology due to the reliability issues such as gate oxide breakdown. Then, the local power supplies for the mixed signal modules are conventionally distributed by linear regulators from one of the global power supplies. Since DSP typically employs dynamic voltage scaling and the digital supply includes lots of unpredictable noise, the global analog supply is used for the generation of local power supplies. As mentioned earlier, linear regulators are cost/area effective; however, as the voltage drops between the main power supply and the local power supplies increase, the collective power loss from the linear regulators becomes significant. For this reason, more power efficient switching alternatives, which consume an area which is as close as possible to an equivalent linear regulator, are required to achieve high efficiency in a broad range of the output voltages.

Since on-chip capacitors have significantly higher quality factor, higher energy density, and lower cost than on-chip inductors in standard CMOS process, switched-capacitor (SC) based on-chip converters have been receiving increased attention from both academia and industry [6, 8, 11, 29, 38, 49, 53, 56, 65, 68, 71, 74, 76, 88, 89].

More recently, there has been a lot of attention to integrate the whole power management system into a single system-on-chip (SoC) solution, as shown in Fig.1.3 to further reduce the PCB size while minimizing the losses [28, 35, 54].
1.2 Thesis Objectives and Contributions

Since the gate oxide capacitance per unit area \( (C_{ox}) \) of MOS capacitor has been increased with the continuous technology scaling, if MOS capacitors are used as charge transfer (or flying) capacitors and a load capacitor instead of MIM or MOM capacitors, SC DC-DC converters can save the total area significantly. For example, the \( C_{ox} \) for 1\( \mu \)m technology \( (t_{ox}=20\text{nm}) \) is 1.75\( fF/\mu m^2 \) while the \( C_{ox} \) for 50nm technology \( (t_{ox}=1.4\text{nm}) \) is 25\( fF/\mu m^2 \) [4]. Moreover, since the on-resistance per unit area has been continuously decreasing with technology
1.2 Thesis Objectives and Contributions

scaling, the size of MOS switches decreases as well when they are designed to have the same on-resistances of the older technology. Therefore, the switching frequency of on-chip SC DC-DC converters can be increased to reduce the area of flying capacitors without compromising the efficiency. However, the bottom-plate parasitic capacitance of a MOS capacitor formed by the junction capacitance of drain/source terminals to the substrate (or bulk) is larger than that of MIM or MOM capacitors; it can be as large as 10% of the actual capacitance. Therefore, if MOS capacitors are used as flying capacitors, the loss due to the bottom-plate capacitors is significant. For example, with 10% of bottom-plate capacitance ratio ($\alpha$), the overall efficiency of the conventional 2-to-1 step-down topology can drop more than 20% when comparing to the case with 0% of bottom-plate capacitance ratio ($\alpha$) when it delivers 85% of the no-load voltage.

In this dissertation, a new 4-to-3 step-down topology for the on-chip SC DC-DC converter, which is less sensitive to increasing bottom-plate capacitance than the conventional topologies, is proposed. In addition, a new low-offset, low-power and high-speed dynamic latched comparator, which is used as a main component for the load regulation scheme, is proposed with the offset calibration technique.

Chapter 2 briefly summarizes prior arts of on-chip DC-DC converters and chapter 3 describes design challenges in on-chip SC DC-DC converters in terms
of multiple voltage generation, load current driving capability and output resistance analysis, loss mechanisms, voltage regulation techniques, and the necessity for the high-speed low-power low-offset comparator.

Chapter 4 describes two implementations of on-chip SC DC-DC converters using proposed 4-to-3 topology. Chapter 4.1 presents the proposed on-chip SC DC-DC converter design that supports a programmable regulated load voltage ranging from 2.6V to 3.2V out of 5V input power supply. Only MOS capacitors \( (2.7fF/\mu m^2, \alpha=6.5\%; \alpha \text{ is the bottom-plate capacitance ratio}) \) are used as flying capacitors (900pF) and load capacitor (400pF) for the minimum area/cost. To maximize the load current driving capability while minimizing the bottom-plate capacitance loss, the proposed 4-to-3 step-down topology utilizes two conventional 2-to-1 step-down topologies; each of them \( (2\text{-to-}1_{up} \text{ and } 2\text{-to-}1_{dw}) \) has a different flying capacitance. As the control circuits operates at a low power supply (1.6V), which is provided by a small internal LDO connected to the internal load voltage \( (V_L') \) from the \( 2\text{-to-}1_{dw} \), and the internal load voltage \( (V_L') \) is used to generate low swing level-shifted gate-driving signals, the proposed implementation reduces control circuit and switching losses as well. The proposed converter achieves the peak efficiency of 74% while it delivers the load current between 1mA and 10mA. 10-phase interleaving technique enables the maximum voltage ripple in the load voltage to be less than 1% of the average load voltage (at 3.2V).
Chapter 4.2 presents another proposed on-chip SC DC-DC converter design that supports two regulated load voltages (2.2V and 3.2V) from 5V input supply and delivers the maximum load currents up to 8mA is proposed. The entire converter utilizes two conventional 2-to-1 converter blocks. The upper output voltage (3.2V) is generated from the $2\text{-to-}1_{\text{up}}$ converter and the lower output voltage (2.2V) is generated from $2\text{-to-}1_{\text{dw}}$ converter. Since the efficiency of the $2\text{-to-}1_{\text{up}}$ converter is less sensitive to increasing $\alpha$, it is implemented with MOS capacitors while the bottom-plate capacitance loss sensitive $2\text{-to-}1_{\text{dw}}$ converter is implemented with MIM capacitors ($1fF/\mu m^2$, $\alpha=2.5\%$). The proposed implementation saves the area and quiescent currents for the control blocks since each converter block shares required analog and digital control circuits. Both output voltages are regulated by means of pulse frequency modulation (PFM) technique using two 18-bit shift registers and two digitally controlled oscillators (DCOs). Over the wide output power ranges from 5.4mW to 43.2mW, the converter achieves the average efficiency of 70.0\% and the peak efficiency of 71.4\%. 10-phase interleaving technique enables the output voltage ripples of the both outputs less than 1\% ($<40mV$) of the output voltages when 400pF of output buffer capacitors are used for both outputs.

In chapter 5, a novel fast-speed, low-power, and low-offset dynamic latched comparator with offset voltage compensation is proposed and analyzed. The dynamic comparator is designed and simulated using 90nm PTM technology
for the proper comparison with the state-of-the-art dynamic comparators. The proposed comparator uses one phase clock signal for its operation and can drive a larger capacitive load with complementary latched outputs. As it provides a larger voltage gain up to 22V/V to the regenerative latch, the input-referred offset voltage of the latch is reduced and meta-stability is improved. It demonstrates up to 24.6% less offset voltage and 30.0% less sensitivity of delay to decreasing input voltage difference (17ps/decade) than the conventional double-tail latched comparator at approximately the same area and power consumption. In addition, with a digitally controlled capacitive offset calibration technique, the offset voltage of the proposed comparator is further reduced from 6.50mV to 1.10mV at 1-sigma at the operating clock frequency of 3 GHz, and it consumes 54µW/GHz after calibration.
Chapter 2

OVERVIEW OF ON-CHIP DC-DC CONVERTER ARCHITECTURES

2.1 Linear Voltage Regulators

There are largely two major topologies for CMOS linear regulators: high dropout (HDO) regulator, as shown in Fig.2.1(b), which pass transistor is NMOS transistor and has common-drain configuration, and low dropout (LDO) regulator.\[12\],

Figure 2.1: Typical representation of Low-dropout regulators: (a) Low drop-out (LDO) voltage regulator (b) High drop-out (HDO) voltage regulator
as shown in Fig.2.1(a), which pass transistor is PMOS transistor and has common-source configuration.

Assume that $M_p$ and $M_n$ operate in the saturation region, the minimum dropout voltage ($V_{DO}$) for $M_p$ is approximately the overdrive voltage, which is typically below 200mV while the minimum $V_{DO}$ for $M_n$ is $V_{DS} = V_{GS} = V_{tn} + V_{OV}$; therefore, $V_{DO}$ for $M_n$ is at least bigger than the threshold voltage of the $M_n$. Therefore, HDO regulators are less efficient than LDO regulators. However, HDO regulators have several performance advantages over LDO regulator. First, HDO regulator is more stable than LDO regulator since the output impedance of an NMOS pass transistor ($\sim 1/(g_{m,N} + g_{mb,N})$) is less than that of an PMOS pass transistor ($r_{o,P}$); thus, the output pole of HDO regulator is much higher than LDO regulator. Second, HDO regulators require less die area than LDO regulator since the mobility of NMOS (electrons) is around three times larger than that of PMOS (holes). Third, HDO regulators show generally better power supply rejection (PSR) since the common-drain configuration shields the supply voltage ripples while the output voltage of the common-source configuration is directly coupled to the supply voltage ripples. Lastly, HDO regulators have better AC line regulation due to better PSR; in addition, they have better load regulation and less over/under shoot due to the common-drain (source follower) configuration. Due to these advantages, researches have studied the methods to generate a higher than supply gate voltage ($V_G$) [9, 14, 21, 27].
PMOS transistor is generally used for low dropout voltage (LDO) without a need for a large gate overdrive. In addition, if $M_p$ operates with a large gate overdrive voltage ($V_{SG} - |V_{tp}|$), the area required for $M_p$ can be reduced significantly. As shown in Fig. 2.1(a), the error amplifier compares the scaled regulator’s output voltage ($V_{FB}$) with a reference voltage ($V_{REF}$). If the $V_{FB}$ is less than the reference voltage, the output voltage of the error amplifier decreases; thus, the load current delivered through the PMOS pass transistor increases until the $V_{FB}$ is equal to the $V_{REF}$. Since the current delivered to the load is the same as the current extracted from the input supply, the maximum efficiency achievable is limited to the ratio of the output voltage to the input voltage ($V_L/V_{IN}$). Thus, as the load voltage decreases away from the battery voltage, the efficiency of the linear regulator decreases accordingly. This limits the potential savings in power consumption that can be achieved by lowering the voltage through dynamic voltage scaling.

Recently, with the increasing demand for system-on-chip designs, there is a growing trend toward power-management integration. On-chip and local LDOs are utilized to support multiple on-chip voltage levels to sub-blocks of a system with the advantages of reduced both area and external pins. In addition, since the operating frequencies of switching converters are increasing to allow higher level of integration, this trend increases the frequency of output...
2.2 Inductor based Switching DC-DC Converters

ripples and therefore the subsequent LDO regulator should provide high power-supply-rejection (PSR) up to switching frequencies [15, 86].

2.2 Inductor based Switching DC-DC Converters

![Diagram](image)

**Figure 2.2**: Typical representation of Inductor-based Buck converter

The off-chip inductor based switching DC-DC converters have been most widely used for a high power (current) converter with high efficiency (>90%), which can generate lower, higher, or of opposite polarity DC load voltages with respect to the input supply voltage. A buck-type (step-down) regulator, as shown in Fig 2.2, can generate different levels of reduced DC load voltages, which is the same polarity of the input voltage and is less than the input voltage. The different levels of DC load voltages are generated by filtering out a pulse-width
modulated (PWM) signal through the LC filter. If the switches and passives (inductor and capacitor) are ideal, an inductor based DC-DC converter can theoretically achieve 100% efficiency independent of the different load voltage levels. Moreover, in the context of DVS systems, the output voltage scaling can be completely done with a digital control circuitry \[10, 34, 77\] which consumes very little overhead power. Although this type of DC-DC converters \[85\] can operate at very high efficiencies (>90%), they generally require bulky off-chip filter components.

As explained earlier, state-of-the-art SoCs in portable electronic devices exploit multiple voltage domains to prolong the battery life. The use of multiple external components based DC-DC converters can be energy efficient than the linear regulators. However, it is bulky, cost inefficient, requires a lot of pins for the bond wire connections, and degrades supply impedance. Hence, most of the on-chip DC-DC converters are linear regulators since they require the minimum area and cost. However, the efficiency of linear regulators is poor; therefore, there are lots of research going on to replace the linear regulators with more efficient switching alternatives.

Largely there are two types of on-chip inductors can be used. Inductor can be formed by connecting bond wires in a loop above the chip \[78, 79\]. Bond wire inductors have a relatively low series resistance (approximately 50m Ohm/nH at 100MHz). In addition, they show a low capacitive coupling to the substrate and
2.3 Switched Capacitor DC-DC Converters

Switched capacitor (SC) DC-DC converters consist only of capacitors and switches; thus, they do not require bulky magnetic storage elements used by inductor-based buck converters. Conventionally, two of the most common SC DC-DC converters are the voltage doublers or charge pumps (Fig. 2.3(c)) and the voltage inverters (Fig. 2.3(d)). The voltage doublers \[16, 59, 64, 66\] (Fig. 2.3(c)) output ideally two times of the input voltage while the step-up voltage converters (charge pumps) \[39, 41, 87\] can output multiple times of the input voltage depending on the topology, and the voltage inverter \[2\] (Fig. 2.3(d)) outputs the opposite polarity of the input voltage.
2.3 Switched Capacitor DC-DC Converters

The operation principle of SC DC-DC converters is as follows. During the first half period of the clock signal, the switches notated as $\phi_{1a}$ turn on while $\phi_{1b}$ switches are off and vice versa for the next half period of the clock signal. Turn on (off) cycle of each different notated switch is usually set to as close to as 50\% with the minimal dead-time to prevent shoot-through current since this generally yields the maximum charge transfer efficiency. Once SC converters reach the steady-state operation after the start-up transient, the flying capacitor ($C_{fly}$) only need to deliver a small amount of charge to the output load capacitor ($C_L$) on each switching cycle except for the SC converter shown in Fig. 2.3(b), which delivers charge to the load every half cycle of the switching period. The amount of transferred charge depends on the load condition and the
2.3 Switched Capacitor DC-DC Converters

switching frequency. Assuming that there is no series resistance on the switches and the charging and discharging time of the switches are small enough, since the amount of transferred charge to the load per each cycle is proportional to $C_{Fly} \cdot f_{sw} \cdot \Delta V_L$ (where $\Delta V_L$ is defined as the voltage difference between no-load voltage ($V_{NL}$) and actual load voltage ($V_L$) at steady-state operation), higher switching frequency allows smaller capacitors for the same amount of the voltage droop ($\Delta V_{out}$).

For the real implementation, however, there are practical limitations on the increase of the switching frequency due to the technology limitation and increasing gate-drive switching loss; thus, the efficiency decreases from a certain switching frequency point as the switching frequency increases. Therefore, most of the previous implementations of SC converters have used off-chip capacitors as charge-transfer capacitors\textsuperscript{[22, 57]} to support high load power levels. One commercial SC DC-DC converter employs gain hopping method, which topology of the converter can be reconfigured according to the different input voltage level, to support a wide range of input voltages\textsuperscript{[3]}. Recently, a fully integrated on-chip SC DC-DC converter was described in \textsuperscript{[52]}.

With continuous CMOS technology scaling, the effectiveness of the on-chip SC DC-DC converters has been increasing since the switching frequency can be significantly increased to reduce the total area of SC converters without compromising efficiency. This can be done since the gate-oxide capacitance
per an unit area increases and the on-resistance per unit area decreases. In addition, since the on-chip SC DC-DC converters do not require any bulky off-chip inductors and on-die capacitors have significantly higher quality factor, higher energy density, and lower cost than on-die inductors in standard CMOS process, on-chip SC DC-DC converters receive increased attention from both academia and industry.
Chapter 3

DESIGN CHALLENGES IN ON-CHIP SC DC-DC CONVERTERS

3.1 Core Design

3.1.1 Multiple Voltage Generation

SC DC-DC converters transfer the charge extracted from the input supply to the load using only capacitors and switches. When a SC DC-DC converter supplies a certain load voltage \((V_L)\), the maximum attainable efficiency of the converter is set by its topology. Each topology is made in a different combination of flying capacitors and switches as shown in Fig. 3.1 \([7, 13, 54, 67, 69, 70]\). Based on the level of no-load voltages \((V_{NL})\) \([54]\), the supplied load voltage when the load does not exist (with the infinite load resistance and hence zero load current), the name of each topology is determined. If the \(V_{NL}\) of a certain topology is \(V_{NL}/3\), the name of the topology is 3-to-1 topology.

If 2-to-1 topology as shown in Fig. 3.1(d) is selected for voltage conversion,
the maximum attainable efficiency decreases linearly as the average load voltage ($V_L$) drops below $V_{NL}=2.5V$, when the input voltage ($V_{IN}$) is 5V. This efficiency drop is essentially in the same manner as the linear efficiency drop in linear regulators. In general, the maximum attainable efficiency of a regulated SC DC-DC converter can be written as

$$\eta_{max} = \frac{V_L}{V_{NL}} \times \frac{V_L}{N \cdot V_{IN}}$$ \hspace{1cm} (3.1)$$

$N$ is the topology dependent constant. For 2-to-1 topology, $N$ is 1/2. With five different types of SC step-down topologies from Fig.3.1, the maximum attainable load voltage can be drawn as shown in Fig.3.2.
Figure 3.2: Maximum attainable efficiencies of five different SC DC-DC converter topologies in Fig.3.1 and for the ideal linear regulator with different load voltages while the input supply voltage $V_{IN}$ is 5V.

As shown in Fig.3.2, by employing five different topologies, five different SC DC-DC converter topologies can support five discrete no-load voltage levels, which are the points when the efficiency is 100%. Using five different step-down topologies from Fig.3.1, SC DC-DC converters can efficiently supply different levels of the load voltages ranging from 1V to $<5V$ out of 5V input voltage; at least 20% higher efficiency than the ideal linear regulators from the point when the load voltage is less than the no-load voltage of 4-to-3 topology, which is 3.75V. The intermediate voltages in between the no-load voltages of each topology can then be obtained by controlling the converter’s output impedance $R_{out}$ as shown in Fig.3.3. With a large number of different topologies, one can
3.1 Core Design

ideally get more than 90\% efficiency (other losses such as gate-driving switching loss, bottom-plate capacitance loss, and control circuit loss are not considered here.) over a wide range of the load voltage. Of course it can be higher than the input voltage or can be a negative polarity of the input voltage with the different topologies as shown in Fig 2.2.

3.1.2 Load Current Driving Capability & Output Resistance Analysis

Assuming that 2-to-1 step-down topology in Fig 3.4 supplies a load voltage ($V_L = V_{NL} - \Delta V_L$) in periodic steady-state, where $V_{NL}$ is the no-load voltage and the value is $V_{IN}/2$ for 2-to-1 topology. During phase $\phi 1a$, the energy extracted from the input voltage source ($V_{IN}$) can be defined as (the extracted energy due to the parasitic and bottom-plate capacitors, the gate-oxide capacitors of switches, and the control circuits is not considered here.)
3.1 Core Design

![Figura 3.4: 2-to-1 step-down topology with bottom-plate parasitic capacitor ($\alpha C_{fly}$), where $\alpha$ is the bottom-plate parasitic capacitance ratio.]

\[
E_{EXT(\text{VIN})} = - \int_{\phi_1 a} V_{IN} i(t) dt = V_{IN} \int_{\phi_1 a} C_{fly} \frac{dV_{C_{fly}}(t)}{dt} dt
\]

\[
= C_{fly} V_{IN} [(V_{IN} - V_L) - V_L] = C_{fly} V_{IN} (2V_{NL} - 2V_L) = 2C_{fly} V_{IN} \Delta V_L
\]

\[
E_{EXT(\text{VIN})} = 2C_{fly} V_{IN} \Delta V_L \quad (3.2)
\]

In a similar way, the energy delivered to the load ($V_L$) is derived as

\[
E_{L(\phi_1 a)} = \int_{\phi_1 a} V_L i_{C_{fly}}(t) dt = \int_{\phi_1 a} V_L C_{fly} \frac{dV_{C_{fly}}(t)}{dt} dt
\]

\[
= C_{fly} V_L \int_{\phi_1 a} dV_{C_{fly}}(t) = C_{fly} V_L [(V_{IN} - V_L) - V_L]
\]

\[
= C_{fly} V_L (2V_{NL} - 2V_L) = 2C_{fly} V_L \Delta V_L
\]

\[
E_{L(\phi_1 a)} = 2C_{fly} V_L \Delta V_L \quad (3.3)
\]
3.1 Core Design

During phase $\phi 1b$, the stored energy (charged electrons) in the flying capacitor ($C_{fly}$) is transferred to the load. The transferred energy to the load during phase $\phi 1b$ is the same as the transferred energy to the load during phase $\phi 1a$. Therefore, the total energy transferred to the load during one cycle (period) is

$$E_L(\phi 1a + \phi 1b) = 2E_L(\phi 1a) = 4C_{fly}V_L\Delta V_L$$  \hspace{1cm} (3.4)

The load current driving capability can be determined by

$$I_L = \frac{E_L}{V_L} \cdot f_{sw} = 4C_{fly}V_Lf_{sw}$$  \hspace{1cm} (3.5)

Eq.3.4 and Eq.3.5 assume that the time constant $R_LC_{fly}$ is small enough relative to $2/f_{sw}$. This condition is often referred to slow switching limit (SSL). With the constant $C_{fly}$ and the heavy load current (small $R_L$), as $f_{sw}$ increases, Eq.3.4 and Eq.3.5 are not valid. This condition is often called fast switching limit (FSL)

$$I_L = 4C_{fly}V_Lf_{sw}k$$  \hspace{1cm} (3.6)

where

$$k = 1 - \frac{1}{1 + e^{-\frac{1}{f_{sw}R_{on}C_{fly}}}}$$

$R_{on}$ is on-resistance of each MOS switch and $k$ is the variable varies between 0 and 1.
and 1. As shown in Eq.3.5 and Eq.3.6, the load current is determined by $C_{fly}$, $R_{on}$, $\Delta V_L$, and $f_{sw}$. Therefore, to deliver a regulated load voltage when the load current changes, the switching frequency ($f_{sw}$), the on-resistance ($R_{on}$) or the flying capacitance ($C_{fly}$) have to be modulated properly. In the following section, several existing control methods will be introduced. In the analogy of the variable resistance of a linear regulator, the output resistance of the SC converter in Fig.3.4 can be modeled as

$$R_{out} = \frac{\Delta V_L}{I_L} = \frac{1}{4kC_{fly}f_{sw}} \quad (3.7)$$

### 3.1.3 Loss Mechanisms

Efficiency of a DC-DC converter is one of the most important considerations for the battery operated portable electronic devices. The overall efficiency ($\eta_{TOTAL}$) of the SC DC-DC converter in Fig.3.4 can be expressed as the ratio between the total energy delivered to the load per cycle ($E_L$) to the sum of the total energy extracted from the input ($E_{TOTAL-EXT(VIN)}$). Therefore, the overall efficiency per cycle can be defined as [54]

$$\eta_{TOTAL} = \frac{E_L}{E_{TOTAL-EXT(VIN)}} = \frac{E_L}{E_{EXT(VIN)} + E_{BP} + E_{SW} + E_{CTRL}} \quad (3.8)$$

where $E_{EXT(VIN)}$ is the energy extracted from the input during one cycle purely
due to the charge transfer to the load. $E_{BP}$ is the energy loss due to charging and discharging bottom-plate capacitors and other parasitic capacitors such as top-plate and drain-to-body/source-to-body junction capacitors. Since the energy loss due to the bottom-plate capacitors is the most dominant than the loss due to other parasitic capacitors, the energy loss due to the bottom-plate capacitors will only be considered as $E_{BP}$ in this thesis. $E_{SW}$ is the gate-drive switching loss of MOS switches. $E_{CTRL}$ is the energy loss due to the control circuit. As explained earlier, if other losses such as $E_{BP}$, $E_{SW}$, and $E_{CTRL}$ are neglected, the maximum attainable efficiency can be written as $V_L/V_{NL}$, which is shown in Eq.3.1.

If the numerator and the denominator of Eq.3.8 are divided by $E_{EXT(VIN)}$ and Eq.3.1 is substituted to Eq.3.8, the following equation can be obtained [54]

$$
\eta_{TOTAL} = \left( \frac{V_L}{V_{NL}} \right) \frac{1}{1 + \frac{E_{BP}}{E_{EXT(VIN)}} + \frac{E_{SW}}{E_{EXT(VIN)}} + \frac{E_{CTRL}}{E_{EXT(VIN)}}} \tag{3.9}
$$

Therefore, in order to maximize the overall efficiency ($\eta_{TOTAL}$) at a certain load voltage ($V_L$), other loss components have to be analyzed and minimized. In the following sub-sections, each energy loss component will be discussed in detail.

### 3.1.3.1 Conduction loss (Charge transfer loss)

As described in the previous section, conduction loss is a fundamental loss which arises from charging/discharging a capacitor through resistive switches. When
3.1 Core Design

the charge flows from the input to the load during $\phi 1a$ or when the stored charge in the flying capacitor flows to the load during $\phi 1b$, some part of charge is dissipated within the switches of the DC-DC converter due to the finite drain-to-source on-resistance of each switch. Considering only the charge transfer conduction loss, the efficiency of 2-to-1 step-down topology in Fig 3.4 can be defined as

$$\eta_{\text{max}} = \frac{E_L(\phi 1a+\phi 1b)}{E_{\text{EXT}}(V_{IN})} = \frac{V_L}{V_{IN}} = \frac{V_{NL} - \Delta V_L}{V_{NL}} \quad (3.10)$$

The load voltage drop ($\Delta V_L$) from no-load voltage ($V_{NL} = 1/(2V_{IN})$) is resulting from the finite output resistance ($R_{out}$) due to the resistances of the switches. Therefore, with the finite output resistance, the maximum attainable efficiency of 2-to-1 topology must be less than the value from Eq 3.10. As the load voltage ($V_L$) drops from the no-load voltage $1/2V_{IN}$, the maximum attainable efficiency decreases linearly in the same manner as a linear regulator.

3.1.3.2 Bottom-plate and parasitic capacitors loss

Energy loss due to the bottom-plate capacitors and other parasitic capacitors (such as top-plate and drain-to-body/source-to-body junction capacitors) is the second dominant efficiency loss, especially when MOS capacitors are used as charge transfer flying capacitors. As explained earlier, since the bottom-plate capacitor loss is more dominant than the other capacitor losses, the energy loss
due to the bottom-plate capacitor will only be considered as $E_{BP}$ in this dissertation. Energy loss due to the bottom-plate capacitors arises during the process when the bottom-plate capacitors are being charged and discharged per every cycle. For MIM capacitors implemented using 2 metals, this bottom-plate parasitic capacitors are formed due to the capacitance between the bottom-plate metal and the substrate. For N-well MOS capacitors, this parasitic capacitors are formed between the N-well and P-substrate due to the reverse biases diode junction capacitors. The bottom-plate capacitance ($C_{BP}$) scales with the capacitor area and can be expressed as $C_{BP} = \alpha C_{fly}$, where $\alpha$ is the technology dependent parameter; $\alpha$ has a different value according to what type of capacitors is used and how they are layouted. Consider the circuit shown in Fig. 3.4 (a). During the phase $\phi 1a$ the bottom-plate capacitor gets charged to $V_L$. In phase $\phi 1b$, the energy stored in the bottom-plate capacitor is lost by connecting it to ground. Therefore, the energy loss per cycle in steady-state due to $C_{BP}$ can be derived as

$$E_{BP\_LOSS(\phi 1a)} = E_{BP\_EXT(VIN)(\phi 1a)} - E_{BP\_Stored(\phi 1a)}$$

$$= \alpha C_{fly}(V_L - 0V)^2 - \frac{1}{2} \alpha C_{fly}(V_L^2 - 0V^2) = \frac{1}{2} \alpha C_{fly}(V_L - 0V)^2$$

$$E_{BP\_LOSS(\phi 2a)} = E_{BP\_Stored(\phi 1a)} = \frac{1}{2} \alpha C_{fly}(V_L - 0V)^2$$
\[ E_{BPLOSS} = E_{BPLOSS(\phi1a)} + E_{BPLOSS(\phi1b)} = \alpha C_{fly} V_L^2 \quad (3.11) \]

3.1.3.3 MOSFET gate-drive switching loss

The energy loss due to switching the gate capacitances of the charge-transfer switches is another significant contributor to the total energy loss. The energy dissipated in the gate capacitors of MOS switches per every cycle can be given by

\[ E_{SW} = \sum_{i=1}^{n} C_{ox}(WL)_t V_{Swing}^2 \quad (3.12) \]

where \( C_{ox} \) is the gate-oxide capacitance per unit area, \( n \) is the number of MOS switches, and \( V_{Swing} \) is the voltage swing of the gate driving voltage. To reduce this switching loss, unnecessary gate driving voltage swing has to be minimized.

In addition, since the switching power is proportional to the switching frequency \( f_{sw} \) and the minimum output resistance is limited to the total series resistance of MOS switches, excessively high switching frequency not only can not increase the load voltage \( (V_L) \), but also decrease the total efficiency.
3.1 Core Design

3.1.3.4 Control circuit loss

For the load voltage regulation, most of DC-DC voltage regulators are requires voltage/current reference circuits [4, 5, 20, 47, 51], which are insensitive to process, supply voltage, and temperature (PVT) variations; error-amplifier; comparator; digital blocks; or oscillators for the references and control circuits. Therefore, the circuit shown in Fig.3.4 basically will be surrounded with some of aforementioned circuit blocks to achieve voltage regulation. Most of these require a constant energy for the operation. Especially, the energy loss due to the control circuits is of specific concern while the converter delivers low load power levels. The energy loss per every switching cycle can be broken into a dynamic and a static manners and is given by

$$E_{CTRL} = C_{CTRL} \cdot V_{Supply(CTRL)}^2 + I_Q V_{Supply(CTRL)} T_{sw}$$  \hspace{1cm} (3.13)$$

where $C_{CTRL}$ is the equivalent capacitance switched in the control circuit per a cycle, $V_{Supply(CTRL)}$ is the supply voltage for the control block, $I_Q$ is the total quiescent current consumed by the control circuitry, and $T_{sw}$ is the average time-period of a switching cycle. Therefore, to minimize the energy loss due to the control circuit, one can minimize the supply voltage for the control block, the quiescent current, or the volume of digital circuit blocks.
3.2 Voltage Regulation Techniques

3.2.1 Pulse Frequency Modulation (PFM) Technique

Pulse frequency modulation (PFM) technique is one of the most popular techniques to regulate the load voltage of the SC DC-DC converter at the desired voltage level against the variations in load current or in input voltage. By employing PFM technique, relatively constant efficiency can be achieved over a wide load current range since the switching, bottom-plate, and control losses scale with the switching frequency ($f_{sw}$). As shown in Eq.3.5 and Eq.3.6 by varying switching frequency depending on the load current variations, $\Delta V_L$ can be maintained to be constant. Fig.3.5(a) shows two of the most popular ways for PFM technique. Fig.3.5(a)-1 shows ring voltage controlled oscillator (VCO) and error amplifier based PFM technique [8] and Fig.3.5(a)-2 shows comparator based PFM technique [29, 55, 56, 71]. Both have their advantages and disadvantages. Ring VCO based PFM technique can effectively generate the uniformly phase shifted switching frequencies for the multi-phase interleaving technique. The number of the phase shifted oscillation frequencies is the same as the number of inverter stages, which is the odd number, and the oscillation frequency ($f_{osc}$) is defined as

$$f_{osc}(=f_{sw}) = \frac{1}{2N \cdot t_d}$$

(3.14)
### 3.2 Voltage Regulation Techniques

**Figure 3.5:** Voltage Regulation Techniques of SC DC-DC Converter (a) Pulse Frequency Modulation (PFM) Techniques and Typical Load Voltage Waveforms (b) Switch Width Modulation (c) Flying Capacitor Modulation
where \( N \) is the number of the inverter stages and \( t_d \) is the time delay between each inverter stage. Since the time delay \( t_d \) is proportional \( C_{load}/I_D \), where \( C_{load} \) is the load capacitance seen at the output of each inverter stage and \( I_D \) is the average drain current of NMOS and PMOS drain currents, by varying \( I_D \) using a current-starved VCO \[43\], the oscillation frequency \( (f_{osc}) \) can be controlled. As shown in Fig.3.5(a), if the inverters are added after each inverter output stage of the ring oscillator, the total number of generable interleaved signals is two times of the number of the inverter stages. With the uniformly phase shifted switching frequency, the interleaved gate-drive signals can be applied to the gates of MOS transistor switches to reduce the output ripple voltage. The basic operation principle of the ring oscillator and error amplifier based PFM technique is as follows. If the load voltage \( (V_{L}(t)) \) decreases, the feedback voltage \( (V_{FB}(t)) \) also decreases proportionally. If \( V_{FB}(t) \) is less than the reference voltage \( (V_{REF}) \), the VCO input voltage \( (V_{FB}(t)) \) increases and the switching frequencies generated from the ring oscillator increases. Therefore, \( V_{L}(t) \) increases until \( V_{FB}(t) \) is equal to \( V_{REF} \). The disadvantages of VCO and error amplifier based PFM technique are as follows. The design of a wide tuning range VCO may be challenging. In addition, this PFM technique relatively consumes more power and area than the clocked comparator based approach and requires a careful frequency compensation technique on the error amplifier to make the closed-loop system stable.
3.2 Voltage Regulation Techniques

On the other hand, dynamic (or clocked) comparator based PFM technique, as shown in Fig.3.5(a)-2, is the simplest existing PFM technique with low-power consumption and low-cost. It generally consists of one fast speed dynamic comparator [30, 31, 32, 33, 37, 46, 60, 63], T-Flipflops(T-FFs), a band-gap voltage reference, and non-overlap clock generators. Dynamic comparator based PFM technique is often called as single boundary hysteretic control (SBHC) [29, 71].

At the rising clock edge, the dynamic comparator compares the scaled output load voltage \( V_{FB}(t) \) to the reference voltage \( V_{REF} \). The comparator outputs logic high if \( V_{FB} \) is larger than \( V_{REF} \) and vice versa. During the reset phase when the clock \( CLK \) is low, the both outputs of the dynamic comparator reset to the supply level (logic high). If one negative edge triggered T-FF is connected to the positive output \( V_{OP} \) of the dynamic comparator, a single PWM gate-drive signal can be generated. The operation principle is as follows. Since the T-FF is negative edge triggered and \( V_{OP} \) is reset to the supply level, if \( V_{FB}(t) \) is less than \( V_{REF} \), the waveform of \( V_{OP} \) will be right hand side in Fig.3.5(a)-2. \( V_{OP} \) is logic high during the evaluation phase (from the rising clock edge before the falling edge of clock signal) of the dynamic comparator and \( V_{OP} \) is logic low during the reset phase. Else if \( V_{FB}(t) \) is larger than \( V_{REF} \), \( V_{OP} \) will be always at logic high until \( V_{FB}(t) \) is less than \( V_{REF} \). In this manner, the feedback voltage \( V_{FB}(t) \) can be regulated at \( V_{REF} \) level; thus, the load voltage can be regulated at the desired level using feedback resistors.
However, the drawback of this approach is the relatively large peak-to-peak output ripple voltage especially at the light load condition especially when a single dynamic comparator and T-FF are used. It is due to the large amount of the charge is transferred to the load through and from the single large flying capacitor at each switching transition. If the flying capacitor is divided into a large number of $N$, where $N$ is the positive integer, and the each flying capacitor transfers $N$ time smaller charge to the load at the $N$ time larger switching transition, ideally the output voltage ripple can be reduced by $N$ while the converter delivers the same load current ($I_L$). This simply can be done by connecting a large number ($N$) of negative-edge triggered D-flipflops in series to make $N$-bit Johnson Counter. However, the maximum possible number of interleaving phases is determined by the speed of the dynamic comparator, logic circuits, and buffers at the specific load current ($I_L$) requirement with a limited flying capacitance.

For example, if the required maximum switching frequency ($f_{sw}$) is 20MHz at the maximum load current and 10 phase interleaved gate-drive signals are required for a small ripple voltage in the load, the clock frequency of the dynamic comparator has to be faster than 200MHz. In addition, the regulation accuracy is directly determined by the offset of the comparator. Therefore, fast-speed low-power low-offset clocked comparator is the key of SBHC technique. In addition, as shown in Fig.3.5(a)-2, the peak-to-peak ripple voltage in the load is
3.2 Voltage Regulation Techniques

mostly determined by the size of the load capacitor since when $V_{FB}(t)$ is larger than $V_{REF}$, the discharging time of the load voltage is proportional to $I_L/C_L$; therefore, the typical load voltage waveform is on the left side of the Fig.3.5(a)-2. Therefore, to minimize the peak-to-peak ripple voltage, relatively large load capacitor is required. Furthermore, since the generated kickback noise from the the dynamic comparator makes a large spike on the both positive ($V_{FB}(t)$) and negative ($V_{REF}$) side of the inputs, filter capacitors has to be employed to both input sides for the accurate regulation.

3.2.2 Switch Width Modulation Technique

If the switching frequency is fixed, the transferred charge to the load per every cycle can be controlled by varying the flying capacitance ($C_{fly}$) at the slow switching limit (SSL) or the series resistance of MOS transistor switches ($R_{on}$) at the fast switching limit (FSL) from Eq.3.6 and Eq.3.7. At the fast switching limit (FSL) [61], since the output resistance ($R_{out}$) is dominated by the switch resistance ($R_{on}$), by increasing or decreasing the width of the MOS transistor switches [88] as the load current varies, the amount of charge delivered to the load every cycle can be controlled. However, since the same amount of flying (charge-transfer) capacitance is used over a large range of load, the bottom-plate capacitance losses do not scale with change in load current. This effect leads to the overall efficiency drop if the bottom-plate capacitor exists. In addition,
since the switch resistance is the control parameter, effective regulation with a wide change in load current is difficult to achieve especially when taking process variations in nanometer CMOS processes into account.

### 3.2.3 Flying Capacitor Modulation Technique

To overcome the aforementioned problems, a digital-capacitance-modulation (DCpM) mode of control [56] is introduced, where the regulation is maintained by controlling the amount of capacitance that takes part in the charge transfer process. Since the amount of charge delivered to the load per cycle is proportional to the charge-transfer capacitance at SSL, $\Delta V_L$ in Eq.3.6 can be regulated with the change in load current by varying the amount of capacitance being switched. The advantage with this scheme is that the width of the charge-transfer switches can be made to scale in size as the capacitance scales. This helps in scaling both the bottom-plate and switching losses with change in load current. However, since the flying capacitance is the control parameter, effective regulation with a wide change in load current is difficult to achieve as well.

### 3.3 High-Speed Low-Power Low-Offset Comparator

A high speed continuous-time open-loop comparator requires a large current; therefore, it consumes a large static power. The required current for the high speed continuous-time comparator can be as large as several hundreds mA. In
addition, during the start-up and positive $V_{REF}$ transitions, the continuous-time comparator may need a reset mechanism to assist the output voltage to initially rise above the $V_{ref}$ \[29\]. A latch based dynamic comparator can be used as the comparator. This type of comparators has the advantage of being a completely digital block, thereby circumventing the need for transition regions. A dynamic (or clocked) comparator also eliminates the need for a start-up circuit. As explained earlier, dynamic comparator based PFM feedback control scheme so far has the minimum power and area overhead. The regulation accuracy is directly determined by the offset of the comparator and the maximum deliverable load current is determined by the speed of the comparator. Therefore, fast-speed low-power low-offset clocked comparator is the key for SBHC technique. In section 5, a novel high-speed low-power low-offset dynamic latched comparator is proposed and analyzed.

### 3.4 Summary

Switched capacitor DC-DC converters are a viable alternative to the linear regulators for power delivery in on-chip integrated circuit applications. This chapter has reviewed and summarized the prior arts, different efficiency loss mechanisms, and the general control schemes for a on-chip SC DC-DC converter. Analytical expressions were provided for these loss mechanisms. It was seen that the bottom-plate parasitic loss is a significant contributor to the overall power lost
within the converter. The analysis done in this chapter will be used in the implementation of CMOS switched capacitor DC-DC converters to be described in the next chapter.
Chapter 4

PROPOSED ON-CHIP SWITCHED-CAPACITOR DC-DC CONVERTERS

The prior arts of the recently published on-chip DC-DC converters are reviewed in Chapter 2. Although the linear regulators are cost/area effective and predominant solutions for supplying local power supplies in modern SoCs, the effectiveness degrades dramatically with increasing drop-out voltage between the main power supply and the local power supplies. Therefore, more energy efficient switching alternatives are required. Due to the higher efficiency than linear regulators and easy of integration relative to the on-chip inductor based solutions, on-chip SC based DC-DC converters are considered as promising alternatives and have been receiving increased attention from both academia and industry. In chapter 3, the design challenges in on-chip SC DC-DC converters are presented in terms of multiple voltage generation to efficiently supply different levels of the load voltages, loss mechanisms for the minimal energy losses, and voltage regulation techniques for efficient and stable load regulation.
In this chapter, a new 4-to-3 step-down topology for the proposed on-chip SC DC-DC regulators, the efficiencies of which are less sensitive to increasing bottom-plate capacitance ratio ($\alpha$) than the conventional topologies, is presented. Two different implementations of on-chip SC DC-DC converters are designed using the proposed topology.

4.1 Single Output On-Chip SC DC-DC Converter Design

4.1.1 Core Design

4.1.1.1 Operating principle

Figure 4.1: (a) Conventional 2-to-1 step-down topology (b) Level-shifted non-overlapping gate-driving signals for conventional 2-to1 topology (c) Simplified block diagram of 2-to-1 (step-down) topology (d) Proposed 4-to-3 (step-down) topology
4.1 Single Output On-Chip SC DC-DC Converter Design

In general, SC DC-DC converter consists of capacitors and switches, which are driven by two non-overlapping clock signals. The clock signals are set as close as 50% duty cycle with a minimal dead-time (NMOS and PMOS switches are never closed at the same time to prevent the shoot-through current loss) for the maximum efficiency and the maximum charge transfer to the load. Fig 4.1(a) and Fig 4.1(b) respectively show the conventional 2-to-1 topology and its low-swing gate-driving signals, which are generated from the level-shifters followed by the non-overlapping clock generators, which will be shown in Fig 4.6 to minimized the switching loss. To present the loss due to bottom-plate parasitic capacitors, a bottom-plate parasitic capacitor is modeled as $\alpha C_{fly}$, where $C_{fly}$ is the actual capacitance of a flying capacitor and $\alpha$ is the process and layout dependent parameter. For convenience, Fig 4.1(a) can be symbolized as the one shown in Fig 4.1(c), which has two input terminals and one output terminal.

Assuming that 1) all MOS switches have the same on-resistance of $R_{on}$, 2) the time durations of \textit{phase1} and \textit{phase2} are the same with the minimal dead time, and 3) the time constant $(R_L + 2R_{on})C_{fly}$ is much larger than $1/(2f_{sw})$, the average load voltage ($V_L'$) in Fig 4.1(a) and (c), is defined as the average voltage between two input voltages ($=(V_{IN}+0V)/2=V_{IN}/2$) minus $\Delta V_L'$, since the average voltage across the flying capacitor ($C_{fly}$) is constant at $V_{IN}/2$ in steady-state. $\Delta V_L'$ results from the conduction loss and can be given by

$$\Delta V_L = (1 - \frac{R_L}{R_L + 2R_{on}})V_{NL}$$  \hspace{1cm} (4.1)
As shown in Eq. 4.1, if the MOS switches have zero on-resistance, $\Delta V_L'$ becomes zero; therefore, no conduction loss exists and the average load voltage ($V_L$) will be the same as the no-load voltage ($V_{NL} = V_{IN}/2$).

In a similar way, the proposed 4-to-3 topology is created in a combination of two 2-to-1 topologies; one input terminal of the 2-to-1_up block is fed directly from the input voltage source ($V_{IN}$) and the other input terminal is fed out of the output ($V'_L$) of the 2-to-1_dw block. Therefore, the generated load voltage $V_L = (V_{IN} + V'_L)/2 - \Delta V_L''$ is the average value of $V_{IN}$ and $V'_L = 1/2 V_{IN} - \Delta V_L'$ minus $\Delta V_L''$. $\Delta V_L''$ and $\Delta V_L'$ represent the voltage difference between the delivered load voltages when there is load and there is no load. Again, $\Delta V_L''$ and $\Delta V_L'$ arise from the conduction loss and they limit the maximum attainable efficiency to $\eta_{lin} = V'_L/(1/2 V_{IN})$ for 2-to-1_dw and $\eta_{lin} = V_L/\{(V_{IN} + V'_L)/2\}$ for 2-to-1_up.

Fig. 4.2(a) shows the transistor level implementations of the 2-to-1_dw(up) blocks, and Fig. 4.2(a) shows the gate-driving signals. Since the gate-oxide breakdown voltage of 5V CMOS transistors in 0.35$\mu$m BCDMOS technology is 5.5V, all switches can withstand any voltage levels between ground (0V) and input (5V). All the gate driving signals in Fig.4.2(b) are generated from the level shifters and the non-overlapping clock generators, which will be shown in Fig.4.6, to minimize the switching loss and shoot-through current loss. The NMOS transistors (Mn1, Mn3, and Mn4) in Fig.4.2(a) are implemented by means of
4.1 Single Output On-Chip SC DC-DC Converter Design

Figure 4.2: Transistor level implementation of one-phase of 4-to-3 converter core; (a) 2-to-1 \( \phi_{1a\_dw} \) and 2-to-1 \( \phi_{1a\_up} \) (b) One of 10 phases of level shifted non-overlapping gate-driving signals.

4.1.1.2 Charge Transfer and Loss Mechanisms

2-way interleaved structure of the proposed SC DC-DC converter, as shown Fig.4.3(a), is used for simplicity of the analysis. For the gate driving signals, \( \phi_{1a} \) (\( \phi_{1b} \)) and \( \phi_{2a} \) (\( \phi_{2b} \)) are 180° out of phase signals while \( \phi_{1a} \) (\( \phi_{2b} \)) and \( \phi_{1b} \) (\( \phi_{2b} \)) represent non-overlapping clock signals, which are shown in Fig.4.2(b). Fig.4.3(b) represents the equivalent circuit during every half period (phase1 and phase2) of the switching frequency. Assuming that the SC DC-DC converter deliver charge to the loads at the average voltages of \( V_L \) and \( V_L' \), the charge extracted from the input voltage source (\( Q_{EXT(IN)} \)) during every half period of
4.1 Single Output On-Chip SC DC-DC Converter Design

Figure 4.3: (a) 2-way interleaved structure for the proposed 4-to-3 step-down topology (b) Equivalent circuit for Fig.3(a)

the switching frequency (when the MOS transistors which have the gate-driving signals of $\phi_{1a}$ ($\phi_{1b}$) and $\phi_{2b}$ ($\phi_{2a}$) are on) can be derived as

$$Q_{EXT(VIN)} = C_{up}(\Delta V_L'') + C_{dw}(\Delta V_L')$$  \hspace{1cm} (4.2)

Since the total charge delivered to the load ($V_L$) is the sum of the charge transferred from both top flying capacitors ($C_{up}/2$) as shown in Fig.4.3(b), the total charge transferred to the load is given by

$$Q_L = 2C_{up}(\Delta V_L'')$$  \hspace{1cm} (4.3)

Considering only the charge transfer, the efficiency can be defined as the total charge delivered to the load, as derived in Eq.4.3, over the charge extracted from
4.1 Single Output On-Chip SC DC-DC Converter Design

the input voltage source, as derived in Eq.4.2. As it is derived that $C_{dw}\Delta V_L'$ is equal to a half of $C_{up}\Delta V_L''$, which will be derived in Eq.4.6. By substituting Eq.4.6 to Eq.4.2, the efficiency of the proposed 4-to-3 step-down SC DC-DC converter is given by $V_L/(3/4V_{IN}(=V_{NL}))$. It shows the upper limit of the efficiency of all kinds of SC DC-DC converters; in other word, the maximum attainable efficiency decreases as the voltage drop between the no-load voltage ($V_{NL}$) and the average load voltage ($V_L$) increases.

In order to determine the minimum required capacitances for each flying capacitor that satisfy the design requirements ($I_{L(MAX)}=10mA$ and $V_L=3.2V$ at $f_{sw(MAX)}=20MHz$), the load current driving capability of the proposed SC DC-DC converter has to be derived in terms of $C_{fly}$, $\Delta V_L$, and $f_{sw(MAX)}$. From Eq.4.2, Eq.4.3 and Fig.4.3(b), the load current driving capability at a fixed switching frequency ($f_{sw}$) and $\Delta V_L(=\Delta V_L''+1/2\Delta V_L')$ since $\Delta V_L=V_{NL}-V_L$, where $V_{NL}=3/4V_{IN}$ and $V_L=(V_{IN}+V_L')/2-\Delta V_L''$ is given by

$$I_L = 2I_1 = 4C_{up}\Delta V_L''f_{sw} \quad (4.4)$$

$$I_1 = 2I_2 - I_{ctrl} \approx 2I_2 = 4C_{dw}\Delta V_L'f_{sw} \quad (4.5)$$

From Eq.4.4 and Eq.4.5, the relationship between $\Delta V_L''$ and $\Delta V_L'$ is determined by the ratio between $C_{up}$ and $C_{dw}$, which is given by
4.1 Single Output On-Chip SC DC-DC Converter Design

\[
\frac{\Delta V_L''}{\Delta V_L'} = \frac{2C_{dw}}{C_{up}} \tag{4.6}
\]

There is the optimal ratio between \( C_{up} \) and \( C_{dw} \) which yields the maximum load current \( (I_L) \) at a constant \( \Delta V_L, f_{sw}, \) and \( C_{fly} \). Since \( \Delta V_L \) is the summation of \( \Delta V_L'' \) and \( 1/2\Delta V_L' \), using Eq.4.6 \( \Delta V_L'' \) can be express in terms of \( \Delta V_L, C_{up} \) \((= C_{fly} - C_{dw})\) and \( C_{dw} \) as

\[
\Delta V_L'' = \frac{4C_{dw}}{3C_{dw} + C_{fly}} \Delta V_L \tag{4.7}
\]

By substituting Eq.4.7 into Eq.4.4, the load current \( (I_L) \) is given by

\[
I_L = 16\Delta V_L f_{sw} \frac{C_{fly}C_{dw} - C_{dw}^2}{3C_{dw} + C_{fly}} \tag{4.8}
\]

By taking the partial derivative of Eq.4.8 with respect to \( C_{dw} \) and putting it to zero, the maximum load current \( (I_L(\text{MAX})) \) is obtained when \( C_{fly} \) is three times of \( C_{dw} \). Therefore, the optimal ratio between \( C_{up} \) and \( C_{dw} \), which yields the maximum load current \( (I_L) \) at a constant \( \Delta V_L, f_{sw}, \) and \( C_{fly} \) \((= C_{up} + C_{dw})\), is given by \( C_{up} = 2C_{dw} \). Therefore, Eq.4.8 can be rewritten as

\[
I_L(\text{MAX}) = \frac{16}{3} C_{dw} \Delta V_L f_{sw} = \frac{8}{3} C_{up} \Delta V_L f_{sw} = \frac{16}{9} C_{fly} \Delta V_L f_{sw} \tag{4.9}
\]

where \( C_{fly} = C_{up} + C_{dw} \), \( C_{up} = 2C_{dw} \)
From Eq. 4.6, if $C_{up}$ is two times of $C_{dw}$, $\Delta V_L''$ is equal to $\Delta V_L'$. Since our target load voltage is 3.2V, $\Delta V_L$ is determined to be 0.55V ($\Delta V_L=\Delta V_{NL}-V_L$). Therefore, both $\Delta V_L''$ and $\Delta V_L'$ are determined to be about 0.367V, since $\Delta V_L$ is equal to the addition of $\Delta V_L''$ and $1/2\Delta V_L'$. For the given specifications, 1) $\Delta V_L''$ ($=\Delta V_L'$) is 0.367V, 2) the maximum load current ($I_{L(\text{MAX})}$) is 10mA, and 3) the maximum switching frequency ($f_{sw}$) of DCO is about 20MHz, the minimum required $C_{up}$ can be estimated as about 340pF. Considering process-voltage-temperature (PVT) variations, $C_{up}$ of 600pF and $C_{dw}$ of 300pF are chosen. The MOS switches are sized with small margins to make sure the converter be able to deliver 10mA load current to the 3.2V load.

As can be observed from Eq. 4.9, with the fixed values of $\Delta V_L$ and $C_{up}(C_{dw})$, the load current ($I_L$) can be controlled by changing switching frequency ($f_{sw}$). Therefore, with change in load current, the output load voltage can be regulated by means of pulse frequency modulation (PFM). In this design, PFM control scheme is used with 18bit shift register and 18bit DCO, which are designed to be operating in the range of 0.65MHz to 20MHz. Switching loss is the maximum at the heaviest load condition ($I_L=10mA$ and $V_L=3.2V$) and scales down linearly with decreasing the load by means of PFM technique.

Besides the conduction loss, the loss due to the bottom-plate parasitic capacitors is significant especially when on-chip capacitors are used as flying capacitors; thus, it has to be considered. Since MOS capacitors (2.7fF/µm²)
have higher capacitance density than MIM capacitors (1fF/µm²) in BCDMOS 0.35µm technology, only MOS capacitors are used as the flying and load capacitors, and the bottom-plate capacitance ratio (α) is assumed to be 6.5% of an actual capacitance. As shown in Fig.4.3(b), during every half period of the switching frequency, each top bottom-plate capacitor αC_{up}/2 (αC_{dw}/2) in 2-to-1_{up}(dw) is charged to V_L (V_L'), while each bottom bottom-plate capacitor αC_{up}/2 (αC_{dw}/2) is discharged to V_L' (0V). While the charged electrons in the bottom-plate capacitors of the 2-to-1_{dw} block are discharged to ground; all stored charge is dumped into ground, the charged electrons in the bottom-plate capacitors of 2-to-1_{up} block are discharged to the load V_L'. As a result, the energy lost per every cycle due to those bottom plate capacitors can be given by

\[ E_{BP} = αC_{up}(V_L - V_L')^2 + αC_{dw}V_L'^2 \]  (4.10)

Fig.4.4 shows the efficiency drop dependencies due to the increasing bottom-plate parasitic capacitance ratio (α) of the flying capacitors of the proposed 4-to-3 topology and conventional 3-to-2 topology[56]. Both load voltages are regulated at ~85% of the no-load voltages (3.75V for 4-to-3 topology and 3.33V for 3-to-2 topology) while delivering the load current of 10mA (the same amount of flying and load capacitors and the same control scheme and bias circuits are used for the implementation of conventional 3-to-2 SC DC-DC converter). As
4.1 Single Output On-Chip SC DC-DC Converter Design

Figure 4.4: Efficiency of proposed SC DC-DC converter with a different bottom-plate capacitance ratio ($\alpha$) while delivering the load current of 10mA at the load voltage of 3.2V ($C_{up}$=600pF and $C_{dw}$=300pF)

shown in Fig. 4.4 with increasing bottom-plate capacitance ratio ($\alpha$) from 0% to 10% of the flying capacitors, the efficiency of the proposed 4-to-3 topology drops less than 8%, which is 2.25 times less than that of conventional 3-to-2 topology. With the assumption of $\Delta V_L''=\Delta V_L'$, 2-to1_up block has 2 time bigger flying capacitors than 2-to1_dw block. It helps the proposed 4-to-3 topology have less sensitive to the increasing $\alpha$ since the energy lost per every cycle due to the bottom plate capacitors of 2-to1_up block is less than that of 2-to1_dw block as shown in Eq. 4.10. To find the maximum efficiency with respect to different flying capacitor ratio between $C_{up}$ and $C_{dw}$, $C_{up}$ is swept from 450pF to 700pF with the constant $C_{fly}$ ($=C_{up}+C_{dw}$=900pF). As shown in Fig. 4.5, the maximum efficiency of $\sim$71% is obtained when $C_{up}$ is 600pF ($C_{up}$=2$C_{dw}$). At this point, the efficiency is $\sim$2% higher than the efficiency when $C_{up}$ is equal to $C_{dw}$.
(C_{up}=C_{dw}=450\text{pF}).

\begin{figure}[h!]
\centering
\includegraphics[width=0.5\textwidth]{Fig4.5.png}
\caption{Efficiency of proposed SC DC-DC converter with a different C_{up} at a constant C_{fly}=C_{up}+C_{dw}=900\text{pF}}
\end{figure}

4.1.2 Architecture

Fig.4.6 shows the overall architecture of the proposed SC DC-DC converter. The complete system consists of 10 phase 2-to-1_{up}(dw) blocks, 18-bit shift register, 18-bit thermometer code digitally controlled oscillator (DCO), non-overlapping clock generators, level-shifters, 4 dynamic comparators \cite{32}, an internal low-drop output (LDO) voltage regulator and a start-up circuit. The DCO is controlled by an 18-bit thermometer code produced by the shift register. As shown in Fig.4.6, the load voltage is scaled to \( V_x \) with feedback resistors, and four reference voltages (\( V_{ref1-4} \)) are generated from the bandgap reference circuit in section 4.3.1. Four dynamic comparators (\( Comp1-4 \)), which are operated at the
Figure 4.6: Architecture of proposed 10-phase interleaved 4-to-3 step-down switched capacitor DC-DC converter
clock frequency of 9MHz, compare $V_x$ to the four different reference voltages to determine the mode of control. For fast start-up and fast transient response with a large load current transition, 18-bit shift register operates with 9MHz clock frequency if $V_x$ is less than $V_{ref4}$ or larger than $V_{ref1}$. If $V_x$ enters between reference voltage $V_{ref1}$ and $V_{ref4}$, the clock frequency for the 18-bit shift register slows down to 2.25MHz from 9MHz for the stable load voltage regulation; the scaled load voltage ($V_x$) is locked between $V_{ref2}$ and $V_{ref3}$.

![Efficiency Graph](image)

**Figure 4.7:** Efficiency of proposed SC DC-DC converter with change in load voltage while delivering a load current of 10mA

### 4.1.3 Simulation Results

The proposed SC DC-DC converter is designed and simulated using high-voltage 0.35μm BCDMOS technology. MOS capacitors are used for flying capacitors to maximize the power density. Each 2-to-1 up block uses 60pF MOS capacitor (the total capacitance of 600pF for 10 phase) for its flying capacitor while each
4.1 Single Output On-Chip SC DC-DC Converter Design

Figure 4.8: Efficiency of proposed SC DC-DC converter with change in load current while delivering a load voltage of 3V from 5V input supply

Figure 4.9: Transient response of $V_L$ with varying load current $I_L$ (1mA to 10mA and vice versa)
4.1 Single Output On-Chip SC DC-DC Converter Design

2-to-1, dw block uses 30pF MOS capacitor (the total flying capacitance of 300pF for 10 phase). The output buffer capacitor, 400pF is used to reduce the output ripple and to maintain the moderate level of transient response for the load current variations. Fig. 4.7 shows the simulated efficiency with the change in load voltage while delivering a load current of 10mA. The proposed converter provides above 60% efficiency over the load voltage ranges between 2.5V and 3.2V, which is about 10% higher than ideal linear regulator. Fig. 4.8 shows the efficiency with the change in load current ($I_L$) while delivering a load voltage of 3V. The converter maintains high efficiency over a wide range of load current since its load voltage is regulated using pulse frequency modulation (PFM) technique with digitally controller oscillator (DCO) and 18-bit shift register. The control logic blocks including BGR (Bandgap Reference) circuit, bias circuits and feedback resistors consume power less than 0.8mW over the full switching frequency range ($0.65MHz \leq f_{sw} \leq 20MHz$).

Table 4.1 shows the load voltages ($V_L$) and the efficiency [%] variations with process, voltage, and temperature variations. For the process variation, which is provided by the foundry, device mismatches such as threshold voltage ($V_{to}$), current factor ($\beta=\mu_o C_{ox}$), and base-to-emitter voltage ($V_{be(eb)}$) variations are considered. In addition to the provided passive components variation and an intentional 20% capacitance variation (at 3-sigma) in flying capacitors are considered. 3% supply voltage variation at 3-sigma at different temperatures are
Table 4.1: (a) Load voltages ($V_L$) and (b) overall efficiency variations with PVT variations

(a)

<table>
<thead>
<tr>
<th>T=40°</th>
<th>T=20°</th>
<th>T=0°</th>
<th>T=25°</th>
<th>T=50°</th>
<th>T=100°</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ave</td>
<td>3.268</td>
<td>3.270</td>
<td>3.267</td>
<td>3.286</td>
<td>3.276</td>
</tr>
<tr>
<td>Min</td>
<td>3.174</td>
<td>3.212</td>
<td>3.221</td>
<td>3.212</td>
<td>3.194</td>
</tr>
<tr>
<td>Max</td>
<td>3.320</td>
<td>3.323</td>
<td>3.322</td>
<td>3.344</td>
<td>3.398</td>
</tr>
<tr>
<td>1-Sigma</td>
<td>0.046</td>
<td>0.041</td>
<td>0.033</td>
<td>0.041</td>
<td>0.061</td>
</tr>
</tbody>
</table>

(b)

<table>
<thead>
<tr>
<th>Efficiency [%] when $L=1mA$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ave</td>
</tr>
<tr>
<td>Min</td>
</tr>
<tr>
<td>Max</td>
</tr>
<tr>
<td>1-Sigma</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Efficiency [%] when $L=6mA$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ave</td>
</tr>
<tr>
<td>Min</td>
</tr>
<tr>
<td>Max</td>
</tr>
<tr>
<td>1-Sigma</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Efficiency [%] when $L=10mA$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ave</td>
</tr>
<tr>
<td>Min</td>
</tr>
<tr>
<td>Max</td>
</tr>
<tr>
<td>1-Sigma</td>
</tr>
</tbody>
</table>
4.1 Single Output On-Chip SC DC-DC Converter Design

Table 4.2: Comparison with Recently Published SC DC-DC Converters

<table>
<thead>
<tr>
<th>Process (CMOS)</th>
<th>[56]</th>
<th>[68]</th>
<th>[74]</th>
<th>[76]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>1.8V</td>
<td>2.5V</td>
<td>5V</td>
<td>3.4–5V</td>
<td>5V</td>
</tr>
<tr>
<td>Regulated $V_L$</td>
<td>0.8–1V</td>
<td>0.9–1.5V</td>
<td>1V</td>
<td>3.3V</td>
<td>2.8–3.2V</td>
</tr>
<tr>
<td>$C_{df}$</td>
<td>534pF (on-chip) MOS-cap</td>
<td>6.72nF (on-chip)</td>
<td>1.2nF (on-chip)</td>
<td>1μF (off-chip)</td>
<td>2μF (on-chip) MOS-cap</td>
</tr>
<tr>
<td>$C_L$</td>
<td>700pF (on-chip) MOS-cap</td>
<td>470nF (off-chip)</td>
<td>10μF (off-chip)</td>
<td>1μF (off-chip)</td>
<td>40μF (on-chip) MOS-cap</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>30MHz</td>
<td>0.2–1MHz</td>
<td>15MHz</td>
<td>100kHz</td>
<td>0.65–20MHz</td>
</tr>
<tr>
<td>% Ripple @ S.S.</td>
<td>&lt;5%</td>
<td>2.67% with $I_L=5mA$</td>
<td>14.9% with $I_L=10mA$</td>
<td>1.21% with $I_L=7.5mA$</td>
<td>&lt;1%</td>
</tr>
<tr>
<td>Peak $I_L$</td>
<td>≤69%</td>
<td>≤66.7%</td>
<td>31%</td>
<td>≤65%</td>
<td>≤74%</td>
</tr>
<tr>
<td>$P_{out(max)}$</td>
<td>7.2mW</td>
<td>7.5mW</td>
<td>10mW</td>
<td>40.59mW</td>
<td>32mW</td>
</tr>
<tr>
<td>$I_L(max)$</td>
<td>8mA</td>
<td>5mA</td>
<td>10mA</td>
<td>12.3mA</td>
<td>10mA</td>
</tr>
</tbody>
</table>

considered as well. In order to extract the average and 1-sigma variations of the
output load voltage and the efficiency, 100 times of transient Monte Carlo (MC)
simulations are performed at a different temperature. The simulation results
show that the load regulation and the efficiency of the proposed SC DC-DC
converter is robust with PVT variations. Fig 4.9 shows simulated transient re-
response with load current ($I_L$) transition from 1mA to 10mA, and vice versa.
The converter settles within 0.8μs (≤1.2μs) for 1mA (10mA) to 10mA (1mA)
transition.

Comparison with recently published SC DC-DC converters is listed in Ta-
Table 4.2. Since the proposed SC DC-DC converter design uses only on-chip ca-
pacitors, it saves the area required for on-chip pads and IC pins for the external
capacitors. At the same time, it minimizes parasitic components such as ESR,
ESL, and ESC, which may cause large switching noises, resulting from the bond-
ing, packaging, and PCB wiring. In addition, the proposed design can provide
high load current up to 10mA with only 900pF of flying capacitors since it employs the wide range of PFM technique for its load regulation. Furthermore, since the proposed topology is less sensitive to increasing bottom-plate capacitance ratio ($\alpha$), the best peak efficiency (74%) is obtained even though only MOS capacitors ($\alpha=6.5\%$) are used as its flying capacitors. The smallest output ripple voltage ($<1\%$) is present on the load when the load voltage is 3.2V due to the employed 10-phase interleaving technique.

### 4.2 Dual Output On-Chip SC DC-DC Converter Design

#### 4.2.1 Core Design

#### 4.2.1.1 Charge Transfer and Loss Mechanisms

Fig. 4.10(a) shows 2-way interleaved structure, where $\phi 1a$ ($\phi 1b$) and $\phi 2a$ ($\phi 2b$) are 180° out of phase signals while $\phi 1a$ ($\phi 2b$) and $\phi 1b$ ($\phi 2b$) represent non-overlapping clock signals as shown in Fig. 4.2(b). Fig. 4.10(b) represents equivalent circuit during every half cycle of the clock. Assuming that the SC DC-DC converter deliver charges to the loads at DC voltage $V_L$ and $V_L'$, the charge extracted from the input voltage source ($Q_{EXT(IN)}$) during every half cycle of the clock ($\phi 1a$ and $\phi 2b$ are on) can be derived as

$$Q_{EXT(VIN)} = C_{up}(\Delta V_L'') + C_{dw}(\Delta V_L')$$  \hspace{1cm} (4.11)
4.2 Dual Output On-Chip SC DC-DC Converter Design

\[ V_L = \left( \frac{4}{5} V_{IN} - \frac{1}{2} \Delta V_L \right) - \Delta V_L \]
\[ V_L' = \frac{1}{2} V_{IN} - \Delta V_L' \]

**Figure 4.10:** (a) 2-way interleaved structure for the proposed dual output topology which provides voltages of \( V_L' (=2.2\,V) \) and \( V_L (=3.2\,V) \) out of \( V_{IN} (=5V) \) input. (b) Equivalent circuit for Fig.4.10

Since the total charge delivered to the each load (\( V_L \) and \( V_L' \)) is the sum of the charge transferred from both top and bottom flying capacitors \( (C_{up}/2, C_{dw}/2) \) as shown in Fig.4.10(b), the total charge transferred to the load is given by

\[ Q_L + Q_L' \approx 2Q_{EXT(VIN)} \]

\[ \approx 2C_{up} \left\{ \left( 2.5V + \frac{V_L'}{2} \right) - V_L \right\} + 2C_{dw} \left( 2.5V - V_L' \right) \]  \hspace{1cm} (4.12)

Since the efficiency for each output can be defined as \( Q_L V_L/Q_{EXT(up)} V_{IN} \) and \( Q_L' V_L'/Q_{EXT(dw)} V_{IN} \), this again sets the fundamental efficiency limitations...
of \( V_L'/2.5V \) for the \( 2\text{-to-}1\_dw \) and \( V_L/(2.5V+V_L'/2) \) for the \( 2\text{-to-}1\_up \).

Besides of the conduction loss, the loss due to the bottom-plate parasitic capacitor is significant and has to be considered. In our design, MIM capacitors (\( 1fF/\mu m^2 \)) and MOS capacitors (\( 2.7fF/\mu m^2 \)) are used, and the bottom plate capacitance ratios (\( \alpha \)) were assumed 2.5% for MIM capacitors and 6.5% of MOS capacitors. During every half cycle, each top bottom-plate capacitor \( \alpha C_{up}/2 \) (\( \alpha C_{dw}/2 \)) is charged to \( V_L \) (\( V_L' \)), while each bottom bottom-plate capacitor \( \alpha C_{up}/2 \) (\( \alpha C_{dw}/2 \)) is discharged to \( V_L' \) (GND). The charged electrons in the bottom-plate capacitors of the \( 2\text{-to-}1\_dw \) block are discharged to ground; all stored charge is dumped into ground, but for the charged electrons in the bottom-plate capacitor of the \( 2\text{-to-}1\_up \) block are discharged to the load \( V_L' \). As a result, the energy lost every cycle due to those bottom plate capacitors can be given by

\[
E_{BP} = \alpha C_{up}(V_L - V_L')^2 + \alpha C_{dw}(V_L')^2
\]  

(4.13)

Fig 4.11 shows the efficiency drop dependencies due to the increasing bottom-plate parasitic capacitance of flying capacitors used in \( 2\text{-to-}1\_up \) and \( 2\text{-to-}1\_dw \) while either \( \alpha_{up} \) (when \( \alpha_{dw} \) is swept) or \( \alpha_{dw} \) (when \( \alpha_{up} \) is swept) is set to 0%. Simulation results are obtained at its maximum load condition (delivering 8mA of load currents to both outputs) while the average output voltages are being maintained at \( V_L'\approx2.2V \) and \( V_L\approx3.2V \). With increasing \( \alpha_{up} \) (0% to 7%), the
Figure 4.11: Efficiency drop dependencies with respect to increasing bottom-plate parasitic capacitance ratio ($\alpha=0\%$ to 7$\%$); Black (Grey) represents the efficiency drop with increasing $\alpha_{up}$ ($\alpha_{dw}$) while $\alpha_{dw}$ ($\alpha_{up}$) is kept constant at 0$\%$.

total efficiency drops less than 1$\%$, which is six times less than the efficiency drop with increasing $\alpha_{dw}$ (0$\%$ to 7$\%$). 1$\%$ of efficiency drop arises from the loss during the charging phase ($V_{L'}$ to $V_L$) of either of $\alpha_{up}C/2$ capacitor and from the increased $V_{L'}$ due to the transferred charge from $\alpha_{up}C/2$ capacitors as shown in Fig.4.10(a) and Eq.4.13.

Since the overall efficiency is less sensitive to the increasing $\alpha_{up}$ and their larger capacitance density ($2.7fF/\mu m^2$) in 0.35$\mu m$ BCDMOS Technology, MOS capacitors are used for implementing the flying capacitors of the 2-to-1 $up$ while MIM capacitors are used for implementing 2-to-1 $dw$ since they have less bottom-plate capacitance ratio ($\alpha_{dw}$) than MOS capacitors. This trades off with bigger area since MIM capacitors have smaller capacitance density ($1fF/\mu m^2$). The
minimum required capacitances for each flying capacitor that satisfies the design requirements (the maximum load currents \( I_L, I_L' \)) of 8mA are determined based on the load current handling capabilities of the proposed converter. From Eq.4.11,4.12 and Fig.4.10(b), the load current handing capabilities for both output loads at a fixed frequency and \( \Delta V_L, \Delta V_L' \) can be obtained by

\[
I_L = 2I_1 \approx 2Q_L f_{sw} = 4C_{up}\Delta V_L f_{sw}
\]  
(4.14)

\[
I_L' + I_{ctrl} + 0.5I_L = 2I_2 \approx 2Q_L' f_{sw} = 4C_{dw}\Delta V_L' f_{sw}
\]  
(4.15)

\[
I_L' \approx 4C_{dw}\Delta V_L' f_{sw} - 4C_{up}\Delta V_L f_{sw} - I_{ctrl}
\]  
(4.16)

where \( \Delta V_L \) and \( \Delta V_L' \) represent the voltage difference of output voltages when there is load and there is no load as described earlier in this paper. Since our target voltages are 2.2V and 3.2V, from Fig.4.10(a), \( \Delta V_L' \) and \( \Delta V_L \) are determined to be 0.3V and 0.4V, respectively. Since the maximum control current (\( I_{ctrl} \)) required by the control block is 300µA, the required control current is chosen to be 0.5mA with the margin of 200µA. Therefore, the required \( 2I_2 \) in Eq.4.15 is 12.5mA (=8mA+0.5mA+4mA) because both \( I_L \) and \( I_L' \) are maximum output load current in this case and they are predetermined as design goals. For the given specifications (\( \Delta V_L \) is 0.4V, \( \Delta V_L' \) is 0.3V, and the maximum switching frequency is 28MHz), the minimum required \( C_{up} \) and \( C_{dw} \) are
estimated as 178.57pF and 372pF, respectively. In our design, \(C_{up}\) of 240pF and \(C_{dw}\) of 500pF are chosen for the margins for process, voltage, and temperature (PVT) variations. As can be observed from Eq.4.14 and 4.16, with the fixed values of \(\Delta V_L (\Delta V_L')\) and \(C_{up} (C_{dw})\), \(I_L (I_L')\) can be controlled by changing switching frequency \(f_{sw}\). With changing load current, therefore, the output voltage can be regulated by mean of pulse frequency modulation (PFM). In this design, PFM control scheme is used with 18bit shift register and 18bit DCO which are designed to be operating in the range of 1MHz to 28MHz.

4.2.2 Architecture

Fig 4.12 shows the overall architecture of the proposed dual output DC-DC converter. The complete system consists of two 10 phase 2-to-1 blocks, two 18-bit shift register, two 18-bit thermometer code digitally controlled oscillator (DCO), non-overlapping clock generators, level-shifters, 4 dynamic comparators \[32\], a low-drop output (LDO) voltage regulator and a start-up circuit. The DCO is controlled by an 18-bit thermometer code produced by the shift register. Again, as shown in Fig 4.12 the load voltages are scaled to \(V_x\) with feedback resistors, and four reference voltages \((V_{ref1-4})\) are generated from the bandgap reference circuit in section 4.3.1. Four dynamic comparators \((Comp1-4)\) compare \(V_x\) to the four different reference voltages to determine the mode of control. For
Figure 4.12: Architecture of dual output switched capacitor DC-DC converter system
fast start-up and fast transient response with a large load current transition, 18-bit shift register operates with 9MHz clock frequency if \( V_x \) is less than \( V_{ref4} \) or larger than \( V_{ref1} \). If \( V_x \) enters between reference voltage \( V_{ref1} \) and \( V_{ref4} \), the clock frequency for the 18-bit shift register slows down to 2.25MHz from 9MHz for the stable load voltage regulation; the scaled load voltage (\( V_x \)) is locked between \( V_{ref2} \) and \( V_{ref3} \).

![Figure 4.13: Efficiency versus \( I_L \) while \( I'_L \) is varying between 1mA and 8mA](image)

### 4.2.3 Simulation Results

The proposed SC DC-DC converter is designed using high-voltage 0.35\( \mu \)m BCD-MOS technology. Two types of flying capacitors (MIM and MOS capacitors) are used for flying capacitors to maximize the power density at the limited area. Each 2-to-1\(_{up}\) block uses 24pF MOS capacitor (the total capacitance of 240pF for 10 phase) for its flying capacitor to maximize the power density, while each
2-to-1,\textit{dw} block uses 50pF MIM capacitor (the total flying capacitance of 500pF for 10 phase) to minimize the loss due to bottom-plate parasitic capacitance. MOS capacitors are used for the output buffer capacitors (400pF for each) to reduce the output ripple voltages and to maintain the moderate level of transient response for varying load currents. Fig.4.13 shows the simulated efficiency with different load current levels between 1mA and 8mA, while the load voltages are regulated about 2.2V (3.2V) for \( V_{L'} \) (\( V_L \)). The proposed converter achieves 70.0% of the average efficiency in the output power ranges between 5.4mW and 43.2mW and the maximum efficiency (71.4%) is achieved when it delivers the maximum power (43.2mW). The control logic blocks including BGR (Bandgap Reference) circuit and bias circuits consume the power between 0.46mW and 1mW over the operating power transfer ranges. Fig.4.13 shows simulated transient response with load current \( I_L \) transition from 1mA to 8mA, and vice versa.

With the proposed regulation scheme as shown in Fig.4.12, the converter settles within 450ns (1\( \mu \)s) for 1mA (8mA) to 8mA (1mA) transition while 2-to-1,\textit{dw} delivers 8mA of the load current \( I_L' \). Table 4.3 summarizes the percent variations and average recovery times, which is the average times of high to low and low to high load current transitions, of load voltage \( V_L \) (or \( V_{L'} \)) with the step changes in the load current \( I_L' \) (or \( I_L \)) when the other load current \( I_L \) (or \( I_L' \)) is constant. As shown in Table 4.3, the percent variation in \( V_{L'} \) (or \( V_L \)) when
4.2 Dual Output On-Chip SC DC-DC Converter Design

Figure 4.14: Transient response of $V_L$ ($V_L'$) with varying load current $I_L$ (1mA to 8mA and vice versa) while $I_L'=8mA$

the load current $I_L$ (or $I_L'$) varies decreases as the change of load current $I_L$ (or $I_L'$) decreases. In addition, the percent variation in $V_L'$ (or $V_L$) when the load current $I_L$ (or $I_L'$) varies decreases as the other load $V_L$ (or $V_L'$) initially delivers more constant load current $I_L$ (or $I_L'$). As shown in Table 4.3, the worst case average recovery time is 1.8$\mu$s when $I_L'$ varies between 8mA and 1mA while $V_L$ initially delivers the constant load current $I_L$ of 2mA. The interference between two outputs are inevitable, but it is controllable and can be minimized with increasing clock frequency of $Comp1,4_{up(dw)}$ or increasing the load capacitance.

Table 4.4 shows the load voltages ($V_L$ and $V_L'$) and the efficiency [%] variations with process, voltage, and temperature variations. Devices and passive components mismatch (20% variations in flying capacitors at 3-sigma are assumed) and 3% supply voltage variation at 3-sigma at different temperatures.
Table 4.3: Percent variations and average recovery times of load voltage $V_L$ (or $V_{L'}$) with the step changes in the load current (a) $I_L$ (or (b) $I_L'$)

<table>
<thead>
<tr>
<th>$I_L$ Variation</th>
<th>$V_L$ Variation</th>
<th>$V_L$ Variation</th>
<th>$I_L$ Variation</th>
<th>$V_{L'}$ Variation</th>
<th>$V_{L'}$ Variation</th>
<th>$I_{L'}$ Variation</th>
<th>$V_{L'}$ Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>8mA-1mA-8mA</td>
<td>90</td>
<td>12.5</td>
<td>95</td>
<td>50</td>
<td>10</td>
<td>8mA-1mA-8mA</td>
<td>95</td>
</tr>
<tr>
<td>6mA-1mA-6mA</td>
<td>95</td>
<td>6.28</td>
<td>90</td>
<td>85</td>
<td>50</td>
<td>6mA-1mA-6mA</td>
<td>90</td>
</tr>
<tr>
<td>4mA-1mA-4mA</td>
<td>4.09</td>
<td>1.82</td>
<td>3.86</td>
<td>0.57</td>
<td>2.27</td>
<td>4mA-1mA-4mA</td>
<td>4.32</td>
</tr>
<tr>
<td>2mA-1mA-2mA</td>
<td>0.725</td>
<td>0.323</td>
<td>0.684</td>
<td>0.101</td>
<td>0.065</td>
<td>2mA-1mA-2mA</td>
<td>0.8625</td>
</tr>
<tr>
<td>Average</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Average</td>
<td></td>
</tr>
<tr>
<td>Recovery time</td>
<td>0.725</td>
<td>0.323</td>
<td>0.684</td>
<td>0.101</td>
<td>0.065</td>
<td>Recovery time</td>
<td>0.8625</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(a) Varying $I_L$ @ Constant $I_{L'}$ ($V_L=3.2V$ and $V_{L'}=2.2V$)

<table>
<thead>
<tr>
<th>$I_{L'}$ Variation</th>
<th>$V_L$ Variation</th>
<th>$V_L$ Variation</th>
<th>$I_{L'}$ Variation</th>
<th>$V_{L'}$ Variation</th>
<th>$V_{L'}$ Variation</th>
<th>$I_{L'}$ Variation</th>
<th>$V_{L'}$ Variation</th>
</tr>
</thead>
<tbody>
<tr>
<td>8mA-1mA-8mA</td>
<td>95</td>
<td>50</td>
<td>95</td>
<td>50</td>
<td>10</td>
<td>8mA-1mA-8mA</td>
<td>95</td>
</tr>
<tr>
<td>6mA-1mA-6mA</td>
<td>90</td>
<td>85</td>
<td>90</td>
<td>85</td>
<td>50</td>
<td>6mA-1mA-6mA</td>
<td>90</td>
</tr>
<tr>
<td>4mA-1mA-4mA</td>
<td>4.32</td>
<td>2.27</td>
<td>4.32</td>
<td>2.27</td>
<td>10</td>
<td>4mA-1mA-4mA</td>
<td>4.32</td>
</tr>
<tr>
<td>2mA-1mA-2mA</td>
<td>3.86</td>
<td>2.27</td>
<td>3.86</td>
<td>2.27</td>
<td>10</td>
<td>2mA-1mA-2mA</td>
<td>3.86</td>
</tr>
<tr>
<td>Average</td>
<td>0.725</td>
<td>0.323</td>
<td>0.684</td>
<td>0.101</td>
<td>0.065</td>
<td>Average</td>
<td>0.8625</td>
</tr>
<tr>
<td>Recovery time</td>
<td>0.725</td>
<td>0.323</td>
<td>0.684</td>
<td>0.101</td>
<td>0.065</td>
<td>Recovery time</td>
<td>0.8625</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(b) Varying $I_{L'}$ @ Constant $I_L$ ($V_L=3.2V$ and $V_{L'}=2.2V$)

are considered for the PVT variation simulations. 100 times of transient Monte Carlo (MC) simulations are performed to extract the data. The simulation results show that the load regulation and the efficiency of the proposed SC DC-DC converter is robust with PVT variations.

Comparison with recently published SC DC-DC converters designed using 0.35µm CMOS technology is listed in Table 4.5. While other SC DC-DC converters are able to support only one step-down output voltage at a time, proposed converter can support two different voltages at the same time. In addition, since the switching frequency of the proposed converter is regulated digitally over wide
<table>
<thead>
<tr>
<th>Temps</th>
<th>$V_L'$ [V]</th>
<th>$V_L$ [V]</th>
<th>Eff. [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ave</td>
<td>2.230</td>
<td>3.246</td>
<td>69.367</td>
</tr>
<tr>
<td>Min</td>
<td>2.216</td>
<td>3.198</td>
<td>65.438</td>
</tr>
<tr>
<td>1Sigma</td>
<td>0.035</td>
<td>0.049</td>
<td>3.77</td>
</tr>
<tr>
<td>Ave</td>
<td>2.239</td>
<td>3.235</td>
<td>69.089</td>
</tr>
<tr>
<td>Min</td>
<td>2.216</td>
<td>3.198</td>
<td>65.438</td>
</tr>
<tr>
<td>1Sigma</td>
<td>0.035</td>
<td>0.049</td>
<td>3.77</td>
</tr>
<tr>
<td>Ave</td>
<td>2.246</td>
<td>3.333</td>
<td>72.885</td>
</tr>
<tr>
<td>Min</td>
<td>2.214</td>
<td>3.169</td>
<td>64.338</td>
</tr>
<tr>
<td>1Sigma</td>
<td>0.046</td>
<td>0.085</td>
<td>2.72</td>
</tr>
<tr>
<td>Ave</td>
<td>2.238</td>
<td>3.240</td>
<td>72.64</td>
</tr>
<tr>
<td>Min</td>
<td>2.214</td>
<td>3.169</td>
<td>64.338</td>
</tr>
<tr>
<td>1Sigma</td>
<td>0.035</td>
<td>0.073</td>
<td>4.65</td>
</tr>
<tr>
<td>Ave</td>
<td>2.235</td>
<td>3.224</td>
<td>69.68</td>
</tr>
<tr>
<td>Min</td>
<td>2.214</td>
<td>3.169</td>
<td>64.338</td>
</tr>
<tr>
<td>1Sigma</td>
<td>0.035</td>
<td>0.073</td>
<td>4.65</td>
</tr>
</tbody>
</table>
frequency ranges between 1 and 28MHz with different load conditions, it main-
tains higher peak and average efficiency even with less flying and output buffer
capacitors, hence less area.

4.3 Major Sub-Circuits

4.3.1 Bandgap Voltage Reference

![Schematic of the bandgap voltage reference](image)

Table 4.5: Comparison with Recently Published SC DC-DC Converters 2

<table>
<thead>
<tr>
<th></th>
<th>[68]</th>
<th>[74]</th>
<th>[74]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process (CMOS)</strong></td>
<td>0.35μm</td>
<td>0.35μm</td>
<td>0.35μm</td>
<td>0.35μm BCDMOS</td>
</tr>
<tr>
<td><strong>Vin</strong></td>
<td>2.5V</td>
<td>5V</td>
<td>3.4~5V</td>
<td>5V</td>
</tr>
<tr>
<td><strong>Regulated VL</strong></td>
<td>0.9~1.5V</td>
<td>1V</td>
<td>3.3V</td>
<td>3.2V and 2.2V</td>
</tr>
<tr>
<td><strong>Cfly</strong></td>
<td>6.72nF (on-chip)</td>
<td>1.2nF (on-chip)</td>
<td>1uF (off-chip)</td>
<td>C_{fly(up)}=240pF MOS-cap</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C_{fly(down)}=500pF MIM-cap</td>
</tr>
<tr>
<td><strong>CL</strong></td>
<td>470nF (off-chip)</td>
<td>10nF (off-chip)</td>
<td>1uF (off-chip)</td>
<td>400pF (x2) MOS-cap</td>
</tr>
<tr>
<td><strong>fsw</strong></td>
<td>0.2~1MHz</td>
<td>15MHz</td>
<td>100kHz</td>
<td>1~28MHz</td>
</tr>
<tr>
<td><strong>% Ripple @ S.S.</strong></td>
<td>2.67% with (I_L=5)mA</td>
<td>14.9% with (I_L=10)mA</td>
<td>1.21% with (I_L=7.5)mA</td>
<td>&lt;1%</td>
</tr>
<tr>
<td><strong>Peak η</strong></td>
<td>≤66.7%</td>
<td>31%</td>
<td>≤65%</td>
<td>≤71.4%</td>
</tr>
<tr>
<td><strong>Pout(max)</strong></td>
<td>7.5mW</td>
<td>10mW</td>
<td>40.59mW</td>
<td>43.2mW</td>
</tr>
<tr>
<td><strong>IL(max)</strong></td>
<td>5mA</td>
<td>10mA</td>
<td>12.3mA</td>
<td>8mA for both loads ((I_L) and (I_L'))</td>
</tr>
</tbody>
</table>
4.3 Major Sub-Circuits

Since the reference voltage determines the maximum regulation accuracy of
the DC-DC converter, it is one of the most important sub-circuits. The bandgap
voltage reference used in this work is based on [5] since the proposed DC-DC
converter requires five independent reference voltages. The schematic is shown in
Fig.4.15. The diode connected BJT Q1 and Q2 together with the resistor, \( R_1 \),
form a proportional-to-absolute-temperature (PTAT) current generator since
the \( \Delta V_D (= V_{D1} - V_{D2}) \) is a function of thermal voltage \( V_T \) and the \( V_T \) has a
positive temperature coefficient (\( \sim 0.085 \text{mV/}^\circ\text{C} \)). The frequency compensated
operational transconductance amplifier (OTA) shown is used to force the voltage
\( V_{INM} \) and \( V_{INP} \) to be equal. Since transistor M1 and M2 are inverting common-
source amplifiers and the small-signal resistance of Q2 plus \( R_1 \) is larger than the
small signal resistance Q1, the node INP is connected to the positive input side
of OTA for the stable operation [4]. The PTAP current in Fig 4.15 is defined as
\[
I_{PTAT} = \frac{V_T \cdot \ln K}{R_1}
\]  
(4.17)

The currents flowing through the resistors, \( R_2 \), are complementary-to-absolute-
temperature (CTAT) since the diode voltage \( V_{D1} \) has a negative temperature
coefficient (\( \sim 1.6 \text{mV/}^\circ\text{C} \)). The CTAP current in Fig 4.15 is defined as
\[
I_{CTAT} = \frac{V_{D1}(= V_{INM})}{R_2}
\]  
(4.18)
Since PMOS transistor M1, M2, and M3 form a current mirror, the drain currents of them are the same as the addition of $I_{PTAP}$ and $I_{CTAP}$. Therefore, the reference voltage, $V_{ref0}$ is defined as

$$V_{ref0} = R_{Total}(I_{PTAT} + I_{CTAT})$$

$$= R_{Total}\left(\frac{V_T \cdot \ln K}{R_1} + \frac{V_{D1}}{R_2}\right) \quad (4.19)$$

The temperature behavior of the bandgap voltage reference is

$$\frac{\partial V_{ref0}}{\partial T} = \frac{V_T \cdot \ln K}{R_1} \cdot \frac{\partial V_T}{\partial T} + \frac{1}{R_2} \cdot \frac{\partial V_{D1}}{\partial T} \quad (4.20)$$

Assuming that the temperature coefficient of the diode ($V_{D1(D2)}$) is -1.6mV/$\degree C$, the temperature coefficient of the thermal voltage ($V_T$) is +0.0085mV/$\degree C$, and the resistors have zero temperature coefficient, for zero temperature coefficient of $V_{ref0}$, the ratio between $R_1$ and $R_2$ can be defined as

$$\frac{R_2}{R_1} = \frac{1.6}{\ln K \cdot 0.085} \quad (4.21)$$

If the $K$ is chosen as 8, $R_2/R_1$ is 9.41. In this design, poly resistors are used, which have the negative temperature coefficient. The target reference voltages are $V_{ref0}=1.25V$, $V_{ref1}=1.125V$, $V_{ref2}=1.025V$, $V_{ref3}=0.98V$, $V_{ref4}=0.925V$ and the total power consumption in BGR is about 90.8µW. Fig[4.16] is obtained from 100 times of transient Monte-Carlo device mismatch simulation with the
temperature variation and Fig.4.16 shows the obtained reference voltages with respect to the supply voltage variation ($V_{IN}$). The bias voltage (BIAS_P1) for OTA is generated from the current reference circuit, which will explained in next section. The simulation results confirms that the designed bandgap voltage reference is well matched with the targeted specification.

![Graph showing reference voltage variation](image)

**Figure 4.16**: Reference voltage ($V_{ref0}$) variation (Max-Ave-Min) with respect to the temperature variation obtained from 100 times of transient Monte-Carlo device mismatch simulation

### 4.3.2 Current Reference

Reference currents are required to supply tail currents for the error amplifier in BGR, the comparator in start-up circuit, and internal linear regulator. For supply independent biasing, beta-multiplier reference (BMR) circuit, as shown...
4.3 Major Sub-Circuits

Figure 4.17: Reference voltages ($V_{ref0}$-$V_{ref4}$) with respect to the supply voltage variation ($V_{IN}$)

Figure 4.18: Schematic of the current reference
in Fig. 4.18 is used. Since the supply voltage is 5V and the threshold voltage of the transistors are less than 1V, to improve current matching between $I_1$ and $I_2$ and to increase the output resistance, a cascode version of the BMR is selected in this design. Start-up circuit is located on the right-hand part of the circuit to ensure the BMR operate in the desired operating point, rather than at zero current. The size of transistor M1 is $K$ times larger than that of transistor M2. This sizing makes $\beta_{M1} = \mu_n C_{ox} (W/L)_1 = K \cdot \beta_{M2}$, which set $V_{GS2} = V_{GS1} + IR_1$. The drain current ($I_2$) of transistor M2 is defined as

$$I_2 = \frac{2}{R_1^2 \beta_{M2}} \left(1 - \sqrt{\frac{1}{K}}\right)^2$$

To maximize the output voltage swings of the cascode configuration, two additional branches on the left-hand part of the circuit are designed to generate the reference voltages (BIAS_N1 and BIAS_P1), which are approximately $V_{th} + 2V_{OV}$ and $V_{DD} - (V_{th} + 2V_{OV})$. Poly resistor is used to implement $R_1$, which is 25kΩ. The total power consumption is about 38.2µW.

### 4.3.3 Linear Regulator

In order to provide a regulated supply voltage (1.6V) for the control circuits (in the first implementation of the proposed DC-DC converter design) from the intermediate load voltage ($V_L'$) variation between 1.8V and 2.2V, a DC-DC regulator is required. $V_L'$ varies depending on the load voltage ($V_L$) setup,
which can be selected to 2.6V, 2.8V, 3V, or 3.2V. Since the control circuits does not require high level of load current, which is always less than 200µA, a linear regulator is selected to provide 1.6V supply voltage for the control circuits.

Fortunately, since the gate voltage of the pass transistor can be larger than the intermediate load voltage ($V_L'$), NMOS transistor is selected as a pass element. As explained in section 2.1, NMOS pass transistor based linear regulators have several performance advantages such as higher stability, less die area, and better PSR over PMOS pass transistor based linear regulators. As shown in Fig. 4.19, for the high DC gain and stability, a single stage coscode amplifier is selected in this design [4]. It shows a DC gain of 70.17dB and the worst case phase margin of 48.75° at the zero load current with the compensation capacitor $C_{.C}$ of 2pF when the load capacitor is 10pF. The total power consumption about 26.65µW.
4.3.4 Dynamic Comparator

Dynamic latched comparators are crucial circuits for the implementation of the fast and accurate load regulation of a SC DC-DC converter. It is because the offset voltage of the comparator limits the regulation accuracy, the speed of the comparator determines the maximum deliverable load current, the regulation speed, or maximum number of interleaving phase for single boundary hysteretic control, and the power consumption of the comparator degrades the overall efficiency. Therefore, a low-power, low-offset, and high-speed dynamic comparator is of great importance for the implementation of load regulation scheme.

The schematic of the selected design of the low-power, low-offset, and high-speed dynamic comparator [32, 33] is shown in Fig. 4.20. The basic operation principle is as follows. The operation phases are divided by two phase; pre-charge...
(or reset) phase and evaluation (or decision-making) phase. During pre-charge phase ($\text{Clk}=0\text{V}$), $D_i'$ nodes are charged to $V_{DD}$. This make $D_i'$ nodes discharge to ground, and $Out$ nodes and $Sw$ nodes are charged to $V_{DD}$. Evaluation phase starts with the rising clock edge. Once the tail current transistor $M1$ turns on, each $D_i$ node capacitance is discharged from $V_{DD}$ to ground in a different rate proportional to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between $D_i+$ and $D_i-$ nodes. Once either $D_i+$ or $D_i-$ node voltage drops below $V_{DD}-|V_{tp}|$, the inverter pairs ($M18/M16$ and $M19/M17$) invert each $D_i$ node signal into the regenerated (amplified) $D_i'$ node signals. Then the regenerated and different phased $D_i'$ node voltages are relayed to the output-latch stage by $M10$-$M13$. As the regenerated $D_i'$ node voltage is rising from $0\text{V}$ to $V_{DD}$ with a different time interval (or a phase difference which increases with the increasing input voltage difference $\Delta V_{in}$), $M12$ and $M13$ turn on one after another and the output latch starts regenerating the small voltage difference transmitted from $D_i'$ nodes into a full-scale digital level: $Out+$ node outputs logic high ($V_{DD}$) if $D_i+'$ node voltage is rises faster than $D_i-$' node voltage and $Out+$ outputs logic low ($0\text{V}$) otherwise. Once either of Out node voltages drops below $V_{DD}-|V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor $M8$ or $M9$ will turn on. For the detailed analysis, please refer to section 5.

For the initial design, the comparator is designed with the minimum transistor
**Figure 4.21:** Input referred offset voltage before and after optimization from 1000 samples of transient Monte-Carlo Simulation
sizes (1.2µm/0.5µm) using high-voltage 0.35µm BCDMOS technology. For the simulation setup, the supply voltage is 1.6V, the input common-mode voltage is 1V, and the clock frequency is 30MHz. As shown in Fig 4.21, the initial design shows one-sigma offset voltage of 37.48mV, which is unacceptably large for the accurate regulation. After the optimization, the dynamic comparator shows one-sigma offset voltage of 5.39mV at the cost of the increased size, hence the increased power consumption (10.1µW from 5.15µW). The optimized sizes of the transistors are shown in Fig 4.20. The delay of the comparator is measured between 50% of the rising clock edge to 50% of the rising (or falling) output $(V_{out+}(out-))$ edge in this simulation. The average of the rising and falling edge of the output delay is 8.41ps when 10mV of the input differential voltage is applied. It consumes 10.1µW of power when 1.6V of the supply voltage and 30MHz of the clock frequency are used.
Chapter 5

PROPOSED LOW-POWER, LOW-OFFSET, AND HIGH-SPEED CMOS DYNAMIC LATCHED COMPARATOR

5.1 Background

As the fast-speed, low-power, and low-offset comparators are crucial for the implementation of the load regulation circuit for SC DC-DC converters, a novel dynamic latched comparator with offset voltage calibration technique is proposed.

Due to fast-speed, low-power consumption, high-input impedance and full-swing output, CMOS dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. The conventional dynamic latched comparators use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) to convert a small input-voltage difference to a
5.1 Background

full-scale digital level in a short time. However, the accuracy of such comparators is limited by the random offset voltage resulting from the device mismatches such as threshold voltage $V_{th}$, current factor $\beta (=\mu C_{ox} W/L)$, and internal-parasitic/external load capacitance mismatches [24, 50, 53]. Therefore, the offset voltage is one of the most important design parameters in designing dynamic latched comparator.

**Figure 5.1:** Typical block diagram of a high-speed voltage comparator

Conventionally, as shown in Fig. 5.1, a pre-amplifier has been used preceding the regenerative latch stage to reduce the latch offset voltage. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also it reduces the kickback noise [17]. However, the pre-amplifier based comparators suffer from both the large static-power consumption for a large bandwidth and the reduced intrinsic gain with a reduction of the drain-to-source resistance $r_{ds}$ due to the continuous technology scaling [48]. Therefore, for the high-speed low-power CMOS applications, a dynamic comparator without pre-amplifier is highly desirable. This can be realized in
5.2 Prior Arts

terms of a dynamic comparator with digital offset calibration techniques. Recently, dynamic comparators with offset calibration techniques have been proposed \[45, 46, 84\]. However, those approaches show a higher sensitivity of the speed variations and offset voltages to a different input common mode voltage or require a tight timing relationship between clock’s true and complementary phases. Furthermore those conventional approaches cannot drive a large load due to its weak drivability.

The proposed dynamic comparator employed in the SC DC-DC converters in section 4 is designed and simulated using high-voltage 0.35\(\mu m\) BCDMOS technology. The simulation results are summarized in section 4.3.4. In this section, for the comparison with state-of-the-art dynamic comparators designed in higher technologies than 0.35\(\mu m\) CMOS technology, the proposed comparator and its offset calibration circuits are designed and simulated using 90nm PTM technology \[1\]. In addition, the offset voltage analysis and optimized design of the proposed comparator are presented.

5.2 Prior Arts

With the advantages such as fast-speed, ideally zero static-power consumption, high input-impedance and full-swing output, the dynamic latched comparator shown in Fig.5.2(a) has been most widely used \[37, 83\]. However, this comparator has only one tail current transistor M1 which controls the currents flowing
5.2 Prior Arts

through both the differential input pair (M2 and M3) and the latch (M6-M9). Therefore, in order to increase the drive currents of the latch, it is inevitable to size up the transistor M1. If the size of transistor M1 is increased, the drain currents of the both input transistors M2 and M3 will increase during the evaluation phase ($Clk=V_{DD}$). This, in turn, reduces the time duration for which the input transistors operate in the saturation region, because $Di$ nodes discharge from $V_{DD}$ to ground in a very short period. Consequently, lower amplification of the input voltage difference will be made between $Di$ nodes and a small $V_{th}$ mismatch between transistor M6 and M7 can yield a large input-referred offset voltage. In addition, since it shows large variations of speed and offset voltage with a different input common-mode voltage $V_{com}$ [83], it is less attractive in applications that need wide input common-mode ranges such as ADCs [60].

![Figure 5.2:](image)

**Figure 5.2:** (a) Conventional dynamic latched comparator [37, 83] (b) Comparator1 [60] (c) Comparator2 [45]

To circumvent these drawbacks, the comparator with separated differential input-gain stage and output-latch stage shown in Fig.5.2 (b) was introduced in
This stage separation makes this comparator be able to operate at a lower supply voltage ($V_{DD}$) and have a more stable offset voltage and speed over wide input common-mode voltage ($V_{com}$) ranges. However, this comparator requires both $Clk$ and $Clkb$ signals and the highly accurate timing relationship between those clocks is required for its optimal operation. Since the voltage difference formed between $Di$ nodes during the evaluation phase ($Clk = V_{DD}$) is time varying, the speed and offset voltage are affected by the clock skew between $Clk$ and $Clkb$ signals. If a simple inverter is used to generate $Clkb$, $Clk$ should be able to drive an additional inverter (at the cost of increased clock loading) that drives the largest transistor M12 for a small delay. If $Clkb$ is lagging the $Clk$, it results in increased delay. If $Clkb$ is leading the $Clk$, it results in increased power dissipation due to the short circuit current path M12 to M10/M11 though M8/M9.

The comparator from [45] without offset calibration technique is shown in Fig.5.2(c), where the $Clk$ skew problem is resolved by replacing $Clkb$ with $Di$ nodes. As a result, the performance is not affected by clock skew and the clock load is reduced. In addition, the input-referred offset voltage and noise are reduced since this comparator has larger $Di$ nodes capacitance and has double transconductance ($g_m$) at $Di$ nodes. However, these improvements are compromised with the increased delay since the current drivability of the output load is weakened due to the fact that transistor M12 and M13 use $Di$ node.
voltages instead of $Clkb$ signals, which are slow exponential decaying shape. Furthermore, the maximum drive current of each Out node is reduced to half of the single tail-current transistor (M12) in the comparator 1 of Fig.5.2 since M12 is divided into two transistors (M12 and M13) in the comparator 2 of fig5.2.

5.3 Operation Principles of Proposed Comparator

The schematic and simulated waveforms of the proposed comparator [31] are shown in Fig.5.3. The circuit is designed and simulated with HSPICE using 90nm PTM Technology [1] at $V_{DD}=1V$, $f_{clk}=3GHz$, $C_{load}=7fF$, Temp.=$25^\circ C$, and input common-mode voltage $V_{com}$ of 0.6V. The basic structure of the proposed comparator stems from the comparators from [46] and [31]. The proposed comparator provides lower input-referred offset voltage and faster operation at the same area and power consumption while the advantages from the previous works are maintained.

During pre-charge (or reset) phase ($Clk=0V$), both PMOS transistors M4 and M5 turn on and $Di$ nodes’ capacitances are charged to $V_{DD}$, which, in turn, make both NMOS transistor M16 and M17 of the inverter pair on and $Di'$ nodes discharge to ground. Sequentially, PMOS transistor M10, M11, M14 and M15 turn on and $Out$ nodes and $Sw$ nodes are charged up to $V_{DD}$ while both NMOS transistors M12 and M13 are off.
5.3 Operation Principles of Proposed Comparator

During evaluation (decision-making) phase ($Clk=V_{DD}$), each $Di$ node capacitance is discharged from $V_{DD}$ to ground in a different rate proportional to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between $Di+$ and $Di-$ nodes. Once either $Di+$ or $Di-$ node voltage drops below $V_{DD}-|V_{tp}|$, the inverter pairs (M18/M16 and M19/M17) invert each $Di$ node signal into the regenerated (amplified) $Di'$ node signals. Then the regenerated and different phased $Di'$ node voltages are relayed to the output-latch stage by M10-M13. As the regenerated $Di'$ node voltage is rising from 0V to $V_{DD}$ with a different time interval (or a phase difference which increases with the increasing input voltage difference $\Delta V_{in}$), M12 and M13 turn on one after another and the output latch starts regenerating the small voltage difference transmitted from $Di'$ nodes into a full-scale digital level: $Out+$.
5.3 Operation Principles of Proposed Comparator

node outputs logic high \((V_{DD})\) if \(Di^+\) node voltage is rises faster than \(Di^-\) node voltage and \(Out^+\) outputs logic low \((0V)\) otherwise. Once either of Out node voltages drops below \(V_{DD}-|V_{tp}|\), this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on.

![Detailed waveforms and voltage differences](image)

**Figure 5.4:** (i) Detailed waveforms of Fig.5.3(b) (ii) Absolute values of the voltage differences at between \(Di\), \(Di^\prime\), and \(Sw\).

Transistor M14 and M15 are used to reset \(Sw\) nodes to \(V_{DD}\) during pre-charge phase to prevent the pre-charge voltage mismatch between \(Sw\) nodes due to \(V_{th}\) mismatch between transistor M6 and M7 and to increase the voltage gain formed between \(Sw\) nodes during the evaluation phase by increasing the time duration for which transistor M12 and M13 operate in the saturation region.

As shown in Fig.5.4 (i) and (ii), the initial input voltage difference of 5mV is amplified up to 110mV before the transistor pair M6 and M7 in the latch
5.4 Offset Analysis of Proposed Comparator

(M6?M9) turn on. Therefore, the input referred offset voltage resulting from the mismatch between transistor M6 and M7 is attenuated by the voltage gain of \( G_1 \times G_2 \times G_3 = \frac{22 \text{V/V}}{} \); where \( G_1 \) is the voltage gain between \( D_i \) nodes and \( \text{In} \) nodes, \( G_2 \) is the voltage gain between \( D_i' \) nodes and \( D_i \) nodes, and \( G_3 \) is the voltage gain between \( Sw \) nodes and \( D_i' \) nodes. In a similar way, the offset voltage of the output latch stage is attenuated by the gain of \( G_1 \times G_2 \) and the offset voltage resulting from the mismatched inverter pair is attenuated by \( G_1 \).

In summary, the two additional inverters inserted between \( D_i \) and \( D_i' \) nodes enable the proposed comparator to have less input referred offset voltage in the output latch by amplifying (regenerating) the weakened \( D_i \) node signals to \( D_i' \) node signals. The output latch stage of the proposed comparator is the complementary version of the latch stage in the conventional design, which makes the proposed comparator deliver bigger load currents.

5.4 Offset Analysis of Proposed Comparator

The offset voltage of the comparator results from the device mismatches, and the offset voltage of the proposed comparator can be expressed as

\[
V_{OS\_Total} = \sqrt{V_{OS\_Diff\_Input}^2 + \frac{1}{G_1^2} \cdot V_{OS\_Inv\_Pair}^2 + \frac{1}{G_1^2 \cdot G_2^2} \cdot V_{OS\_Output\_Latch}^2}
\]  

(5.1)
where $V_{OS\_Diff\_Input}$, $V_{OS\_Inv\_Pair}$, and $V_{OS\_Output\_Latch}$ are the offset voltages resulting from the mismatched transistor pairs in each stage, respectively. $G1$ is the voltage gain between $Di$ nodes and $In$ nodes, and $G2$ is the voltage gain between $Di'$ nodes and $Di$ nodes.

In order to optimize the comparator in terms of the minimal offset voltage, the offset voltage contributions of each stage have to be verified first. Therefore, all transistors (but the inverter pairs) are designed to have the same aspect ratio of $W/L=1\mu m/0.1\mu m$. In order for the inverter pair to have the proper gain and correct functionality, PMOS transistors of the inverter pair are designed three times larger than NMOS transistors ($Wp/Wn=1.5\mu m/0.5\mu m$). To simulate 1-sigma offset voltages for each stage, the random mismatch in threshold voltage $V_{th}$ and current factor $\beta (=\mu Cox W/L)$ for each transistor pair are modeled as follows \[53\],

$$
\sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}}, \quad \sigma_{\beta} = \frac{A_{\beta}}{\sqrt{WL}} \quad \text{where } W, L \text{ are in } \mu m 
$$

where $A_{V_{th}}$ and $A_{\beta}$ are process dependent parameters and are assumed to be $4.5mV\cdot\mu m$ and $1\%\cdot\mu m$, respectively in this mismatch analysis. As shown in Fig\[5.5\] (in grey), the input referred offset voltages of each stage of the comparator with respect to the different the input common mode voltages are extracted from 100 times of transient Monte-Carlo simulations ($V_{DD}=1V$, $f_{Clk}=3GHz$). As expected, the offset voltage resulting from the mismatched transistor pairs
in the regenerative output-latch stage is the smallest since it is reduced by the gain of \( G1 \times G2 \). The offset voltage from the mismatch between the inverter pair is reduced by the gain of \( G1 \), and it is also small comparing to the offset voltage of the differential input stage.

As a result, the dominant part of the overall input referred offset voltage is caused by the mismatch between the differential input pair transistors. If less than 2mV of 1-sigma offset voltage is required, each stage should have less than 1.2mV of 1-sigma input referred offset voltage, which means the size of the input differential pair (M2/M3) has to be sized up around 140 times larger than the initial size (1\( \mu \text{m} \)). In the same way, other transistors also have to be sized up and the overall power consumption and the area increase considerably. Therefore, the technique to reduce the offset voltage without increasing power and area of the comparator is required and it has to be located between the input differential stage and the inverter pair to maximize the efficiency.

### 5.4.1 Offset Voltage in Differential Input Gain Stage

The differential input stage of the proposed comparator is simplified for offset analysis as shown in Fig.5.5. During evaluation phase (\( Clk=V_{DD} \)), the input differential pair discharges each \( Di \) node voltage from \( V_{DD} \) down to 0V with a different time rate proportional to each input voltage. Assuming \( \lambda=\gamma=0 \) for simplicity, since both transistor M2 and M3 operate in the saturation region
5.4 Offset Analysis of Proposed Comparator

Figure 5.5: Offset voltage contributions of each stage before (Grey) and after (Black) optimization.

Figure 5.6: Simplified schematic of the dynamic differential input gain stage.
between the time \( t_1 \) and \( t_2 \) (\( t_1 \): time at which transistor M1 is just turned on at the rising \( Clk \) edge and transistor M2 and M3 start operating in the saturation region, \( t_2 \): time at which either of transistor M2 or M3 moves out of the saturation region and goes into the linear region), the drain-to-source current of transistor M2 and M3 are constant over \([t_1, t_2]\). Therefore, these currents can be expressed as

\[
C_{Di-} = \frac{dV_{Di-}(t)}{dt} = -I_{D2} \quad C_{Di+} = \frac{dV_{Di+}(t)}{dt} = -I_{D3} \quad (5.3)
\]

Integrating both sides of Eq.5.3 over \([t_1, t]\) and applying the initial condition: \( V_{Di}(t_1) = V_{DD} \), the following equations are obtained,

\[
V_{Di-}(t) = V_{DD} - \frac{I_{D2}}{C_{Di-}} t \quad V_{Di+}(t) = V_{DD} - \frac{I_{D3}}{C_{Di-}} t \quad (5.4)
\]

Then the dynamic voltage gain formed from inputs to \( Di \) nodes can be defined as (where \( \Delta V_{Di}(t) = V_{Di-}(t) - V_{Di+}(t) \) and \( \Delta V_{in} = V_{in+} - V_{in-} \))

\[
A_{V_{Di,eff}}(t) = \frac{\Delta V_{Di}(t)}{\Delta V_{in}} \quad (5.5)
\]

Applying the small signal approximation: \( 2(V_{GS2,3} - V_{tn}) >> \Delta V_{in} \) and assuming that \( C_{Di} = C_{Di+} = C_{Di-} \), Eq.5.5 can be expressed as
5.4 Offset Analysis of Proposed Comparator

\[ A_{V, Diff}(t) = -\frac{g_{m2(3)} t}{C_{Di}} \]  \hspace{1cm} (5.6)

where \( g_{m2(3)} = \mu_n C_{ox} \frac{W_{2(3)}}{L} (V_{com} - V_{D1}(t) - V_{t2n(3)}) \)

\[ V_{D1}(t) = (I_{D2} + I_{D3}) \cdot r_{ds1} \approx Const. \]

Eq. 5.6 reveals that as long as the input transistor pair M2 and M3 operates in the saturation region, the dynamic gain \( A_{V, Diff.}(t) \) keeps increasing linearly as time increases. To maximize the gain \( |A_{V, Diff.}(t)| \), \( |g_{m2(3)}/I_{D2(3)}| \) should be maximized because the integration time \( t \) is proportional to \( C_{Di}/I_{D2(3)} \) from Eq. 5.4. Since \( g_m \) in the saturation region is larger than the one in the linear region except for the sub-threshold operation, the input transistor pair M1 and M2 keeps operating in the saturation region longer by reducing the size of transistor M1. However, higher gain is obtained at the cost of the increased delay since the reduced \( I_{D2(3)} \) increases the discharging time of \( Di \) node voltages during the evaluation phase.

The offset voltage \( (V_{OS, Diff.}) \) of the input differential stage can be derived as while the input transistor pair (M2 and M3) is operating in the saturation region.

\[ V_{OS, Diff.} = V_{OS2,3} = V_{GS2} - V_{GS3} \]  \hspace{1cm} (5.7)
5.4 Offset Analysis of Proposed Comparator

\[\frac{1}{2} \sqrt{\frac{2I_D}{\beta}} \left[ -\frac{\Delta I_D}{I_D} + \frac{\Delta \beta}{\beta} \right] - \Delta V_{tn} \quad (5.8)\]

\[\frac{V_{GS2(3)} - V_{tn}}{2} \left[ -\frac{\Delta C_{Di}}{C_{Di}} + \frac{\Delta \beta}{\beta} \right] - \Delta V_{tn} \quad (5.9)\]

Since mismatches are independent statistical variables, the random offset voltage \(V_{OS\_Diff.}\) can be expressed as the variance of Eq 5.9

\[V_{OS\_Diff.}^2 = \Delta V_{tn}^2 + \left( \frac{V_{GS2(3)} - V_{tn}}{2} \right)^2 \left\{ \left( \frac{\Delta C_{Di}}{C_{Di}} \right)^2 + \left( \frac{\Delta \beta}{\beta} \right)^2 \right\} \quad (5.10)\]

Eq 5.10 reveals that (i) the threshold voltage mismatch is directly referred to the offset voltage; (ii) the influence of Di node capacitance mismatch (which consists of the mismatch between the gate capacitances of inverter pair (M18/M16 and M19/M17) and the mismatch between the drain diffusion capacitances of the input transistor pair (M2 and M3)) and the current factor \(\beta\) mismatch on the offset voltage increase with the increasing common mode voltage \(V_{com}\). Since the random device mismatch parameters are related to the size of transistors, the offset voltage can be reduced at the cost of the increasing size of the transistors, hence increasing area and power consumption. Eq 5.10 also presents that the offset voltage can be compensated by controlling the threshold voltages or the drain currents of transistor M2 and M3 and the size of the capacitances at Di nodes.
5.4 Offset Analysis of Proposed Comparator

5.4.2 Offset Voltage in Regenerative Output Latch Stage

![Simplified schematic of the output stage combined with latch when Di' node voltages (V_{Di'}) are reaching around V_{tn12(13)} during evaluation phase.](image)

The inputs of the regenerative output latch stage are at the gates of transistor M10-13 which are connected to Di-' and Di+' nodes. During the evaluation phase (Clk=V_{DD}), each Di-' node voltage rises from 0V to V_{DD} with a different time interval if V_{in+}\neq V_{in-}. Therefore the output latch stage can make a decision whether logic high or low. However, both Di-' node voltages rise up exactly at the same time rate if V_{in+}=V_{in-} and no mismatch exists. This makes both branches of the output latch stage maintain a balanced state [24], which means V_{out+}(t)=V_{out-}(t) during all the transient time. However, if a mismatch exits at the output latch stage, the circuit will be unbalanced and make V_{out+}(t)\neq V_{out-}(t). In order for the circuit to be balanced, a voltage V_{OS,latch} should be applied between the output of the inverter (M18/M16) and Di-' node.
5.4 Offset Analysis of Proposed Comparator

to compensate the mismatch when Di’ nodes rises. To calculate the offset voltage of the output latch stage \((V_{OS,OutputLatch})\), two random mismatches, current factor \(\beta (=\mu C_{ox} W/L)\) and threshold voltage \(V_{th}\), are considered as they are the dominant factors to cause the offset voltage in this analysis.

Although the operation regions of the transistors of the output latch stage vary with time, at the time point when Di’ node voltage is around the threshold voltage of the transistor M12 (M13) \(V_{th12(13)}\), those transistors just turn on and operate in the saturation region. Once \(V_{D12(13)}\) \((Sw)\) node voltages drop down below \(V_{DD}-V_{tn6(7)}\) from \(V_{DD}\), transistor M6 and M7 also start turning on and operate in the saturation region since both their drain and gate voltages are dropping down at the same rate under the balanced condition. At this time, the transistor M10 and M11 operate in the linear region since both \(V_{out+}\) and \(V_{out-}\) are still around \(V_{DD}\), and the effects of the reset transistor M14 and M15 on node \(V_{D12(13)}\) are negligible because they are designed to be much smaller than transistor M12 and M13. The effects of the transistor M8 and M9 on \(Out\pm\) nodes are also ignored because they are in the cut-off region. Therefore, the output latch stage can be simplified as shown in Fig.5.7 for analysis. First, mismatch between transistor M12 and M13 is considered and other pairs are assumed to be perfectly matched. The load capacitance \(C_{L1}\) and \(C_{L2}\) are assumed to include the parasitic capacitances at \(V_{out+}\) nodes and at this time, \(C_{L1}\) and \(C_{L2}\) are assumed to be the same and it is denoted as \(C\).
5.4 Offset Analysis of Proposed Comparator

\[ I_{D12} = I_1 \quad I_{D13} = I_2 = I_1 + \Delta I_1 \]  \hspace{1cm} (5.11)

\[ I_1'' = -C_{L1} \frac{dV_{out-}}{dt} \quad I_2'' = -C_{L2} \frac{dV_{out+}}{dt} \]  \hspace{1cm} (5.12)

Since \( V_{out-} = V_{out+} \) and \( dV_{out-}/dt = dV_{out+}/dt \) in the balanced condition, it is fair to say that

\[ I_1'' = I_2'' \quad \Delta = I'' \]  \hspace{1cm} (5.13)

Also, from KCL and KVL, the followings are obtained

\[ I_1' = I_1 - I_1'' \quad I_2' = I_2 - I_2'' \]  \hspace{1cm} (5.14)

\[ I_1'R_{10} = I_2'R_{11} \]  \hspace{1cm} (5.15)

From Eq.5.11 and Eq.5.13-Eq.5.15

\[ \frac{\Delta I_1}{I_1} = \frac{\Delta I_D}{I_D} = \frac{R_{10} - R_{11}}{R_{10}} \left(1 - \frac{I''}{I_1} \right) \]  \hspace{1cm} (5.16)

From Eq.5.16 and Eq.5.8, the following equation is obtained

\[ V_{\text{OS12,13}}^2 = \left[ \left( \frac{V_{Di'} - V_{\text{tn}}}{2} \right)^2 \left( \frac{\Delta \beta_{12}}{\beta_{12}} \right)^2 + \Delta V_{\text{tn12}}^2 \right] \cdot \left[ 1 + \frac{V_{Di'} - V_{\text{tn12}}}{2(V_{DD} - V_{Di'}) - |V_{tp10}|} \left( \frac{I_1'}{I_1} \right) \right]^{-2} \]  \hspace{1cm} (5.17)
5.4 Offset Analysis of Proposed Comparator

Eq. 5.17 shows the influence of transistor M10 and M11 (which are used as both reset switches and input transistors for the output-latch stage) on the output-latch stage offset voltage $V_{OS_{OutputLatch}}$. In the double-tail comparators from [45, 60], since both the output branches of the output-latch stage are activated by $Clkb$ signal (not by the signals generated from the dynamic pre-amplifier stage), only the pair of the input transistors transfers the gain generated from the previous stage. However, since the proposed comparator and comparator from [73] have two pairs of the input transistors which are linked each other, the offset voltages caused from one pair are compensated by the other input transistor pair. Therefore, the additional term followed by the negative square root term in Eq. 5.17 compensates the former offset voltage term caused by transistor mismatch between M12 and M13. As $V_{D_{1'}}$ increases from $V_{tn}$ to $V_{DD} - |V_{tp}|$ and $I_{1'}/I_1$ increases, $V_{OS_{OutputLatch}}$ is further reduced since the influence of the additional denominator term increases. While larger NMOS transistor M12 and M13 are desirable for low offset and large drive currents, larger PMOS transistor M10 and M11 are also required to have low offset by increasing $I_{1'}/I_1$ ratio. Therefore, there is an optimal ratio between $W_{12(11)}$ and $W_{10(11)}$ at a limited area for minimum offset voltage.

For mismatch between transistor M6 and M7, $\mu_n C_{ox}$ mismatch is considered instead of current factor $\beta$ mismatch to find out the optimal ratio between the width of transistor M6(M7) and M12(M13). From the fact that $I_{D12}=I_{D6}$ and
5.4 Offset Analysis of Proposed Comparator

\[ I_{D13} = I_{D7}, \text{ we have} \]

\[
V_{OS6,7}^2 \approx \frac{W_6}{W_12} \left[ \left( \frac{\Delta \mu_n C_{ox}}{\mu_n C_{ox}} \right)^2 \left( \frac{V_{out} - (+) - V_{D13(12)} - V_{tn6}}{4} \right)^2 + \Delta V_{tn6(7)}^2 \right] \tag{5.18}
\]

Eq.\ref{5.18} shows that the offset voltage caused by the mismatch between the transistor M6 and M7 is a function of the sizes of the transistor M6(M7) and M12(M13). It seems as \( \frac{W_6}{W_{12}} \) increases, \( V_{OS6,7} \) decreases. However, as \( W_6 \) decreases, the random mismatches of \( \Delta \mu_n C_{ox} \) and \( \Delta V_{tn} \) increase. Therefore, there is a particular \( \frac{W_6}{W_{12}} \) ratio that makes an optimum tradeoff between them to have the minimum \( V_{OS6,7} \). In a similar way, the offset voltage \( V_{OS10,11} \) caused by the transistor mismatch between M10 and M11 can be found as follows.

\[
V_{OS10,11}^2 = \left[ (V_{DD} - V_{D1'1} - |V_{tp}|)^2 \left( \frac{\Delta \beta_{10}}{\beta_{10}} \right)^2 + \Delta V_{tp10}^2 \right] \\
\cdot \left[ 1 + \frac{V_{Di'} - V_{tn12}}{2(V_{DD} - V_{Di'} - |V_{tp10}|)} \left( \frac{I_1'}{I_1} \right) \right]^{-2} \tag{5.19}
\]

To calculate the offset voltage resulting from the capacitance mismatches at \textit{Out} nodes (which includes the load capacitance and parasitic capacitance), it is necessary to assume that \( C_{L1} = C \) and \( C_{L2} = C + \Delta C \). Applying this relationship to Eq.\ref{5.12}. 

100
\[ I_1'' = I'' \quad I_2'' = I'' + \Delta I'' \]  

(5.20)

From Eq.5.8, Eq.5.14, Eq.5.15, and Eq.5.20, the following result is obtained.

\[
V_{OS,Cl_{load}}^2 = \left( \frac{V_{Dv'} - V_{tn}}{2} \right)^2 \left( \frac{\Delta C}{C} \right)^2 \left[ 1 + \frac{V_{Dv'} - V_{tn12}}{2(V_{DD} - V_{Dv'} - |V_{tp10}|)} \left( \frac{I'}{I} \right) \right]^{-2}
\]

(5.21)

Eq.5.21 shows that the offset voltage caused by the capacitance mismatch at the output nodes is affected more by the relative capacitance mismatch \( \Delta C/C \) than the absolute capacitance mismatch \( \Delta C \). In addition, Eq.5.21 can be added to Eq.5.17 because it has the same additional term in Eq.5.17.

### 5.5 Offset Calibration Techniques

Based on the offset voltage analysis and Monte-Carlo simulation, the proposed comparator was optimized for the minimal offset voltage. As a result, as shown in Fig.5.5 (in Black), 1-sigma offset voltage was reduced from 12.5mV to 6.5mV at 0.6V of input common mode voltage at the cost of 9% increase in the power dissipation (152\( \mu \)W from 136\( \mu \)W). To further reduce the offset voltage of the proposed comparator without pre-amplifier, digitally controlled capacitive offset voltage compensation technique is developed in this research.
Figure 5.8: (a) Proposed offset voltage calibration technique using $Di$ node capacitance compensation. (b) Offset voltage calibration logic. (c) Signal waveforms of the proposed offset calibration process with the intentional $V_{OS}$ of $+20$ mV and $f_{Clk}=3$ GHz.

As explained in Eq.5.10, the offset voltage can be compensated by controlling $Di$ node capacitance, current or threshold voltage of the differential input pair ($V_{tn(3)}$) [45, 46, 84]. The current calibration technique introduced in [45] exploits additional one pair of NMOS compensation transistors in parallel with the differential input pair and a charge pump. Even though these calibration techniques consume no static power, the calibration process has to be done frequently since the charged voltage in the compensation capacitor (which is connected to the gate of one of NMOS compensation transistor pair) falls down due to the leakage current. In addition, the calibration speed and accuracy are limited by the size of the charging/discharging current sources of charge pump.
5.5 Offset Calibration Techniques

The digital calibration technique from [72] uses additional capacitance arrays to calibrate the offset voltage. Although the calibration resolution and the maximum offset coverage range are limited by the minimum unit capacitance and the number of bits of the capacitance arrays, this technique does not require the calibration refresh process and does not consume static power as well. In addition, the increase of the node capacitance at $Di$ node reduces the input referred noise. However, it slows down the speed of the comparator since $Di$ node voltages in the comparators from [37, 45, 60] are directly linked to the latch stage. The degree of speed degradation is more severe when this technique is applied to the internal nodes ($D\pm$) of the comparator from [45] since those internal node voltages are directly applied to the both input transistor pairs of the second stage. On the other hand, the speed of the proposed comparator is relatively less sensitive to the increase of the $Di$ node capacitance due to the fact that the $Di$ node voltages in the comparator are buffered by the inverter pair.

Fig. 5.8 shows the proposed offset calibration technique using 4-bit capacitor array, which consists of 4-bit shift register, divide-by-two circuit, D flip-flops, and 4-bit capacitor arrays, while the size of the unit capacitance is implemented with PMOS transistors ($W/L=120\text{nm}/100\text{nm}$). The proposed comparator operates above the clock frequency of 3GHz. However, the calibration logic timing needs more time and the calibration logic uses the half clock frequency using the
divide-by-two clock frequency divider. Therefore, the timing requirement for the offset calibration logic is relaxed with an extra clock cycle added after switching on each binary weighted capacitor. Before calibration, as shown in Fig. 5.7(c), the output of the comparator outputs logic low (0V) regardless of the input differential voltage of ±2mV due to the intentional input referred offset voltage of 20mV. After calibration, however, the proposed comparator can distinguish the input differential voltage that is even less than ±2mV. The required calibration time is only about 4ns at $f_{\text{Clk}} = 3\text{GHz}$ and the reset signal (RST) can be simply generated using 3-bit shift register, inverters, switches and an AND gate, which is initiated by the enable signal (En).

**Figure 5.9:** Input referred offset voltage before and after offset calibration obtained from 1000 samples of transient Monte-Carlo
### 5.6 Simulation Result

The proposed comparator with a capacitive offset voltage calibration circuit is designed and simulated in HSPICE using 90nm PTM process. To compare the input referred random offset voltages of the proposed comparator before and after offset calibration, 1000 times of transient Monte-Carlo simulations are performed with the random mismatch model from Eq.5.2 and Eq.5.3, where \( A_{V_{th}} = 4.5 mV \cdot \mu m \) and \( A_{\beta} = 1% \cdot \mu m \), and the total input referred offset voltage was measured by applying slowly varying slope signals to the comparator inputs. As shown in Fig.5.9, 1-sigma offset voltage of 6.03mV was reduced to 1.10mV with switching frequency of 3GHz and the power consumption of 162\( \mu W \) after the offset calibration.

<table>
<thead>
<tr>
<th></th>
<th>[60]</th>
<th>[45]</th>
<th>[46]</th>
<th>[84]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \sigma_{V_{os \ (before \ cal.)}} )</td>
<td>8mV</td>
<td>13.7mV</td>
<td>12.8mV</td>
<td>31.8mV</td>
<td>6.03mV</td>
</tr>
<tr>
<td>( \sigma_{V_{os \ (after \ cal.)}} )</td>
<td>–</td>
<td>1.68mV</td>
<td>3.3mV</td>
<td>4.3mV</td>
<td>1.10mV</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>1GHz</td>
<td>250MHz</td>
<td>500MHz</td>
<td>1.4GHz</td>
<td>3GHz</td>
</tr>
<tr>
<td>[Delay [ps]/log(( \Delta V_{in} ))]</td>
<td>44ps/decade</td>
<td>24.3ps/decade</td>
<td>–</td>
<td>–</td>
<td>17ps/decade</td>
</tr>
<tr>
<td>Power</td>
<td>113( \mu W )</td>
<td>40( \mu W )</td>
<td>39( \mu W )</td>
<td>350( \mu W )</td>
<td>162( \mu W )</td>
</tr>
<tr>
<td></td>
<td>113( \mu W/GHz )</td>
<td>160( \mu W/GHz )</td>
<td>70( \mu W/GHz )</td>
<td>250( \mu W/GHz )</td>
<td>54( \mu W/GHz )</td>
</tr>
<tr>
<td>Process</td>
<td>90nm</td>
<td>90nm</td>
<td>90nm</td>
<td>0.18um</td>
<td>90nm</td>
</tr>
</tbody>
</table>

### Table 5.1: Performance Comparison
6.1 Summary of Contributions

6.1.1 On-Chip Switched Capacitor DC-DC Converter

A new 4-to-3 step-down topology for SC DC-DC converters, which efficiency is less sensitive to increasing bottom-plate capacitance ratio ($\alpha$) than the conventional topologies, is proposed. For the implementations of SC DC-DC converters, only on-chip capacitors (MOS or MIM capacitors) are used as load capacitors and charge-transfer (flying) capacitors to save the number of on-chip pads and IC pins. Therefore, the proposed design reduces the system volume while it minimizes parasitic components such as ESR, ESL, and ESC caused by the bonding, packaging, and PCB wiring. Two different implementations of fully on-chip SC DC-DC converters are presented using proposed 4-to-3 step-down topology as a promising alternative to on-chip linear regulators.

For the first implementation, a new on-chip SC DC-DC converter supports a programmable regulated load voltage ranging from 2.6V to 3.2V out of 5V input
power supply. Only MOS capacitors ($2.7fF/\mu m^2$, $\alpha=6.5\%$) are used as flying capacitors (900pF) and load capacitor (400pF) for the minimum area/cost. To minimize the bottom-plate parasitic capacitor related loss while maximizing the load current driving capability, the proposed 4-to-3 step-down topology utilizes two differently sized conventional 2-to-1 step-down topologies, each of which has a different value of flying capacitor. The proposed converter achieves the peak efficiency of 74% while it delivers the load current between 1mA and 10mA. 10-phase interleaving technique enables the output voltage ripple of the load voltage to be less than 1% at the output load voltage 3.2V.

For the second implementation, a new on-chip SC DC-DC converter that supports two regulated power supply voltages (2.2V and 3.2V) from 5V input supply and delivers the maximum load currents up to 8mA is proposed. The entire converter system uses two conventional 2-to-1 converter blocks. The upper output voltage (3.2V) is generated from the $2$-to-$1_{up}$ converter by means of averaging the 5V input and the generated lower output voltage (2.2V), which is generated from $2$-to-$1_{dw}$ converter by means of averaging the 5V input and the ground. Since $2$-to-$1_{up}$ converter is less sensitive to the bottom-plate parasitic capacitance loss, they are implemented with MOS capacitors, which show higher capacitance density ($2.7fF/\mu m^2$, $\alpha=6.5\%$) than MIM capacitors ($1fF/\mu m^2$, $\alpha=2.5\%$) while they have larger bottom-plate parasitic capacitance ratio ($\alpha$). The proposed implementation saves the area and quiescent currents
for the control blocks since each converter block shares required analog and digital control circuits. Over the wide output power ranges from 5.4mW to 43.2mW, the converter achieves the average efficiency of 70.0% and the peak efficiency of 71.4%. 10-phase interleaving technique enables the output voltage ripples of the both outputs less than 1% (<40mV) of the output voltages when 400pF of output buffer capacitors are used for both outputs.

The two SC DC-DC converters are designed and simulated using high-voltage 0.35µm BCDMOS technology and demonstrate higher than 70% peak efficiencies. This work shows that the on-chip SC DC-DC converters can outperform the linear regulators in terms of efficiency with a little expense of area/cost. Since the merits of the on-chip SC DC-DC converters have be increasing with technology scaling since the gate-oxide capacitance per unit area has been increasing, the on-resistance of MOS transistors per unit area has been decreasing, SC on-chip DC-DC converters are promising alternatives to linear regulators for low power (<50mW) on-chip DC-DC converters in modern portable SoCs.

6.1.2 Low-power, Low-offset, and High-speed CMOS Dynamic Latched Comparator

A new low-offset, low-power and high-speed dynamic latched comparator, which is used as a main component for the fast and precise load regulation of the proposed SC DC-DC converter, is proposed with a detailed offset voltage analysis
and the offset calibration technique. The proposed dynamic comparator uses one phase clock signal for its operation and can drive a larger capacitive load than the conventional one. In addition, as the proposed comparator provides a larger voltage gain up to 22V/V to the regenerative latch, the input-referred offset voltage of the latch is reduced and meta-stability is improved.

For the comparison with state-of-the-art dynamic comparators designed in higher technologies than 0.35µm CMOS technology, the proposed comparator and its offset calibration circuits are designed and simulated using 90nm PTM technology and 1V power supply voltage. It demonstrates up to 24.6% less offset voltage and 30.0% less sensitivity of delay to decreasing input voltage difference (17ps/decade) than the conventional double-tail latched comparator at approximately the same area and power consumption. The offset voltage analysis and optimized design of the proposed comparator are presented. In addition, the offset voltage of the proposed comparator is further reduced from 6.50mV to 1.10mV at 1-sigma with a digitally controlled capacitive offset calibration technique at the operating clock frequency of 3 GHz, and it consumes 54µW/GHz after calibration.
6.2 Future Works

In this dissertation, the SC DC-DC converters using the proposed 4-to-3 step-down topology are implemented. Since the unit cell of the proposed 4-to-3 topology employs two flying capacitors unlike to the conventional 4-to-3 topology, it is easy to transit to other SC topologies such as 3-to-1, 2-to-1, and 3-to-2, those of which employs two flying capacitors for their unit cells. Differently sized flying capacitors ($C_{up}:C_{up}=2:1$) for the unit cell of the proposed topology degrades the maximum load current driving capability for 3-to-1 and 3-to-2 topologies; however it also reduces bottom-plate capacitance losses for those topologies at the same time. Therefore, the high power efficiency over a wide range of voltage regulation using the proposed 4-to-3 topology as an unit cell can be implemented if the bottom-plate parasitic capacitance ratio ($\alpha$) of the on-chip capacitor is large.

The gate-oxide capacitance per unit area ($C_{ox}$) has been increasing and on-resistance per unit area has been decreasing continuously with the technology scaling. With the advanced technology such as 45nm, 32nm or beyond, the required area for the charge-transfer/load capacitors and MOS switches is clearly expected to be reduced when the converter drives the same load current. In addition, the load transient response is expected to be faster. Therefore, the load regulation with a high-bit up-down-hold counter and DCO or low-power
6.2 Future Works

low-power fast-speed ADC and DCO based pulse frequency modulation (PFM) technique can be studied in depth.

With the adoption of the high capacitance density on-chip capacitor which has low parasitics, the overall efficiency is expected to be improved while delivering relatively high output power. For example, SC DC-DC converter for the higher performance processors (\(\sim 1\text{W/mm}^2\)) presented in [11] utilizes \(\sim 200\text{fF/\mu m}^2\) deep trench capacitors and achieves 90% efficiency at a power density of 2.185W/mm\(^2\). SC DC-DC converter design with existing high-density capacitor technologies appears promising in enabling the broad adoption of fully on-chip SC DC-DC converters for middle to high power applications.

Phase interleaving techniques have been widely used to reduce the output ripple voltage. The multiple phase shifted clock signals can be generated from the ring oscillator or T-FFs after the dynamic latched comparator [32]. Although later choice is more stable, consumes lower power/area and shows faster load transient response, the generated multiple phase shifted clock signals can be easily non-periodic and this makes bigger ripple voltage than the ring oscillator based multiple clock generation. Therefore, the method for fast and low power uniformly phase-shifted multiple clock generation can be studied in depth.
Bibliography

[1] 90nm ptm models @ONLINE. 83, 86, 109

[2] Lm2781 ultra-low ripple switched capacitor voltage inverter, national semiconductor. 15

[3] Lm2797/lm2798 120ma high efficiency step-down switched capacitor voltage converter with voltage monitoring, national semiconductor corporation. 17


[22] B.R. Gregoire. A compact switched-capacitor regulated charge pump power


