0.18µm CMOS Low Power ADPLL with a Novel Local Passive Interpolation Time-to-Digital Converter Based on Tri-State Inverter

A Thesis Presented
by

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to
The Department of Electrical and Computer Engineering

in partial fulfillment of the requirements
for the degree of

Master of Science
in
Electrical Engineering

in the field of
Electrical and Computer Engineering

Northeastern University
Boston, Massachusetts

July 2012
Thesis Title: 0.18µm CMOS Low Power ADPLL with a Novel Local Passive Interpolation Time-to-Digital Converter Based on Tri-State Inverter.

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Abstract

The objective of the thesis is to design a novel ADPLL with local passive interpolation time-to-digital (LPI-TDC) based on a tri-state inverter for clock synchronization, clock recovery, and noise and jitter suppression in modern microprocessors. When compared to traditional implementations of PLLs, an all-digital approach turns out to be more suitable for the integrated circuits in order to improve overall system timing issues. In order to accomplish a fast lock of ADPLL, the higher resolution of TDC is needed. An All-Digital Phase-Locked Loop (ADPLL) design is proposed to achieve short locking time using a circuitry of the LPI-TDC based on tri-state inverter. Unlike the conventional LPI-TDC, the proposed LPI-TDC has a tri-state inverter delay cell in only first delay chain. Other delay cells are composed of only normal inverters that have the same delay as tri-state inverter. LPI-TDC based on a tri-state has the advantages in the aspects of higher resolution (1.5 times) and reduced (smaller) number of gates than the conventional LPI-TDC. In addition, the simplified digital loop filter (DLF) is developed and implemented. In the DLF, the shift registers are used to avoid complex multiplication using the approximation method. These facts directly affect to the locking cycles in the proposed ADPLL. The results show that the proposed ADPLL, implemented in 0.18um CMOS technology, needs only 80 clock cycles to lock at 700MHz. The proposed LPI-TDC consumes 13% more power than the conventional LPI-TDC. However, the overall power consumption of the proposed ADPLL is decreased 11% than the ADPLL with the conventional LPI-TDC because of the fast locking time. Average power consumption is 43.47mW at 700MHz with 1.8 supply voltage. The peak-peak jitter is 32.86ps, and the operating frequency range of the proposed ADPLL is 400MHz-860MHz. The proposed ADPLL design is a viable solution for a variety of applications which require precise time intervals.
Acknowledgements

I am deeply grateful to all the people who in one way or another have helped me during my MS thesis. Without the support of others, it would be impossible for me to reach this stage. Especially, I would like to acknowledge Professor Yong-Bin Kim at Northeastern University for his technical assistance in the research and writing of this MS thesis, and his invaluable assistance in conducting research and writing this thesis is greatly appreciated. This academic research experiences have encouraged me for continuing exploring the integrated circuits in the future.

I am also grateful to the members of committee, Dr. Lombardi, Dr. Onabajo, and the Electrical and Computer Engineering Department Head, Dr. Abur for their valuable suggestions and numerous help. Through their instruction, I learned how to pursue research. Lastly, I would like to thank my parents for all that they have done for me. Only with their support can I take the courage to study and succeed across globe. I owe my accomplishments to them.
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Chapter 1

Introduction

The phase-locked loop (PLL) is involved in a wide range of applications that include clock recovery, noise and jitter suppression in communications, clock synchronization in memory interface and high-performance microprocessors, and frequency synthesis for instrumentation and RF receivers [29]. A PLL is a feedback system that causes an output signal to track a reference signal in phase and frequency [4, 21, 25, 26, 29, 51, 55]. When both frequency and phase of these signals are synchronized, it can be said that the PLL is locked.

PLLs have been extensively studied in analogue and digital areas and systems since a wide range of applications that rely on PLLs for proper operation. In a design of PLLs, typically, there are two types of approaches, which are the analogue and digital. In an analogue approach, analog phase/frequency detector (PFD), charge-pump (CP), loop filters (LF) and voltage controlled oscillator
(VCO) are employed in analog PLLs. However, the analog PLLs have problems caused from the analog components. Due to high integration of very-large-scale integration (VLSI) systems, PLLs often operate in a very noisy environment. The digital switching noise coupled through power supply and substrate induces considerable noise into noise-sensitive analog circuits [1, 5, 10, 27, 33, 37, 56].

Many analog approaches are proposed to improve the jitter performance of PLLs, such as choosing a narrow bandwidth or using a low-gain voltage-controlled oscillator (VCO) [56]. However, those analog approaches often result in long lock-in time and increasing design complexity of the PLLs. In addition, the basic analog PLL is at least a second-order system. Its output is susceptible to power supply, process and temperature variations [29]. They needs to overcome the digital switch noise coupled with power through power supply as well as substrate induced noise. Furthermore, the analog PLL is very sensitive to process parameters and must be redesigned if the process is changed or migrates to next generation process [60]. The PLL based on a charge-pump (CP) and voltage-controlled oscillator (VCO) are not quite amendable to integration [43].

Another method is to use digital implementation circuitry to alleviate all problems mentioned above in an analog PLL. Recently, all-digital phase-locked loops (ADPLLs) have become more attractive because they yield better testability, programmability, stability, and portability over different processes [12, 20, 21], and the needs have arisen to reduce cost and power consumption of integrated
circuits with high level of integration in circuitry, especially with the conspicuous growth of the communication systems. The use of high CMOS technologies allow for an unprecedented level of scaling and integration in digital circuitry [43]. To satisfy high integration in circuitry, traditional analog blocks have been replaced with robust digital circuits in development of circuit technologies. Replacing analog part with the robust digital complements, it brings significant advantages of improved programmability, insensitivity to PVT variations and avoiding large analog elements for a digital-intensive architectures. Compared to the traditional analog PLLs, One advantage of a digital implementation is the inherent noise immunity of digital circuits and another advantage of a digital design is its scalability and easy redesign with process changes or shrinks [61]. Furthermore, the ADPLL designed with static CMOS components can easily solve the leakage issue in contrast to analog PLL, and it cooperates well with the other digital circuits on the chip, which makes it used in wide range of microprocessors.

In a digital method, the PLL is composed of phase/frequency detector (PFD), time-to-digital converter (TDC), digital loop filter (DLF) and digitally controlled oscillator (DCO). In the ADPLL, TDC compares the phase error between the reference clock \( F_{\text{ref}} \) and the divided loop clock \( F_{\text{div}} \). Since the performance of ADPLL is affected directly on the resolution of TDC and the linearity of DCO, the careful design works for TDCs and DCOs are necessary. In recent
ADPLL design, efforts have been devoted to increasing the time resolution of the TDC. This is the main issue for the low power and high resolution ADPLL. Moreover, the digital loop filter (DLF) is also an essential part for ADPLL. The digitized phase error is filtered by a digital loop filter (DLF) since one of key characteristics of the ADPLL is the jitter, which is mainly determined by the quantization operation performed within the loop. Although the digital circuit is not sensitive to high frequency noise, it may affect TDC quantization errors. Thus recursive filter is employed to reduce jitter and quantization errors from a high frequency transition noise of ADPLL.

Due to above mentioned reasons, research in the area of digital equivalent implementations circuitry is in great demand now. In this paper, particular, a mathematical description of important factors of LPI-TDC and a novel concept of delay cell suitable for obtaining a fine resolution LPI-TDC for ADPLL are presented. The proposed LPI-TDC based on the cascode tristate inverters, which replace the multiplexers and inverters, achieves a fine resolution when it measures phase error in time-scale with only one inverter delay and reduces the power consumption with a large detection range. The objective of the research presented is to develop low jitter, wide lock range phase-locked and fast acquisition using all-digital techniques.

Chapter 2 first reviews the basic operation involved in phase-locked mechanism and presents overview of various building blocks. Some design aspects of PLL
are explored in Chapter 3, including jitter associated with oscillators [53]. In addition, the frequency step and lock-in time are also discussed in Chapter 3. In chapter 4, the basic principal blocks is explored including various types of time-to-digital converter (TDC), basic theory and blocks of digital loop filter, and digitally controlled oscillator.

Chapter 5 describes the architecture, circuit design and implementation of the proposed ADPLL that has low jitter, fast lock-in time and wide frequency range suitable for microprocessor. The principal blocks of all-digital phase-locked loop are shown in Chapter 3. The conventional phase/frequency detector, charge pump, and RC loop filter are replaced by a local passive interpolation time-digital converter (LPI-TDC) and a digital loop filter. A traditional VCO is also altered with a fully digitally controlled oscillator (DCO), which avoids any analog tuning controls. Particularly, the novel local passive interpolation time-to-digital converter (LPI-TDC) also involved in Chapter 5. The proposed LPI-TDC is distinguished from the conventional LPI-TDC. The proposed LPI-TDC is replaced the conventional delay cell in TDC to the delay cell based on the tristate inverter. ADPLL are discussed in Chapter 6 and applied to the design of ADPLL for frequency synthesis applications. Some experimental results extracted from a test design provide the proof in operation of the ADPLL with LPI-TDC based on tri-state inverter, and the results of Chapter 6 verify robust operations and loss sensitivity to variations in process, temperature and power supply through
the Monte-carlo simulation with the proposed ADPLL discussed in the previous chapters. Chapter 7 summarizes that the conclusions and contributions of this research. Additionally, suggestions are indicated for further investigation and future work in this chapter.
Chapter 2

Review of Phase-Locked Loop (PLL)

2.1 Traditional Phase-Locked Loop

A PLL is used to generate high speed on chip clocks by frequency multiplication, to deskew of clocks to reduce clock skew and attenuate a jitter. A PLL is characterized by the frequency range, jitter, jitter attenuation and lock-time [15]. Traditionally, the PLL is designed by analog approaches [15]. The PLLs are composed of a voltage controlled oscillator (VCO) as clock source, a phase and/or frequency comparator, a loop filter and a frequency divider, which is presented in Figure 2.1. Usually the VCO clock is divided by an integer divider and then compared to a reference clock which is input to the PLL. The
2.1 Traditional Phase-Locked Loop

Figure 2.1: The principal blocks of traditional PLL

compare result as phase and /or frequency difference is converted into a voltage which controls the VCO [15]. This converter normally is a simple low pass filter, also called the loop filter. However, for the analog approaches, the conventional charge-pump based PLLs encounter the problems including capacitor leakage, current mismatch, and limited dynamic range under low supply voltage [54]. In addition, in the SoC era and deep-sub micro technology, to integrate an analog block into a digital system needs to take more design efforts. Furthermore, as the technology changing, the analog blocks need to redesign [15].

The basic operations of a PLL can be divided into three steps. First, the phase detector (PD) catches the phase difference between two inputs and generates an error signal $\varepsilon_\phi$ whose the average value is linearly proportional to the phase difference. A loop filter, especially low pass filter (LPF) is used to suppress the high frequency components of the PD output, allowing the average value to control the VCO frequency. Finally, an oscillator generates an output signal whose frequency is a linear function of the control signal out of the LPF. The
2.1 Traditional Phase-Locked Loop

![ PLL diagram ]

Figure 2.2: PLL in lock (N=2)

generated signal is fed back to the input of the PD and another phase comparison is started until the phase difference achieves a fixed relationship. Some important aspects of the basic PLL needs.

1. Phase is the interesting value in a PLL rather than the voltage and current in general feedback circuits.

2. The difference of the phase information is changed to voltage or current during the different steps of the PLL operation [50].

3. The loop is said to be locked if the phase difference is constant with time. In other words, the frequency is equal between the two compared signals in Figure 2.2 [50, 55].

4. In general, a PLL exhibits non-linear locking behavior.

5. A tiny frequency difference accumulates fast and the phase error grows significantly after several cycles.

6. The PLL output is a periodic signal, while the reference could be periodic, frequency or phase modulated signals, or data.
Chapter 3

Issues for Phase-Locked Loop

3.1 Acquisition

Acquisition process is very important issue for ADPLL since the PLL must support fast entry and exit from the power management [10]. Acquisition is a nonlinear process. If the frequency difference is small and the loop can acquire lock without the cycle in PLLs, it can be considered as phase acquisition where a PLL locks up with just a phase transient. A more difficult analysis is the frequency acquisition, where the reference frequency is initially far away from the VCO free-running frequency. Basically, when the frequency acquisition with no phase difference is done under the lock condition in PLLs, phase-locked loop (PFD) and time-to-digital converter (TDC) generates a coarse and a fine bit to all zeros. Then, the accumulated bits and all zero bits continuously are injected...
into digitally controlled oscillator (DCO). The constant bits generates a constant frequency from DCO.

### 3.2 Period Jitter, Cyclic Jitter and Long-term Jitter

In the data communication systems, the jitter becomes a severe issue since the jitter tolerant budget shrinks with the increase of clock speed [58]. Recently, the devices use the high clock frequencies, thus the timing margin in digital system is important when data is set up and held. Jitters are the timing variations of a set of signal edges from their ideal values, and typically caused by noise or other disturbances in the system.

#### 3.2.1 Period Jitter

Period jitter is the deviation in cycle time of a clock signal with respect to the ideal period over a number of randomly selected cycles [46]. Many publications defined as the time difference between a measured cycle period and the ideal or reference cycle period. Figure 3.1 is a graphical representation of period jitter. The period jitter is measured as peak to peak jitter of by the root of mean square (RMS). The period jitter in this case, especially all-digital phase-locked
3.2 Period Jitter, Cyclic Jitter and Long-term Jitter

Figure 3.1: Period Jitter

Period jitter, is calculated as following equation:

\[ jitter_{period} = T_{non-ideal} - T_{ideal} \]  

(3.1)

Period jitter is useful in calculating timing margins in digital systems. Consider a microprocessor-based system in which the processor requires 1 nS of data setup before clock rise. If the period jitter of the clock is -1.5 nS, then the rising edge of the clock could occur before the data is valid [16, 47]. Hence the microprocessor will be presented with incorrect data, which is illustrated in Figure 3.2.

Similarly, if another microprocessor has a data hold time requirement of 2 nS
but now the clock jitter is +1.5 nS, then the data hold time is effectively reduced to 0.5 nS. Once again, the microprocessor will see incorrect data. This situation is illustrated in Figure 3.3.

Figure 3.3: Data hold time violation

Period jitter measurements are used to calculate timing margins in systems. For example, a microprocessor-based system in which the processor requires 2 ns of a data set-up time. Assume that the clock driving the microprocessor-based system has a maximum of 2.5 ns period jitter. In this example, the rising edge of the clock can occur before the data is valid on the data bus. The processor will then be given incorrect data and the system will not operate correctly.

### 3.2.2 Cyclic Jitter

Cycle to cycle (C2C) jitter is defined as the variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs, which means the time differences between successive periods of a signal. C2C jitter is typically reported as a peak value which defines the maximum
3.2 Period Jitter, Cyclic Jitter and Long-term Jitter

Figure 3.4: Cycle-to-Cycle Jitter

deviation between the rising edges of any two consecutive clocks. This type of jitter specification is commonly used to illustrate the stability of spread spectrum clocks because the period jitter is more sensitive to the frequency spreading feature while C2C jitter is not. C2C jitter is sometimes expressed as a RMS value in ps as well. C2C jitter is illustrated in Figure 3.4.

3.2.3 Long-term Jitter

Long-term jitter measures the maximum change in a clocks output transition from its ideal over a large number of cycles [47]. The actual number of cycles used in the measurement is application dependent [46]. Long-term jitter is illustrated in Figure 3.5. The clock is connected to an oscilloscope that has a time-base feature. The scope is set to trigger on the rising edge of the clock. The long-term
3.3 Operating Frequency Range

jitter is the time difference of the first rising edge and the time delayed edge.

3.3 Operating Frequency Range

Basically, the output frequencies of ADPLL are determined by the reference frequency multiplied by $N$ factor, and $N$ factor depends on the application’s specification. The factors are categorized by the characteristics of ADPLLs. It may have a fixed factors or a programmable ones.

The operating frequency range of the digitally controlled oscillator (DCO) limits the ADPLL’s pulling range \[23\]. Since the ranges of output frequencies are dictated by the target application, the DCO produces the proper frequencies in ranges of the applications. In addition, the output frequencies should be considered with unpredictable effects on target applications such as temperature variation, supply voltage fluctuation and so on.
The Principal of All-Digital Phase-Locked Loop (ADPLL)

4.1 Basic Blocks of ADPLL

The ADPLL is comprised of the phase/frequency detector (PFD), time-to-digital converter (TDC), digital loop filter (DLF) and digitally controlled oscillator (DCO). Figure 4.1 shows the basic block diagram of the all-digital PLL (ADPLL).

Compared with the traditional PLL, the ADPLL has many advantages [54, 57]. First, the ADPLL avoids analogue components and takes the advantage of nanometer-scale CMOS process. Second, the ADPLL is immune to the digital switching noise in a system-on-chip environment because all the signals in
4.2 Time-to-Digital Converter

the ADPLL is digital. Third, the frequency acquisition process is faster in the ADPLL than in CPPLLs [22]. Table 4.1 presents the comparisons between the traditional analogue PLLs and the ADPLL.

<table>
<thead>
<tr>
<th></th>
<th>ADPLLs</th>
<th>analogue PLLs</th>
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</thead>
<tbody>
<tr>
<td>stability</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td>Scalability</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td>System Order</td>
<td>≤1</td>
<td>≥2</td>
</tr>
<tr>
<td>Simplicity</td>
<td>Good</td>
<td>Poor</td>
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<tr>
<td>Tuning</td>
<td>Discrete</td>
<td>Continuous</td>
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<tr>
<td>Lock Tange</td>
<td>Limited</td>
<td>Wide</td>
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<tr>
<td>Noise / jitter</td>
<td>Predictive</td>
<td>Sensitive</td>
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<tr>
<td>Immune to variations in PVT variations</td>
<td>Good</td>
<td>Poor</td>
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4.2 Time-to-Digital Converter

The basic idea of time-to-digital converters (TDC) is to measure time difference with delay elements and to generate the digital words with respect to time difference. The concept of TDC is to sample the outputs of all delay elements
at the same time. The basic operation of a TDC by discussing the shape of a TDC input and output characteristic will be explained.

### 4.2.1 Basic Theory of Time-to-Digital Converters

![Figure 4.2: Principle of counter based TDC](image)

The strategy to provide TDCs as generic mixed-signal building blocks for various applications raises questions about the suitability in ultimately scaled CMOS technologies. Obviously this does not hold for any analog TDC which converts time domain information first into the analog and then to the digital domain. Such TDCs consist mainly of an ADC so have all the impairments of analog circuits in deep sub-micron technologies. The advantages of the time domain can be exploited only if there is no analog conversion step in the time-to-digital conversion. Only if the TDC is clearly dominated by digital circuitry the scaling and robustness arguments hold. The simplest technique to quantize a time interval is to count the cycles of a reference clock fitting into the respective measurement interval. As shown in Figure 4.2, the measurement interval defined
4.2 Time-to-Digital Converter

by the lead and lag signal is completely asynchronous to the reference clock signal. This causes a measurement error $\Delta T_{\text{lead}}$ at the beginning and $\Delta T_{\text{lag}}$ at the end of the time interval. The measurement interval $\Delta T$ can be expressed as

$$\Delta T = N \times T_{CP} + (T_{CP} \Delta T_{lag}) - (T_{CP} \Delta T_{lead})$$

$$= N \times T_{CP} + \varepsilon_T$$

$$\Delta T_{\text{lead}} \in [0; T_{CP}]$$

$$\Delta T_{\text{lag}} \in [0; T_{CP}]$$

$$\varepsilon_T = \Delta T_{\text{lead}} - \Delta T_{\text{lag}} \in [T_{CP}; T_{CP}]$$

where $N$ is the counter value and $T_{CP}$ the reference clock period. $\Delta T_{\text{lead}}$ and $\Delta T_{\text{lag}}$ are the time intervals between the start and the stop signal, respectively, and the next rising edge of the clock signal. The quantization error of the $\Delta T$ measurement is between $-T_{CP}$ and $+T_{CP}$ is limited to twice the period of the clock signal [17].

The measurement accuracy can be increased by a higher clock frequency, however, the higher the clock frequency the higher the power consumption for the generation and the processing of the clock signal.
4.2 Time-to-Digital Converter

4.2.2 Basic Performance of TDCs’ Measurement

The basic input and output behavior of a TDC is given by a quantizer characteristic, which is presented in Figure 4.3. In Figure 4.3, the input time interval is plotted on the $x$-axis and the corresponding digital output word is represented by the $y$-axis. The term quantizer characteristic means that continuous time intervals at the TDC input are mapped to discrete output values. The width of time interval is the absolute resolution $T_{LSB}$ and the corresponding output increment is called 1 LSB. The time-to-digital conversion is not invertible and the input/output behavior. Its mathematical expression is shown in the equation (4.3),

$$T_{in} = B_{out} \cdot T_{LSB} + \varepsilon, \quad 0 \leq \varepsilon < T_{LSB} \quad (4.3)$$
4.2 Time-to-Digital Converter

can be described only by means of the so called quantization error $\epsilon$. For periodic operation, the quantization error which is actually not noise but deterministically dependent on the signal gives rise to harmonic distortion [17].

The time intervals where the steps occur are labeled by $T_B$, where B is the quantization level after the step, $T_{0...01}$ indicates the position of the very first and $B1...11$ of the last step.

A further difference compared to ADCs is the fact that the steps in a TDC characteristic usually occur at the end of a quantization interval whereas for ADC characteristic the steps often lie in the middle of an interval. This is a minor difference that changes the definition of the TDC performance figures slightly.

4.2.3 Sub-Gate Delay Resolution

A basic time-to-digital converter quantizes a time interval in multiples of a gate delay. Thus, the maximum resolution that can be achieved in a certain technology corresponds to one inverter delay. Any TDC that achieves a higher than the technology resolution is said to have a sub-gate delay resolution. The ratio between the technology resolution and the actual resolution is the so called sub-gate delay interpolation factor ($IF$). It can be expressed in the equation

$$IF = \frac{T_{tech}}{T_{LSB}}$$

(4.4)
4.2 Time-to-Digital Converter

TDCs with sub-gate delay resolution use sophisticated circuit techniques to circumvent the limitation of the technology delay. The circuit elements in such structures have another loading and other dimensions than in a basic TDC.

4.2.3.1 Parallel Scaled Delay Element TDC

As in the basic delay-line TDC the stop signal drives all sampling elements, i.e. the corresponding net has a high capacitance so a buffer tree is required [17]. For linearity reasons the skew in this tree has to be minimized. An additional challenge in the TDC based on parallel scaled delay elements is the start signals which has to be connected to all parallel delay elements with a skew smaller than the resolution. Especially for a high dynamic range the balancing of the start and lag nets is challenging which also means that the layout is very critical. For a maximum dynamic range $T_{\text{max}}$, $N = \frac{T_{\text{max}}}{T_{\text{LSB}}}$ parallel branches are required.

This means N delay elements, N flip-flops, and $12 \cdot N(N + 1)$ tuning capacitors. The conversion results are immediately available after the rising edge of the lag signals. The conversion time and latency for the measurement of a time interval $T$ are thus given by

$$T_{\text{conv}}^{\text{parallel}} = T$$

$$T_{\text{latency}}^{\text{parallel}} = 0$$

These times are not dependent on the resolution which makes the embedding of the TDC into a system quite easy. The delays of the buffer trees and the comparator delay cause a constant offset.
4.2 Time-to-Digital Converter

4.2.4 Various Types of TDCs

4.2.4.1 Basic Delay-Line Based TDC

To increase the measurement resolution beyond the maximum feasible clock frequency each counter clock cycle has to be sub-divided asynchronously by a time-to-digital converter. Figure 4.4 illustrates that the counter value then provides a coarse quantization of the measurement interval and the TDC a fine sub-quantization. The subdivision of the reference clock interval, also known as reference clock interpolation, is done by using multiple phases of the reference clock. A ring oscillator consisting of $k$ delay stages for instance generates $k$ equally spaced versions of the clock signal.

An even higher resolution is achieved by delaying the original reference clock in a chain of digital delay elements. The resolution then depends on the delay of the delay elements in the chain. Figure 4.4 illustrates the operating principle of a

![Figure 4.4: Operating principle of a time-to-digital converter](image)
4.2 Time-to-Digital Converter

TDC based on a digital delay-line. The reference clock which is in a more general sense an arbitrary start signal is delayed along the delay-line. On the arrival of the stop signal the delayed versions \( start_i \) of the start signal are sampled in parallel. Either latches or flip-flops can be used as sampling elements. The sampling process freezes the state of the delay-line at the instance where the stop signal occurs. This results in a thermometer code because all delay stages which have been already passed by the start signal give a HIGH value at the outputs of the sampling elements, all delay stages which have not been passed by the start signal yet give a LOW value. The position of the HIGH-LOW transition in this thermometer code indicates how far the start signal could propagate during the time interval spanned by the start and the stop signal. Hence this transition is a measure for the time interval. The number \( N \) of all sampling elements with a HIGH output is related to the measurement interval \( \Delta T \) according to in the equation (4.6),

\[
N = \left\lfloor \frac{\Delta T}{T_{LSB}} \right\rfloor \quad (4.6)
\]

where \( T_{LSB} \) is the delay of a single delay element in the delay-line. The time interval \( \Delta T \) can be calculated from the number of HIGH outputs by the equation (4.7),

\[
\Delta T = NT_{LSB} + \varepsilon \quad (4.7)
\]

where \( \varepsilon \) describes the quantization error that arises as a delay element has
4.2 Time-to-Digital Converter

been either passed by the start signal yet or not. Any intermediate state is not
possible. An implementation of the basic delay-line TDC is shown in Figure 4.5.
The lead signal ripples along a buffer chain that produces the delayed signals
\( \text{start}_i \). Flip-flops are connected to the outputs of the delay elements and sample
the state of the delay-line on the rising edge of the lag signal. The lag signal
drives a high number of flip-flops so a buffer-tree is required. Any skew in this
buffer-tree directly contributes to the non-linearity of the TDC characteristics.
For a correct thermometer code the skew between adjacent branches in this tree
has to be smaller than \( T_{\text{LSB}} \) which makes the design challenging.

4.2.4.2 The Inverter Based TDC

The resolution can be doubled by replacing the buffers by CMOS inverters. The
use of inverters means that both the rising and the falling signal transitions
are used for measurement. Hence the thermometer code at the outputs of the
sampling elements becomes a pseudo thermometer code with alternating ones

![Figure 4.5: Implementation of a basic delay-line based TDC](image-url)
4.2 Time-to-Digital Converter

![Time-to-Digital Converter Diagram]

**Figure 4.6:** Time-to-digital converter based on inverters instead of buffers and zeros. The length of the measurement interval is indicated not by a HIGH-LOW transition but by a phase change of the alternation HIGH-LOW sequence.

### 4.2.4.3 Vernier TDC

A delay-line based TDC that is capable of measuring time intervals with a sub-gate delay resolution is the Vernier TDC. A vernier delay line is well known for its fine time resolution. Figure 4.7 illustrates a simplified Vernier inverter delay line TDC. It employs two inverter/buffer chains with different delays of $\tau_1$ and $\tau_2$, respectively. Time resolution of the Vernier TDC now becomes the delay difference of two delay lines, namely, $\tau_1 - \tau_2$. The delay elements in the first delay-line have a delay $\tau_1$ which is slightly larger than the delay $\tau_2$ of the
4.2 Time-to-Digital Converter

\[ T_{LSB} = \tau_1 - \tau_2 \] (4.8)

4.2.4.4 Local Passive Interpolation TDC

The local passive interpolation TDC achieves a sub-gate delay resolution by subdividing the coarse time interval given by an inverter delay line. The basic principle is similar to the voltage interpolation \[ \text{[41]} \] that is illustrated in Figure 4.8. A new signal \( V_{int,i} \) defined by

\[ V_{int,i} = V_A + a_i \cdot (V_A - V_B), \quad 0 < a_i < 1 \] (4.9)
Figure 4.8: The basic concept of LPI-TDC

The equation (4.9) shows its transition between those of the two generating signals $V_A$ and $V_B$. Together with a comparator latch detecting the crossing of the midlevel, the new signal can be used to quantize the time interval in between $V_A$ and $V_B$. A passive voltage divider as shown in Figure 4.9 can be connected between $V_A$ and $V_B$ to generate the interpolated signals defined by the equation (4.9). Parallel sampling gives a high-resolution thermometer code but at the same low latency and dead-time as for the coarse inverter based TDC. In contrast to the Vernier and pulse shrinking TDC this means that the measurement time does not increase with increasing resolution.

It is worth mentioning that the time interpolation in the LPI-TDC is monotonic by construction. The sequential inverter chain is monotonic even under strong variations due to the causality in the delay line [17]. The interpolated
signals are linear dependent on the signals generated by the inverters. The passivity assures a monotonic local interpolation as an interpolated signal is always smaller than all interpolated signals further above in the interpolated elements and always larger than all signals below. The interpolated signal is exactly parallel to the generating signals $V_A$ and $V_B$ only in the middle of the transition region. Indeed this is sufficient as the comparators detect the crossing of the midlevel only. The passive interpolation is also the reason why the LPI TDC is said to be robust against local variations. If the delay of an inverter stage varies, the passive interpolation translates this variation to a subdivided variation of the intermediate signals. The sequence of the interpolated signals remains unchanged even for strongly varying resistors. The switching sequence of parallel scaled delay elements for example can be disordered by local variations. This may result in missing codes in the converter characteristic. Local variations also alter the sampling behavior of the comparators which may disorder the switching sequence of all types of TDCs. Therefore, the sampling elements must be
4.2 Time-to-Digital Converter

\[ \frac{1}{2n(n + 1)RC_{ \text{cmp} }} \ll t_{\text{rise}} \]  \hspace{1cm} (4.10)

where \( C_{\text{cmp}} \) is the capacitance at the interpolation nodes and \( t_{\text{rise}} \) is the rise-time of the original signal. As small resistors mean large cross currents there is a tradeoff between a good linearity and a low power consumption. Figure 5.15 illustrates this trade-off.
Two logically equivalent signals with a skew of only one inverter delay ($t_{inv}$) cannot be realized with single ended static MOS logic. The large delay of buffers would require unattractively low signal slopes. Hence, according to Figure 4.10 two coupled inverter chains are used to propagate both the start signal and the inverted start signal. Now, two rising signals with a skew $t_{inv}$ of are available at a node A in the first delay chain and at the output node B of the subsequent inverter in the second delay chain. Therefore, the delay chain in Fig. 8 provides a set of skewed copies of the start signal $Rising_i$ and a set of skewed copies of the inverted start signal $Falling_i$ aligned to the first set. The aligned and complementary signals at the inputs of the chain are generated by a balanced clock splitter. On the rising edge of the stop signal the state of the LPI delay chain is sampled by differential comparators connected to the pairs of complementary signals ($Rising_i$ and $Falling_i$).

A LPI delay line according to Figure 4.9 can be combined with any existing TDC architectures, for instance the multistage TDC [41] or the reference recycling TDC [41]. It can be used open-loop, in a ring or in a DLL structure. In contrast to Vernier [7] or pulse shrinking [41] TDCs both the latency and the dead-time are extremely low, i.e., equivalent to a basic delay-line TDC with coarse quantization.
4.2.5 Process Variations in TDCs

The variations are important issues of the performance and behavior of TDCs because the process and environmental variations influence the behavior and the performance of time-to-digital converters (TDCs). Environmental parameters such as PVT (Process, Supply voltage and Temperature) have global impacts on the performance for the circuit block of TDC. The main reason for local variations are random dopant fluctuation and line edge roughness. Both phenomena are critical especially in heavily scaled process where quantization effects become visible [17].

In TDC, the variations change the gate delays in the delay-line and the buffer tree of the stop signal. The impact of local variations in TDC, especially a

![Figure 4.11: Skew in a buffer tree](image)

buffer tree, is uncertainty of the arrival time of the stop signal. One reason of the uncertainty is the deterministic skew in a buffer tree. Another reason are local process variations that cause skew even in a perfectly balanced tree [17].
The Figure 4.11 shows two groups of delay elements together with their sampling flip-flop. Each buffer level causes the skew in the associated branches of a buffer tree. The TDC characteristics caused by the skew (uncertain value) are illustrated in Figure 4.12. $T_{skew} > 0$ means that the second group of delay elements is sampled later than the first group, and $T_{skew} < 0$ all step positions related to the second group are shifted to the right. If a $T_{skew}$ is larger than $T_{LSB}$, this results not only in a DNL error but also in missing code. These facts cause an increased step width at the handover point of the two groups. This means that the uncertainty of the arrival time of the respective branches is partially correlated and the prediction of variation effects becomes complicated.

Next impact is the local process variations on delay-line. Local process variations cause a modification of each gate delay along the delay-line that can be modeled by

$$T_{d,i} = T_{LSB} + \varepsilon_i$$  \hspace{1cm} (4.11)
where $\varepsilon_i$ is the delay error. If $\varepsilon_i$ become smaller than $-T_{LSB}$, the gate delay $T_{d,i}$ would become negative \[17\]. The step positions of TDC characteristic where the ideal buffer tree and comparators is represented by the switching time which given by.

$$t_n = nT_{LSB} + \sum_{i=1}^{n} \varepsilon_i$$  \hspace{1cm} (4.12)

Thus, the differential non-linearity (DNL) can be calculated according to

$$DNL_n = \frac{t_{n+1} - t_n - T_{LSB}}{T_{LSB}} = \frac{\varepsilon_{n+1}}{T_{LSB}}$$  \hspace{1cm} (4.13)

DNL is directly given by the delay variation of the respective delay element in terms of $T_{LSB}$ \[17\]. The delay-line variations sum up and contribute to the gain error $E_{gain}$ and the integral non-linearity (INL). The arrival time at the end of a delay-line consisting of N delay elements is shown in the equation \[4.14\].

$$t_N = N \cdot T_{LSB} + \sum_{i=1}^{N} \varepsilon_i$$  \hspace{1cm} (4.14)

From the equation \[4.14\], the gain error can be calculated and expressed as

$$E_{gain} = \frac{1}{T_{LSB}} [t_N - t_1] - [N - 1] = \sum_{i=2}^{N} \varepsilon_i$$  \hspace{1cm} (4.15)
From the equation (4.14) and (4.15), the non-linearity (INL) is calculated. INL is given by

\[ INL_n = \frac{1}{T_{LSB}} [t_n - t_1 + \frac{n - 1}{N - 1} (t_N - t_1)] \] (4.16)

From the equation (4.16), the maximum of \( INL_n \) occurs in the middle of the delay-line, more precisely at the position

\[ n = \frac{1}{2} (N + 1) \] (4.17)

This means that the uncertainty of the arrival time grow with the length of the delay line. Therefore, in the aspect of the INL, the delay line should be considered to avoid increasing the uncertainty of the arrival time.

In addition, the one more variation should be considered. That is the variations for the comparators inside TDC. The variations for the comparators, which is components of TDC, are also important issues with TDCs. For example, the blackout time of the comparators functionally affects the TDC offset, the gain and the resolution [17]. The offset error is not critical in most applications. The TDC gain, however, delineates the change of the output word per change of the input time interval. Therefore, the variation of TDC should be considered and controlled for the further calibration and applications.
4.3 Quantization Error of Time-to-Digital Converters

Converting a continuous signal into a discrete signal results in a quantization error $\varepsilon$ according to the equation (4.3). In contrast to ADCs, where the quantization error is usually symmetrical around zero ($0 \leq \varepsilon < \frac{1}{2}V_{\text{LSB}}$), the quantization error of a TDC is not mean free ($0 \leq \varepsilon < T_{\text{LSB}}$). An equally distributed quantization error has the mean value. It can be expressed in the equation (4.18) [17].

$$\langle \varepsilon \rangle = \frac{1}{T_{\text{LSB}}} \int_{0}^{T_{\text{LSB}}} \varepsilon d\varepsilon = \frac{1}{2}T_{\text{LSB}}$$ (4.18)

The quantization noise power is presented in the equation (4.19)

$$\langle \varepsilon^2 \rangle = \frac{1}{T_{\text{LSB}}} \int_{0}^{T_{\text{LSB}}} \varepsilon^2 d\varepsilon = \frac{1}{2}T_{\text{LSB}}^2$$ (4.19)
4.4 Digital Loop Filter

The output of the traditional loop filter (analog loop filter) is quite noisy even after acquisition because of timing jitter, which lowers the synchronizer performance, especially in the parallel structure, where the loop delay would be much longer.

A digital filter is a basic building block in digital systems. Through this work, there has a benefit from replacing the bulky passive loop filter by a more cost-effective and flexible digital filter. The frequency response of the filter depends on the value of its coefficients [31]. The values of the coefficients are computed based on the desired frequency response. These values are typically floating point numbers and they are represented with a fairly high degree of precision[31]. However, when a digital filter is implemented, the coefficients need to be represented with the smallest number of bits that still gives acceptable resolution for the numbers. This is because representing a number with excess bits increases the size of the registers, buses, adders and multipliers. The bigger sizes of implemented circuits result in a chip with a large die size, which translates into increased power consumption. Therefore, the bit precisions are important in the performance of desired digital filter.

A digital filter is categorized into two classes known as a finite impulse response (FIR) filter and an infinite impulse response (IIR) filter [52].
4.4 Digital Loop Filter

4.4.1 FIR Filter

FIR filter is one whose impulse response is of finite duration. The general differential equation of FIR filter is stated mathematically as

\[ y(n) = \sum_{k=0}^{M-1} b_k x[n - k] \]  

where \( y(n) \) is the filter output at discrete time instance \( n \), \( b_k \) is the \( k \)-th feed-forward tap, or filter coefficient, \( M \) is the number of feed-forward taps in the FIR filter, and \( x(n-k) \) is the filter input delayed by \( k \) samples [31]. The differential equation of FIR filter is the discrete time equivalent of a continuous time differential equation. In FIR filter, the output depends only on the previous \( M \) inputs. Once the impulse passes through the tapped delay line, if the input is Kronecker delta function \( \delta(n) \), the output of the filter is zero.

The advantages of FIR filter are simple to design and they are guaranteed to be bounded input-bounded output (BIBO) stable, and FIR filter is sure to have linear phase. FIR filters also have a low sensitivity to filter coefficient quantization errors [31]. This is a desirable property to have when implementing FIR filter for many applications using digital signal processing.

The drawback of FIR filters is straightforward to design by using CAD tools. One of the major drawback of FIR filters is that large amounts of memory and arithmetic processing are needed. This makes them unattractive in many
4.4 Digital Loop Filter

4.4.1.1 FIR Filter Structures

An FIR filter can be realized using either recursive or non-recursive algorithms \cite{12}. The former, however, suffer from a number of drawbacks and should not be used in practice. On the other hand, non-recursive filters are always stable and cannot sustain any type of parasitic oscillation, except when the filters are a part of a recursive loop. They generate little round-off noise. However, they require a large number of arithmetic operations and large memories.

A number of delay lines contained in a filter determine the order of a filter. For example, if the filter is assumed to be of order 10, it means that it is necessary to save 10 input samples proceeding to the current sample. All eleven samples will affect the output sample of FIR filter \cite{36}. The fundamental blocks of FIR filter is presented in Figure 4.13.

The transform function of a typical FIR filter can be expressed as a polynomial of a complex variable $z^{-1}$. All the poles of the transfer function are located at the origin. For this reason, FIR filters are guaranteed to be stable, whereas IIR
filters have potential to become unstable.

4.4.1.2 Effect of the Poles and Zeros of the Transfer Function

The locations for the poles and zeros of the transfer function are very important for discrete-time system analyses and synthesis since their location is used to test stability of a discrete-time system. In order that a discrete-time system is stable, all poles of the discrete-time system must be located inside the unit circle, as shown in Figure 4.14. If this requirement is not satisfied, the system becomes unstable. The location of zeros doesn’t affect the stability of discrete-time systems. FIR filters do not have a feedback, which further means that the transfer function has no poles. This causes a FIR filter to be always stable. This property of FIR filters actually represents their essential advantage.
Frequency deviation depends on the spacing between the zeros of the FIR filter transfer function. FIR filter coefficient error affects more the frequency characteristic as the spacing between the zeros of the transfer function narrows. This property is particularly typical of high order filters because their zeros are very close each other. However, slight errors in coefficient representation may cause large frequency deviations [6, 36].

4.4.2 IIR Filter

Infinite impulse response (IIR) filters are filters in the theory of digital signal processing. In contrast to finite impulse response filter known as FIR filter, IIR filter have a build-in feedback which leads to an infinitely long response to an impulse [39]. When the high-speed design circuitry is implemented such as digital-phase locked-loop (DPLL), IIR filters are useful because they typically require a lower number of multiplies compared to FIR filters. IIR filters are also used to have a frequency response that is a discrete version of the frequency response of an analog filter.

Two kinds of transformation methodologies are used to design IIR filters. One is the impulse invariance, and the other is the bilinear transformation. The transfer function of impulse invariance is computed from the transfer functions of analog filter. Through the Laplace inverse transforming, the transfer function of s-domain, H(s), is converted into h(t) in the form of time-domain. The h(t)
is, then, sampled by the sampling frequency \((f_s)\) to obtain the \(h(nT)\). The basic principle of the impulse invariance is shown in Figure 4.15. The other design methodology of IIR filters is to use the bilinear transform. This method is the most popular method and used in the proposed ADPLL. The bilinear transform is a correction of the backwards of difference method [40]. Additionally, this technique allows an algebraic transformation between the variables \(s\) and \(z\) that maps the entire \(j\Omega\)-axis in the \(s\)-plane to one revolution of the unit circle in the \(z\)-plane. Since \(-\infty < \Omega < \infty\) maps onto \(-\phi < \omega < \phi\), the transformation between the continuous-time and discrete-time frequency variables must be non-linear. Therefore, the use of this method is acceptable for the corresponding warping of the frequency [39].

The bilinear transform is defined as,

\[
s = \frac{2 \left(1 - z^{-1}\right)}{T_s \left(1 + z^{-1}\right)} \quad (4.21)
\]
The bilinear transform produces a digital filter whose frequency response has the same characteristics as the frequency response of the analogue filter. As mentioned above, this method is used to map the variable $s$ in $s$-plane into the variable $z$ in $z$-plane. To verify this characteristic, the two cases could be considered.

$$s = \sigma + j\Omega \quad (4.22)$$

To solve for $z$, the equation (4.22) substitute into (4.21). The expression for $z$ is stated as

$$z = \frac{1 + s}{1 - s} = \frac{1 + \sigma + j\Omega}{1 - \sigma - j\Omega} \quad (4.23)$$

Therefore,

$$|z|^2 = \frac{(1 + \sigma)^2 + \Omega^2}{(1 - \sigma)^2 + \Omega^2} \quad (4.24)$$

The equation (4.24) is important to look into the characteristics of the mapping property of the bilinear transform. If the imaginary axis, i.e. $\sigma=0$. This corresponds to the boundary of stability for the analogue filters’ poles. With $\sigma=0$, the equation (4.24) is solved as following;

$$|z|^2 = \frac{(1)^2 + \Omega^2}{(1)^2 + \Omega^2} = 1^2 \quad (4.25)$$

This result shows the imaginary (frequency) axis in the $s$-plane maps to the unit circle in the $z$-plane. Moreover, if the imaginary axis $\sigma \neq 0$, the corresponding
result is shown in the equation (4.26).

\[ |z|^2 = \frac{(1 + \sigma)^2 + \Omega^2}{(1 - \sigma)^2 + \Omega^2} \leq 1^2 \]  

(4.26)

The equation (4.26) indicates that the left half s-plane maps onto the interior of the unit circle of z-plane. This property of the bilinear transform, thus, provides that the left half s-plane maps onto the interior of the unit circle in the z-plane. The relationship between variables s and z is presented in Figure 4.16. This property allows us to obtain a suitable frequency response for the digital filter, and also to ensure the stability of the digital filter [40]. In addition, the relationship between \( \Omega \) and \( \omega \) should be considered to preserve the important features of the frequency response. In the bilinear transform, the relationship
4.4 Digital Loop Filter

between \( \Omega \) and \( \omega \) can be expressed as

\[
\omega = 2 \arctan(\Omega)
\] (4.27)

This equation (4.27) provides the important issues for the mapping property of the bilinear transform. First, the \( \Omega=\omega \) mapping is monotonic. Second, if \( \Omega=0 \), it is mapped to \( \omega=0 \), and \( \Omega=\infty \) is mapped to \( \omega=\pi \), which means half of the sampling frequency. Therefore, for instance, an analogue low-pass response that decays to zero at \( \Omega=\infty \) produces a low-pass digital filter response that decays to zero at \( \omega=\pi \) [31, 39, 40].

The general equation of the IIR filter is,

\[
y(n) = a_0 x[n] + a_1 x[n-1] + \cdots + a_{M-1} x[n-(M-1)] - b_1 y[n-1] \quad (4.28)
\]

The transfer function of IIR filter is generally expressed as following equation;

\[
H(z) = \frac{Y(z)}{X(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \cdots + b_M z^{-M}}{1 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} + \cdots + a_N z^{-N}} \quad (4.29)
\]

\[
H(z) = \frac{\sum_{k=0}^{M} b_k z^{-k}}{1 + \sum_{k=1}^{N} a_k z^{-k}} \quad (4.30)
\]
4.4 Digital Loop Filter

4.4.2.1 IIR Filter Structures

The basic block of IIR filter structures is presented in Figure 4.17. Basically, the structures of IIR filters adopt a recursive form, which means the filters use feedback. An infinite number of coefficients are not realized with a finite number of computations per sample.

1. Direct I realization

Direct realization is expressed as

\[
y[n] = \sum_{k=0}^{N} b[k] \cdot x[n-k] - \sum_{k=1}^{N} a[k] \cdot y[n-k]
\]  
(4.31)

The first part of the expression refers to non-recursive part and the other part refers to recursive part. In the direct realization, this structure is known as a direct form I structure. The direct form is the simplest straightforward implementation of an IIR filter. As seen from Figure 4.18, direct realization requires
4.4 Digital Loop Filter

in total of $2N$ delay lines, $(2N+1)$ multiplications and $2N$ additions. The structure is pair of two separate systems which are connected via an adder. The two systems are named nominator and denominator. This structure consists of the minimum number of multipliers and just one accumulator to add the partial sums up. The direct realization is convenient for software implementation, and is most commonly used. Some of disadvantages of this realization are the sensitivity to accuracy of realized coefficients regarding a large finite word-length effect, and the complexity due to implementation.

2. Direct II realization

In most IIR filter systems, the nominator and denominator have the same polynomial grade. This structure is canonic; it requires the minimum number of
memory elements. Applying direct form II, both are merged to one system, therefore only half of the delay-elements are needed [2].

3. Direct transpose realization

Direct transpose I realization is similar to direct I realization. The only difference is the position of delay-elements. Therefore, it has the minimum length $N+1$ of the non-recursive coefficients, where $N$ is the filter order. Figure 4.20(a) and Figure 4.20(b) illustrate the block diagrams of the direct transpose I realization structure and the direct transpose canonical realization structure.

Direct transpose canonical realization structure has reduced number of delay lines to the minimum of $N$ delay lines as well as reduced number of adders to $N+1$. Recursive and non-recursive parts of IIR filter are not considered separately, which causes implementation to be more complex than for direct realization structure, but similar to direct canonical structure. A good thing is that
4.4 Digital Loop Filter

\[ y(n) = b_0 x(n) + b_1 x(n-1) + \cdots + b_N x(n-N) - a_1 y(n-1) - a_{N-1} y(n-N-1) - a_N y(n-N) \]

Figure 4.20: The direct transpose realization of IIR filter

The coefficients are the same as for direct realization [36].

The transpose form of a given direct form is as simple as reverse all directions of the signal graphs and make accommodations, such as changing signal branch-points to summers, and summers to branch-points. The flipped diagram is the new transposed form with input and output on the correct site. It is also called flow graph reversal or transposition [31, 39].

4. Parallel realization

After a partial fraction expansion, the system is interpreted as a parallel connection between different order systems. A rational transfer function can be written as the equation (4.32).

\[ \frac{\sum_{k=0}^{M} b_k z^{-k}}{1 + \sum_{k=1}^{N} a_k z^{-k}} = c_0 + c_1 z^{-1} + \cdots + \frac{A_1}{z - p_1} + \frac{A_2}{z - p_2} + \cdots + \frac{A_N}{z - p_N} \]  

(4.32)
Figure 4.21 represents an example of the parallel form IIR filter system. As seen in the equation (4.32), the complex-conjugate pole pairs is combined into second-order sections with real coefficients. For this reason above, this parallel form is of interest because the parallel form is less sensitive to coefficient quantization than the higher-order structures.

5. Cascode realization

After the equation (4.30) of a fundamental IIR filter system is factorized, the equation (4.33) is obtained, where $M=M_1 + 2 \cdot M_2$ and $N=N_1 + 2 \cdot N_2$.

$$H(z) = H(0) \cdot \frac{\prod_{k=1}^{M_1} (1 + a_{1k}^{(1)} z^{-1}) \prod_{k=1}^{M_2} (1 + a_{1k}^{(2)} z^{-1} + a_{2k}^{(2)} z^{-2})}{\prod_{k=1}^{N_1} (1 - b_{1k}^{(1)} z^{-1}) \prod_{k=1}^{N_2} (1 - b_{1k}^{(2)} z^{-1} - b_{2k}^{(2)} z^{-2})} \quad (4.33)$$

This equation (4.33) describes as a serial connection of the first order and the second order system. The first order coefficients represent real value poles and zeros, second order coefficients represent conjugate complex pole and zero pairs.
4.4 Digital Loop Filter

![figure 4.22: The blocks of cascode realization](image)

The cascode form is presented in Figure 4.22.

4.4.2.2 Effect of the Poles and Zeros of the Transfer Function

The locations for the poles and zeros of the transfer function are very important for discrete-time system analyses and synthesis since their location is used to test stability of a discrete-time system. In order that a discrete-time system is stable, all poles of the discrete-time system transfer function must be located within the unit circle, as shown in Figure 4.16. If this requirement is not satisfied, the system becomes unstable. The locations of zeros do not affect the stability of discrete-time systems. In FIR filters do not have a feedback, which makes them stable. However, IIR filters have a feedback. Therefore, the bilinear transformation is preferred to use because it makes the poles and zeros maps onto the unit cycle in z-plane, and always makes filter stable.
Chapter 5

Design of Procedure Proposed

ADPLL

5.1 Phase Frequency Detector

PLLs includes a tri-state phase frequency detector (PFD) to monitor the phase and frequency differences between lead and lag signals (inputs), and PFD produces the signal, which includes the information regarding the phase and frequency differences, to injected into the charge-pump for an analog PLLs and to controls the sign bit for a digital PLLs. The tri-state PFDs are built with memory components, and they need a reset signal to clear the memory components \cite{9}. Among the previous published PFD topologies, the precharge PFDs and the latch-based PFDs \cite{8, 28, 49} are the most commonly used for a high
5.1 Phase Frequency Detector

![Figure 5.1: PFD ideal and non-ideal characteristics](image)

operation speed, low power consumption, wide input range, and independence to the input duty cycle [9].

5.1.1 Issues of PFDs

The characteristic of PFD is ideally linear for the entire range of input phase differences from \(-2\pi\) to \(2\pi\) as depicted by Figure 5.1. When the inputs differ in frequency, the phase difference changes each cycle by \(2\pi\left(\frac{T_{ref}-T_{feedback}}{\max(T_{ref},T_{feedback})}\right)\) [32].

On a clock cycle during frequency acquisition, the PFD transfer curve is held from \(-2\pi\) to \(2\pi\) and repeats as the output clock cycle slips. Once within the lock-in range, the cycle slipping stops and the phase is acquired, behaving as a linear system. However due to the reset path, the linear range is less than \(4\pi\) (\(\pm2\pi\)) as shown in Figure 5.1.

The most important issue of PFD is the dead zone, which is the minimum pulse-width of the PFD output including the missing the phase and frequency information. To mitigate the dead zone issue, the reset signal inside the tri-state PFD should be designed to the trigger pulses with a constant width at the PFD.
5.1 Phase Frequency Detector

outputs when the phases of the inputs are aligned \[9\]. However, during the reset process, PFD has the blind zone, where the PFD cannot work any transitions on the input signals. If the phase difference falls into the blind zone during the frequency acquisition, the PFD delivers incorrect phase information.

Due to this reason, the chance of cycle for comparisons the phase and frequency differences is increased, and the increased cycle directly affects the PLL frequency acquisition time. With increasing input frequency, the fixed reset pulse-width becomes a greater portion of the total period, and design techniques are needed to reduce the blind zone while maintaining the same reset pulse-width \[3\]. The widely used technique reducing a blind zone is adding an extra delay cell \[32, 49\]. This approach reduces the blind zone close to the theoretical limit imposed by PVT variations.

5.1.2 Previous Improved Precharge PFD

This section discusses the previous improved precharge PFD with adding extra transistors. When the phase difference between the two inputs is close to \(2\pi\), the rising edge of the leading phase can fall into the reset region. During reset process, the PFD is not able to detect the lead input signal. Thus, the PFD detects the following lag signal as the lead signal, and it generates the wrong phase information, which is reversed signal. This is the blind zone since the PFD is under blind in this region \[9\]. This effect causes the phase comparison range
5.1 Phase Frequency Detector

of the PFD to reduce onto $2\pi \Delta$, where $\Delta$ is the length of the blind zone. Figure 5.2 shows the input-output phase response characteristic of PFD with blind zone. In general, the width of the reset pulse is around several hundred picoseconds.

The second zero-crossing point is an unstable point. This point prolongs the phase acquisition time when the phase-locking process is performed. An ideal PFD does not suffer from the error information because there is no second zero-crossing point in the ideal phase characteristic waveform of the PFD, as shown in Figure 5.1. In reality, the blind zone provides those zero-crossing points [9]. If the clock period is much longer than the blind zone, the zero crossing points are located close to the multiples of $2\pi$ phase difference. As mentioned above, the blind zone affects directly the frequency acquisition time. Reducing the blind
zone mainly decreases the frequency acquisition time, and it increases the phase-locking range. Therefore, for high-frequency operation, decreasing the blind zone becomes more crucial since it not only improves the acquisition time and the phase-locking range but also reduces the chance of hang-up, which is caused by the periodic property of the phase detector in the characteristic waveform in $2\pi$ phase shift [13, 14]. In the previous improved PFD, which is published in [49], adding the extra delay elements, $T_D$, to the inputs reduces the $T_{reset}$, as shown in Figure 5.3. The extra added delay cells shift the lead signal until the reset process, then the PFD responses to the rising edge of the input signal [9].
5.1 Phase Frequency Detector

For a proper operation, $T_D$ should be smaller than $T_{reset}$. When the condition is opposite, the clock that triggers the reset process activates after the reset is finished. This condition makes the PFD not to work properly. According to this approach, due to the $T_D$ of extra delay cell, the lead signal is delayed, and when the phase difference enters the blind zone, the blind zone becomes $T_{reset} - T_D$. $T_{reset} - T_D$ is close to zero where $T_D$ is close to $T_{reset}$.

5.1.3 Implemented PFD for the Proposed ADPLL

The implemented PFD is published in [9]. In previous section above, the technique that reduces the length of blind zone is discussed. However, the blind zone consists of two major portions. One of portions is the reset process ($T_{reset}$) and the other is precharge time ($T_{pre}$) of the internal nodes as depicted in Figure 5.4. In this Figure 5.4, the blind zone is composed of $T_{reset} - T_{pre}$. As the $T_{reset}$
is reducing, the precharge time ($T_{pre}$) occupies a large portion of the blind zone and cannot be ignored. If the delayed signal after the reset process could not provide enough time to charge the internal nodes at node X1. Then the node X1 could not be high enough to switch off the transistor PMOS 3. This effect causes an undesired transition at the output of PFD, as shown in Figure 5.6. The same problem also exists in the lower branch circuit. Therefore, the blind zone is actually $T_{reset} - T_D + T_{pre}$ rather than $T_{res} - T_D$. With the increasing delay time, the length of the blind zone reduces. However, the charging time of the internal nodes in the PFD is responsible for the remaining portion of blind
Figure 5.6: Erroneous output form the PFD without added transistors PMOS 7 and PMOS 8.

Since the blind zone has a large portion of precharge time ($T_{pre}$), the two transistors PMOS 7 and PMOS 8 are added to turn on the pull-up paths at the falling edges of the inputs. The waveforms in Figures 5.6 and 5.7 is described the role of the added transistors. Without PMOS 7 and PMOS 8, the half-charged node X1, which is the output of inverter between NMOS 1 and PMOS 2, pulls node Y1, which is the output node between NMOS 2 and PMOS 3, high at the falling edge of the inputs, and the undesired transition, which is uncharged fully, gives an unexpected information at the output. The added transistors PMOS 7 and PMOS 8 makes node X1 to high at the falling edges of the inputs, and the extra transistors prevent the output from
erroneously changing states. Since the delay cells are mainly designed to delay the rising edges of the input, PMOS 7 and PMOS 8 do not affect the function of the delay cells. The two added transistors are used to remove the delay at the falling edges of the input.

The improvement of the proposed PFD can be evaluated by the gain attenuation factor of the PFDs. The gain attenuation factor $\alpha$ is introduced in [8] to calculate the average gain reduction of the PFD caused by the blind zone in high-speed operation. The equation for the factor is repeated as

$$\alpha = 1 - 2(\Delta - T_D) - T_D^2$$

(5.1)
5.1 Phase Frequency Detector

Figure 5.8: Simulated phase characteristic waveform of the PFDs

where $\Delta$ is the normalized width of the blind zone, and $T_D$ is the delay of the delay cell normalized to one clock cycle. Figure 5.8 [9] shows the phase characteristic waveforms and the corresponding gain attenuation factors of the three PFDs [9]. As can be seen in the figure, since the three PFDs have the same circuit delay and reset pulse-width, the phase characteristic curves bend down almost at the same position, but because of the reduced charging time, the blind zone of the proposed PFD shrinks, which leads to the lowest gain reduction. Reducing the blind zone leads to a faster frequency acquisition time [8, 32], and consequently, the proposed design is suitable for the applications that require fast frequency switching.

The two added transistors PMOS 7 and PMOS 8 also increase the maximum operating frequency because of the finite precharge time $T_{pre}$. To see this, one
can compare the charging time $T_{chr}$, as shown in Figures 5.6 and 5.7 [9]. Without transistor PMOS 7 and PMOS 8, the maximum $T_{chr}$ is equal to $(\frac{\text{period}}{2} - T_D)$, where $\text{period}$ is the period of the input signal. When the input frequency increases to several gigahertz, $T_{chr}$ might be smaller than $T_{pre}$, preventing X1 and X2 from being pulled to a high-enough level. The halfcharged voltage on X1 and X2 extends the reset pulse and reduces the operating speed. Adding transistors PMOS 7 and PMOS 8 mitigates this limitation since $T_{chr}$ is always equal to $\frac{T_{chr}}{2}$. 
5.2 Implemented LPI-TDC

The basic block of LPI-TDC is presented in Figure 5.9. Local Passive interpolation (LPI)-TDC is discussed briefly in previous TDC chapter, this type of TDC has more advantages than other types of TDCs. However, the LPI-TDC has disadvantages about the fixed resolution and the cross current. Therefore, the proposed LPI-TDC based on conventional LPI-TDC is proposed. The conventional LPI-TDC [17] is presented in Figure 5.2 and the proposed LPI-TDC is presented in Figure 5.2.

5.2.1 The Proposed LPI-TDC

As discussed above, the conventional LPI-TDC has problems about the fixed resolution, which depends on the CMOS technology. The inverter based TDC depends on the inverter delay. Thus, inverter delay should be small enough to satisfy the resolution of TDC. However, the conventional LPI-TDC does not have only one inverter delay.

Since the delay element of the conventional LPI-TDC is composed of two multiplexers (MUX) and four inverters, the one delay elements has delays of MUX.
Figure 5.10: The proposed LPI-TDC structure

and inverters as shown in Figure 4.9. The expression of the delay element is expressed as

\[ t_{D_{\text{conv}}} = t_{\text{mux}} + t_{\text{inv}} \]  

(5.2)

\( t_{D_{\text{conv}}} \) is a delay of the delay element in the conventional LPI-TDC, and each \( t_{\text{mux}} \) and \( t_{\text{inv}} \) is a delay of the multiplexer and the inverter. These facts interrupt achieving a high resolution of TDC, and affect the quantization error such as missing codes when TDC convert time to digital codes. Therefore, to fix this
5.2 Implemented LPI-TDC

The proposed first delay element of LPI-TDC is presented in Figure 5.11. The delay of this tristate inverter must be same as the normal inverter.

Figure 5.11: The proposed first delay element of LPI-TDC

problem of the conventional delay cell, the delay cell based on the cascode tristate inverters is proposed to eliminates a term $t_{mux}$. Basically, the coarse resolution of LPI-TDC is determined by $\frac{t_{mux}}{f_F}$. Thus, A higher resolution will be achieved as the $t_D$ is getting smaller.

Therefore, the $t_D$ needs to be small enough to achieve the high resolution of LPI-TDC. To maintain the $t_D$ as small as possible, just one inverter delay unlike the conventional LPI-TDC is considered, not $t_{mux} + t_{inv}$. The proposed LPI-TDC is presented in Figure 5.10. The difference between the conventional LPI-TDC and the proposed LPI-TDC is the elements inside delay cell for LPI-TDC. The proposed LPI-TDC consist of different delay elements. The first delay element of the proposed LPI-TDC is replaced the delay element based on the tristate inverter. Figure 5.11 represents the first delay element of the proposed LPI-TDC. The delay of this tristate inverter must be same as the normal inverter.
5.2 Implemented LPI-TDC

(t_{inv}) because the purpose of these tristate inverters is to remove the unnecessary delay (t_{mux}), which is caused from the multiplexer, and to keep the same delay of a normal inverter (t_{inv}). Each delay cells of the proposed LPI-TDC has the same $t_{delay}$ and the interpolation factor ($IF$) of 4. A fine resolution is determined by the sense amplifiers with latches, which is processed with same function of the conventional LPI-TDC \[17\]. The coarse digital codes are determined with a 6 bit binary counter at output of the proposed LPI-TDC. The expression of $t_{coarse}$ is presented in the equation (5.3).

$$t_{coarse} = t_{delay} (= t_{LSB} \times IF) \times N \times N_C$$  \hspace{1cm} (5.3)

N indicates the number of delay cells and $N_C$ is a number from a counter at the end of TDC. As shown in equation (5.3), the counter measures $t_{coarse}$ with the $t_{delay}$ between the lead signal and the lag signal of ADPLL. Thus the $t_{delay}$
5.2 Implemented LPI-TDC

is important factor for the LPI-TDC as discussed in the previous section. The small $t_{delay}$ of the proposed LPI-TDC that removes the term of $t_{mux}$ provides the more accurate measurement of time differences than the conventional LPI-TDC, which has an additional term of $t_{mux}$ as shown in Figure 5.12.

5.2.2 Comparison

The improvements make it possible to achieve higher resolution and results in lower power consumption than the conventional TDC composed of multiplexers and inverters. In addition, the proposed structure does not change the unique characteristics of LPI-TDC. The proposed LPI-TDC is also monotonic and has a robustness to process.

5.2.2.1 TDC Response

When the loop signal is high, the TDC measures the phase difference with the resolution of TDC. Figure 5.13 and 5.14 are measured by the binary counter at the end of LPI-TDC for the coarse bit. As seen in Figure 5.13 and 5.14, if the phase difference 0.7ns, the counter detects 6 times and 9 times with the conventional LPI-TDC and the proposed LPI-TDC. Then, the binary counter generates the coarse bit within the phase difference. The resolution is increased 50% compared to the conventional one. This result explains how the resolution of LPI-TDC affects to measure time difference by LPI-TDC.
5.2 Implemented LPI-TDC

Figure 5.13: The response of the conventional TDC

5.2.2.2 Power Consumption

Figure 5.15 presents the power consumption of the conventional and the proposed LPI-TDCs. As expected, the power consumption is increased 15% with the proposed LPI-TDC if the phase difference between the reference clock and the feedback clock is 0.7ns. However, this is not disadvantage of the proposed LPI-TDC. Since the higher resolution of the proposed LPI-TDC measures time difference more accurately than the conventional one, the number of cycle in ADPLL is reduced. Therefore, even though the proposed LPI-TDC consumes more power than the conventional one, overall power until the frequency acquisition is decreased by 12% compared to the ADPLL with the conventional
5.2 Implemented LPI-TDC

Figure 5.14: The response of the proposed TDC

Figure 5.15: The comparison between the conventional and the proposed TDCs of the power consumption with various resistances
5.2 Implemented LPI-TDC

LPI-TDC.

Figure 5.15 also presents the power consumption compared to the resistances, which is used as the voltage divider. The reason the power consumption compared to the resistances is to compare the alternative elements for the interpolated resistors. As known, the MOSFETs can be implemented instead of a interpolated resistor. However, as can be seen in Figure 5.15, very low resistance consumes more power. If using the on-resistance of MOSFETs in the saturation region, the proposed LPI-TDC consumes maximum 13% more than the LPI-TDC with the interpolated resistors. Furthermore, in order to design a low power consumption model of TDC, the value of interpolated resistors should be considered because it is the trade-off between the area and the low power consumption. The 33% reduction of the power consumption is the best case when the resistance is 1.5kΩ, otherwise the 13% reduction is the worst case when the resistance is 0.5kΩ.
5.3 Proposed Digital Loop Filter

The basic block of proposed digital loop filter (DLF) is shown in Figure 5.16. As seen in Figure 5.16, the basic block is same as the fundamental first order recursive filter with the coefficients $\alpha$ and $\beta$. The differences between the conventional first order digital loop filter and the proposed one are the complexity when it is implemented and the benefit regarding of the area. To avoid the complex calculation, where the coefficients are applied, the approximation method is used.
for the proposed DLF. The approximation method provides benefits regarding
the less complexity and small area. The shift register instead of the multipliers
is utilized as multiplying coefficients.

### 5.3.1 Implemented Digital Filter Circuitry

Since the conventional phase/frequency detector and charge pump, which encode
the phase error by the width of the train of pulses at frequency rate, are replaced
by the time-to-digital converter (TDC), the phase-domain operation does not
fundamentally generate any reference spur thus allowing the digital loop filter
(DLF) to be set at an optimal performance point between the reference phase
noise and the oscillator phase noise \[48\]. Figure 5.16 represents the digital fil-
ter circuitry for the proposed ADPLL. The Figure 5.16 is also represented into
Figure 5.17. The Figure 5.16 and Figure 5.17 have same functionality.

The single-pole loop filter consists of an integral path with the loop gain co-
efficient \(\beta\), a proportional path with loop gain coefficient \(\alpha\), and path for the
function of \(z^{-1}\) respectively. The each path is a direct path from the output
of the phase/frequency detector or the time-to-digital converter (TDC) to the
control bits of the DCO. The integral path is in the function of integrator of se-
quential inputs and the proportional path is in charge of the step size of the scaler
for the stability. The proportional path of the DLF is important for the loop
stability \[44\]. The DLF is clocked by the divided clock, which is synchronous
5.3 Proposed Digital Loop Filter

with the reference clock in the locked condition. The loop filter configuration can be expressed in the following equation;

\[ H(z) = \alpha + \frac{\beta}{1 - z^{-1}} = \frac{(\alpha + \beta) - \alpha \cdot z^{-1}}{1 - z^{-1}} \]  \hspace{1cm} (5.4)

\[ y(n) = (\alpha + \beta) \cdot x(n) - \alpha \cdot x(n - 1) + y(n - 1) \]  \hspace{1cm} (5.5)

The parameters of a digital loop filter \( \alpha \) and \( \beta \) can be obtained from the parameters of an analog loop filter \( R \) and \( C \) by using the bilinear transform \[24].

The bilinear transform in the equation (4.21), which is depicted in chapter 2, is commonly used to design digital filters based on their analog prototypes \[38].

The only disadvantage of the bilinear transform is frequency warping. This affects the frequency response at frequencies close to the Nyquist rate \[24]. Since the bandwidth of the PLL is at least ten times smaller than the update rate, frequency warping will have a negligible effect.

The relationship between \( \alpha \) and \( \beta \) is expressed by a consequence of the analysis.

A simple relationship between the proportional gain \( \alpha \) and the integral gain \( \beta \) can be established \[24]. The equations for the calculation of the relationship between \( \alpha \) and \( \beta \) are presented in the following expression;

\[ \alpha = R - \frac{1}{2f_s} \]  \hspace{1cm} (5.6)
5.3 Proposed Digital Loop Filter

\[ \beta = \frac{1}{Cf_s} \]  

(5.7)

The coefficients for both proportional and integral paths are calculated as \( \alpha = 0.194611 \) and \( \beta = 0.0212579 \) by the equations of the relation of parameters of the digitally controlled oscillator (DCO). In the approximation method, the coefficients are changed to simple expression in a binary fashion. Since the

![Diagram](image1)

**Figure 5.18:** The basic concept for the modified \( \alpha \) coefficient multiplying

![Diagram](image2)

**Figure 5.19:** The basic concept for the modified \( \beta \) coefficient multiplying

coefficient \( \alpha \) is under \( 2^{-3} \leq \alpha < 2^{-2} \), the \( \alpha \) is converted into \( (2^{-3} + 2^{-4} + 2^{-7}) \)
5.3 Proposed Digital Loop Filter

≃ \alpha. In a same method, due to \(2^{-7} \leq \beta < 2^{-6}\), the \(\beta\) is converted into \((2^{-6} + 2^{-7})\). The approximation method provides a benefit with compromising the complexity as using a shift register instead using a multiplier. Both concepts of modified applying coefficients are presented in Figure 5.18 and 5.19.

The above approximation affects the effective loop band-width and phase margin of the designed ADPLL. For the designed ADPLL, the effective phase margin is \(PM=48.3^\circ\) and the effective unity gain bandwidth is \(UGBW = 0.5\) MHz. The response differences for the phase margin and unity gain bandwidth is depicted in [24] when the parameters is applied in difference circumstances. The magnitude and phase responses of the analog prototype, the analog prototype with coefficients approximated for the digital implementation for the simplicity and area. Since the coefficients are in a binary fashion, the multiplying between the input vectors and coefficient are operated with the shift registers. The basic block for this operation is presented in Figure 5.18 and 5.19 for the proposed DLF.
5.4 Digitally Controlled Oscillator (DCO)

The proposed Digitally Controlled Oscillator (DCO), which is an on-chip oscillator, is the one of key components in the proposed ADPLL. The DCO used in this ADPLL is presented in Figure 5.21. This architecture is based on the DCDEs in [34], [35]. The DCO in [34], [35] is derived from the current starved digitally controlled digital elements. This is the basic idea of the proposed DCO and the 4 to 1 multiplexer is added to extend the frequency ranges.

5.4.1 Principal Operation Theory of the Proposed DCO

As can be seen in this Figure 5.20, a current starved buffer, MN7 to MN11, is one of key elements for this proposed DCO. A current mirror, which composed of transistors MN6 and MN7, control the controlling current through the current starved buffer. The controlling current through MN7 is adjusted by the input digital words, while transistor MN5, as indicated in [34], is always on.

The capacitor between the MP9 - MN8 and MP11 - MN10 starts to discharge when MN8 is turned on. The passing current, which is determined by the gate voltage of MN6, through transistor MN7 controls the discharging current of node T [35].

Therefore, the diverse appropriate frequencies, which are generated by the DCO, are digitally controlled by the input digit-words through MP1 to MP10. In this circuit, the proposed DCO operates in steps of 2048 different frequencies.
The transistor MP5 that always is on contributes toward the lower frequency of this proposed DCO. Thus, the W/L ratio of transistor MP5 should be designed carefully to determine the lower frequency and the operating range. The lower frequency is 400MHz in this DCO, which the W/L is applied in MP5 is 0.50µm/0.22µm. The mathematical model analysis is provided in Section 5.4.2.

5.4.2 Mathematical Model of the Proposed DCO

Figure 5.20 represents the element of DCO. For the better controllability, the W/L ratio of transistor MN8 should be much bigger than that of MN7. In such an arrangement, the current is controlled by MN7 [34]. In order to provide a mathematical expression for this DCO, the short-channel length equations expressed in the equation (5.8) for CMOS is applied since the transistors used in this proposed DCO is relatively small transistors with a channel length of 0.18µm.

\[
I_D = \frac{k_n W_7}{2L_7} (V_{GS7} - V_{th7})(1 + \lambda_7 V_{DS7})
\]  

(5.8)

Equation (5.8) is valid as long as the transistor is in the saturation region. This situation is suitable for most of the transition time since the gate voltage of MN7 is not much bigger than its threshold voltage [34]. The output voltage of node
"OUT1" ($V_{OUT1}$) can be expressed in the following:

\[-C_{L1} \frac{dV_{OUT1}}{dt} = \left[ \frac{k_n W_7}{2L_7} (V_{GS7} - V_{th7})(1 + \lambda_7 V_{DS7}) \right] + V_{drop-MN8} \]  

(5.9)

where $C_{L1}$ indicates the overall capacitance for $V_{OUT1}$ at node OUT1. From the equation (5.9), the circuit delay of the delay element can be obtained. The circuit delay of the delay element can be expressed as

\[ t_{d1} = \tau_1 L_n \frac{1 + \lambda_7 V_{dd}}{1 + \lambda_7 \frac{V_{dd}}{2}} \]  

(5.10)

When the delay of the delay element equation is computed, the current starved natures of the first inverter should be considered. The fall time of the first
5.4 Digitally Controlled Oscillator (DCO)

inverter \((V_{OUT1})\) is not small, therefore, the direct current passing through transistor MN10 and MP11 is not negligible \([34]\ [35]\). It is necessary to consider the current in both of these two transistors in order to find \(V_{OUT2}\). However, this direct current through transistor MN10 and MP11 and finding the \(V_{OUT2}\) complicate the equations, and defeat the purpose of a simple analytical model. We assume that the direct path current is negligible and can be ignored in these calculations. Moreover, ignoring the channel length modulation effect of MP11, the path current can be presented as

\[
i_{d-MP11} = C_L \frac{dV_{OUT2}}{dt} = \frac{k_p W_{11}}{2 L_{MP11}} (V_{GS11} - V_{T11})^2
\]

From the equation \([5.11]\), \(V_{OUT2}\) can be obtained as the equation \([5.12]\).

\[
V_{OUT2} = (V_{DD} + \frac{1}{\lambda_7} - |V_{T11}|) \left( \frac{k_p W_{11}}{2 L_{11} C_L} \right)^2 \tau_1 \left( \frac{1}{\tau_1} + 2 e^{-t/\tau_1} - \frac{1}{2} e^{-2t/\tau_1} - 1.5 \right)
\]

The delay time of the circuit of delay element can be computed from the equation \([5.12]\). This equation is very important when a linearity of the proposed DCO is measured.

5.4.3 Design Procedure of the Proposed DCO

In this section, the proposed DCO is discussed along the design procedure list. As seen in Figure \(5.20\), this proposed DCO is based on the current control of
5.4 Digitally Controlled Oscillator (DCO)

Figure 5.21: The structure of Digitally Controlled Oscillator (DCO)

MN7 with a current mirror as same as DCDEs in [34] [35].

1. The transistor MN7 should be much smaller than MN8 such that the discharging current is controlled by MN7.

2. The size of MN6 is determined as the element of the current mirror. Usually the size of MN6 can be same as MN7 However, these transistors may have different sizes to reduce the static power consumption of the DCO, as explained in [34].

3. The number of transistors (N) can be obtained from the maximum difference, which is measured and digitized by the one inverter delay in time-to-digital converter (TDC), such that bits (m) = 2^N. Moreover, the circuit
must contain one more PMOS transistor (MP5) which is always on.

4. MP5 is placed and sized to have the lowest frequency in allowed frequency range of the digitally controlled oscillator (DCO) \[34, 35\].

5. The sizes of parallel transistors (MP0 to MP10) in binary fashion, which is fragmented into N=11 from MP5. That is,

\[
\left(\frac{W}{L}\right)_{M_p} = \frac{2^{i-1}}{2^{11}}\left(\frac{W}{L}\right)_{M_5}, \quad i = 1, \cdots, 11 \quad (5.13)
\]

6. The frequencies of the circuit for all the possible input digitized code combinations are generated. If the higher resolution is needed, the higher numbers of input controlling bits are required.

These basic steps are important to design the DCO based on current mirror because the considering about determining the specific size MP5 for $I_{CTRL}$ and keeping a low static power consumption.

**5.4.4 The proposed DCO**

One of the main issues in the design of DCO, which is using the basic DCDE structure, is the impact of PVT (Process, Supply Voltage and Temperature) variations. As explained by the previous section, the DCO is based on the DCDE controlled by the current passing through the controlling transistor of the current-starved inverter. In order to have the same frequency steps, the delay
5.4 Digitally Controlled Oscillator (DCO)

The inverter of the current-starved inverter is independent of process, supply voltage and temperature. This means the controlling current should be independent of these parameters. Using the current source for the proposed DCO is based on [34]. In this paper, controlling current is independent of the above mentioned parameters (Process, Supply Voltage and Temperature) by using current sources instead of the controlling PMOS (MP5) transistor as shown in 5.21. In this circuit, the transistors (MP2 to MP10) act as current sources and the controlled current is able to be independent of PVT parameters. This technique helps reduce the impact of PVT variations.

The proposed DCO is based on the DCDEs as depicted in [34] [35]. However this DCDEs has lower frequency ranges due to the DCDEs based DCO only depends on the controlled current. The proposed DCO use a 4 to 1 multiplexer to avoid this problem. The MSB bit and MSB-1 bits determine a frequency ranges for ADPLL. If two bits are all zero, the DCO operates in 400MHz to 660MHz and otherwise the DCO operates in 660MHz to 860MHz. Since the MSB and MSB-1 bits are determined by the counter at the end of TDC, it has time margin with the filtered output of DLF. Therefore, two bits should be aligned with the filtered output of DLF to have DCO operate properly.
5.4 Digitally Controlled Oscillator (DCO)

5.4.5 The Performance of the Proposed DCO

The performance factors of DCO for ADPLL are the linearity and the power consumption. When the DCO is designed for ADPLL, these performance factors should be considered carefully because these factors affect directly the performance of DCOs and ADPLLs.

5.4.5.1 Linearity

The linear characteristic of digital-input word-to-frequency of the DCO is essential for ADPLL since the frequency of the DCO is varied according to the digital-input words. The linearity of the proposed DCO is presented in Figure 5.23.

![Figure 5.22: Linearity of Digitally Controlled Oscillator (DCO)](image-url)

Figure 5.22: Linearity of Digitally Controlled Oscillator (DCO)
5.4 Digitally Controlled Oscillator (DCO)

**Figure 5.23:** Linearity of Digitally Controlled Oscillator (DCO) from 400MHz to 660MHz

**Figure 5.24:** Linearity of Digitally Controlled Oscillator (DCO) from 660MHz to 860MHz
5.4.5.2 Power Consumption

The power consumption is very important issue for on-chip micro systems. In ADPLL, the power consumption of DCO is most important issue to have the overall power consumption low. The power consumption of the oscillator is the biggest part of the overall power consumption, especially, due to the MN5 of DCO is always on in case of the proposed DCO. The average power is 2.3mW. This is the reasonable power consumption for the proposed ADPLL. In addition, this proposed DCO has power consumption in the worst case: 3.9mW when DCO has the highest frequency and best case: 1.36mW when DCO has the lowest frequency. The proposed DCO is more power efficient than the conventional DCOs in many research papers.

![Power consumption of Digitally Controlled Oscillator (DCO)](image)

**Figure 5.25:** Power consumption of Digitally Controlled Oscillator (DCO)
Chapter 6

Simulation Results

The proposed ADPLL structure is designed and simulated using 0.18\(\mu\) CMOS technology. From the simulation diagram of the step frequency response, the proposed ADPLL has unique locking mechanism. The specifications of proposed ADPLL is as the following: the target frequency \(F_{\text{original}}\) is 800MHz, and Integer part of division (N) is 16. Since the frequency of the reference clock is 50MHz, which is

\[
\frac{F_{\text{original}}}{\text{division factor}} = \frac{800\text{MHz}}{16}
\]

Digital loop filter (DLF) is designed by the following factors; the reference clock is 50MHz, the phase margin is 48.3° and the unit gain -bandwidth is 50KHz. Total numbers of the proposed ADPLL are 11,824. The frequency acquisition time under the lock condition is \(< 5\) cycles. When the phase difference between the inputs of reference and feedback is less than \(\pm 2\pi\) of the normalized period of the reference clock, the lock-in time is less than 3 cycles. If the original clock is 800MHz, for example, the lock-in time is
Figure 6.1: The proposed ADPLL structure
6.1 Jitter Measurement

As mentioned in the previous chapter of the jitter performance, jitter performance is very important in the ADPLL because the margin-time for data set-up and hold time are crucial issues for the clock distribution in the integrated circuitry when data is written and read.

The jitter is measured through the 200 iterations using Monte Carlo Simulation for the actual clock jitter of the output of digitally controlled oscillator (DCO).

![Jitter Measurement through Monte Carlo Simulation at 700MHz](eyeDiagram: f_out)

**Figure 6.2:** Jitter measurement through Monte Carlo simulation at 700MHz
The jitter measurements under various target frequencies are dictated in Table 6.1. The jitter is 32.86ps at 700MHz and 49.93ps at 800MHz.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Jitter measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>700MHz</td>
<td>32.86ps</td>
</tr>
<tr>
<td>800MHz</td>
<td>49.93ps</td>
</tr>
</tbody>
</table>

Table 6.1: Jitter measurement under the various target frequencies

6.2 Frequency Response

The response of the frequency under time-domain is presented in Figure 6.3. As

![Frequency response graph](image)

Figure 6.3: Frequency response
discussed in previous section, the lock-in time is less than 3 cycles, equivalently < 50ns. This figure 6.3 provides that the frequency acquisition for both target frequencies at 700MHz and 800MHz is held less than 50ns. In addition, the frequency is generated by DCO. The frequency variation is approximately 0.05% where the ADPLL is under lock-in condition.

6.3 Power Consumption

The total power consumption of time-to-digital (TDC) and ADPLL is presented in Table 6.2. As seen in Table 6.2, even though the power consumption of the proposed TDC is increased compared to the conventional TDC, the total power consumption of ADPLL is decreased because the higher resolution of the proposed TDC than the conventional one decreases the number of cycles until lock-in condition of ADPLL.

<p>| Table 6.2: Comparison between the conventional LPI-TDC and the proposed LPI-TDC |
|-----------------------------------------------|-----------------|</p>
<table>
<thead>
<tr>
<th>Process</th>
<th>Conventional LPI-TDC [18]</th>
<th>Proposed LPI-TDC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>90nm / 0.18µm</td>
<td>0.18µm</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>14mW / 18.6mW</td>
<td>21.2mW @50MHz</td>
</tr>
<tr>
<td>Resolution($\frac{t_{delay}}{f}$)</td>
<td>4.7ps / 14.3ps</td>
<td>7.84ps</td>
</tr>
</tbody>
</table>
6.4 Measurement of ADPLL

The overall measurements for the proposed ADPLL are shown in Table 6.3. The proposed ADPLL is designed and simulated using Synopsys Hspice and Cadence IC design tools. Compared to ADPLL published in TVLSI’ 11 [19], the proposed ADPLL with a novel LPI-TDC based on tri-state inverter provides less power consumption, and lower jitter values in various frequency ranges. Particularly, even the proposed ADPLL is operated in higher frequency than ADPLL [19] in the jitter performance, the proposed one has lower jitter value than the ADPLL [19].

The range of frequency of the proposed ADPLL is from 400MHz to 860MHz. The linearity of DCO in the proposed ADPLL is presented in the section of digitally controlled oscillator (DCO).

<table>
<thead>
<tr>
<th>Table 6.3: Comparison between the performance of ADPLLs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process</strong></td>
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<tr>
<td>-------------</td>
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<tr>
<td><strong>Power Consumption</strong></td>
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<td></td>
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<tr>
<td><strong>Resolution</strong></td>
</tr>
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<td><strong>Jitter Performance</strong></td>
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<td></td>
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<tr>
<td><strong>Frequency Range</strong></td>
</tr>
</tbody>
</table>
Chapter 7

Conclusion

This research focuses on the analysis and design of low noise, low power and high resolution all digital phase-locked loop. Using the theory and circuits developed, a fully digital All-digital phase-locked loop with a novel local passive interpolation time-to-digital converter (LPI-TDC) based on a tri-state inverter is designed in 0.18\(\mu\text{m}\) technology. Efforts have been put on the new design of phase acquisition process, digitally controlled oscillator, and time-to-digital converter. Several key research contributions are highlighted.

(1) Develop an all-digital PLL utilizing the LPI-TDC based on a tri-state inverter with a comparable jitter performance.

(2) The proposed ADPLL is demonstrated to operate from 400MHz and 860MHz. A unique frequency and phase acquisition process is presented. The proposed ADPLL is locked within less than original reference 80 clock cycles.
(3) In the aspect of power consumption, the proposed ADPLL has 43.37mW at 700MHz. This ADPLL consumes the power 12% less than the conventional ADPLL with LPI-TDC based on the multiplexers. In addition, this power consumption is comparable with other types of ADPLLs.

(3) Replaced the Delay-cell from the multiplexers based LPI-TDC into a tri-state inverter based LPI-TDC. This development results in not only a higher resolution by 1.5 times but also smaller number of CMOS gate and reduced dummy signal connections than conventional LPI-TDC based on the multiplexers.

(4) As an entirely digital implementation, it is portable and scalable for other process and low supply voltage operation. Besides, the proposed delay-cell in LPI-TDC is exploited to obtain high performance and low power consumption. Other parts in the proposed ADPLL such as DLF and DCO are implemented to reduce jitter, and to generate a proper frequency through accurate digitized control words. The proposed ADPLL performs better than the conventional ones, and it will be a good reference for the future work.
Bibliography


[9] W.H. Chen, M.E. Inerowicz, and B.H. Jung. Phase frequency detector with minimal blind zone for fast frequency acquisition. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, Vol. 57(No. 12):Pages 936–940, Dec. 2010. [61] [52] [53] [54] [55] [56] [57] [58] [59] [60] [61] [62]


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