Dual-Edge Triggered Pulsed Flip-Flop With High Performance And
High Soft-Error Tolerance

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ABSTRACT

Flip-flops are critical timing elements in digital circuits which have a large impact on circuit speed and power consumption. The performance of the Flip-Flop is an important element to determine the performance of the whole synchronous circuit. In this thesis, a dual-edge triggered flip-flop with high performance and high soft-error tolerance is designed. Pulse-triggered flip-flops employ time borrowing across cycle boundaries which results in zero or negative setup time. Moreover, the pulse generator can be shared among many flip-flops to reduce the power dissipation and chip area. Pulse generator provides a narrow window to the latching stage during which the flip-flop is in the transparent mode. By reducing this pulse width, the setup time and hold time of the flip-flop are reduced. In recent years, there has been an increasing demand for high-speed digital circuits at low power consumption. The use of dual edge-triggered flip-flops can help reduce the clock frequency to half of the single edge-triggered flip-flops while maintaining the same data throughput, this thereafter translates to better performance in terms of both power dissipation and speed. With the increasing of the transistor densities and the technology scaling, the circuits are more and more sensitive to the externally induced phenomena called soft-error. The occurrence of this kind of faults will affect the integrity of the data, and the flip-flop can cause malfunction. It is critical to design integrated circuit with high soft-error tolerance. Comparing to other flip-flops in the latest publications, the Clock-to-Q delay, setup time, hold time and power consumption of this flip-flop are all smaller and the critical charge of the flip-flop is increased significantly resulting in much better hardness against alpha particle hits. Moreover, a scan chain algorithm used to test faults in combinational logic is proposed using the dual-edge triggered flip-flop along with the scan control signal incorporation in this thesis. The result of the simulation demonstrates that this dual-edge triggered flip-flop is a viable means to improve design performance and to ease the strict and tight timing budget.
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Chapter 1

Introduction

1.1 Background

In the past decades, Moore’s law drives the VLSI technology to continuously increase the transistor densities, there are hundreds millions of transistors or even billions of transistors on a chip today, which results in that the power consumption of VLSI chip has constantly been increasing. Although the capacitances and the power supply scale down meanwhile, the power consumption of the VLSI chip is still increasing continuously.

Flip-Flops are extremely important circuit elements in all synchronous VLSI circuits. They are not only responsible for the correct timing, functionality and performance of the chip, but also they and other clock distribution networks consume a significant portion of the total power of the circuit. It is estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power [1]. Comparing to different elements in the VLSI circuits, flip-flops are the primary source of the power consumption in synchronous system. Moreover, flip-flops have a large impact on circuit speed. The performance of the Flip-Flop is an important element to determine the performance of the whole circuit. For example, the Clock-to-Q delay, Setup time and Hold time, all these parameters of the flip-flops can affect the performance of the whole circuit. Therefore, the studies on Flip-Flop become more and more in recent years.

With the increasing of the transistor densities and the technology scaling, the circuits are more and more sensitive to the externally induced phenomena, which we usually called soft-error. Due to the lower Vdd and the smaller node capacitance, the amount of charge stored on a circuit node is becoming increasingly smaller, the result of this is that the circuits have become more susceptible to spurious voltage variations caused by externally induced phenomena, the occurrence of this kind of faults will affect the integrity of the data, and the flip-flop will cause malfunction. In industry, the cost for avoiding the transient faults is significant every year. So how to design a circuit which can have a high soft-error tolerance is very popular today.
1.2 Problem Statement

Power consumption and timing delays are the two important design parameters in high speed VLSI systems. In many digital very large scale integration (VLSI) designs, the clock system that includes clock distribution network and flip-flops, is one of the most power consumption components. It accounts for 30% to 60% of the total system power, where 90% of which is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop [1]. As clock frequency increases, the latency of the flip-flop or latch will play an even greater role in the overall cycle time.

A Flip-Flop that synchronizes the state changes during a clock pulse transition is the edge-triggered flip-flop. When the clock pulse input exceeds a specific threshold level, the inputs are locked out and the flip-flop is not affected by further changes in the inputs until the clock pulse returns to 0 and another pulse occurs. As the clock frequency increase, pulse-triggered flip-flop tends to be popular as compared to conventional master-slave flip-flops. Because they employ time borrowing across cycle boundaries which results in zero or negative setup time. Moreover, the number of transistors we used in the pulse-triggered flip-flop is less than the number we used in the conventional master-slave flip-flops, so the simple structure of the pulse-triggered flip-flop leads to a better power efficiency.

In recent years, there has been an increasing demand for high-speed digital circuits at low power consumption. Because the clock frequency is determined by system specifications, the clock signal is constantly active, it makes timing components (latches and flip-flops) the most power consuming components in the VLSI system [2]. Like the single-edge triggered flip-flop, the output of the flip-flop will follow the input D at the edge of the clock, the difference is that the dual-edge triggered flip-flop will cause a transition on both the positive edge of the clock pulse and the negative edge of the clock pulse. On the rising edge of the clock and the falling edge of the clock, the output is given the value of the D input at that moment. The output can only change at the clock edge, and if the input changes at other times, the output will be unaffected. The used of dual edge-triggered flip-flops can help to reduce the clock frequency to half that of the single edge-triggered flip-flops while maintaining the same data throughput [3]. In other words, the dual-edge triggered flip-flop requires a lower clock frequency than the single-edge triggered flip-flop to achieve comparable performance [4-8]. Therefore, the dual edge triggered flip-flop offers the same data throughput of single edge-trigger flip-flops at half of the clock frequency, this thereafter translates to better performance in terms of both power dissipation and speed.
1.3 Outline of the thesis

In this thesis, a dual-edge triggered flip-flop with high soft-error tolerance and high performance is designed. In chapter 2, some state-of-the-art dual edge triggered flip-flops are reviewed. In chapter 3, a dual-edge triggered flip-flop with higher performance is proposed, and then we will introduce the definition of the soft-error and try to increase the soft-error tolerance of the flip-flop in the thesis. The PVT variations of the flip-flop will be shown in this chapter, and then we will analyze these parameters. The chapter 4 is the application of this dual-edge triggered flip-flop. In this chapter, a scan chain using this flip-flop is designed, in order to prove that this scan chain can work correctly, we will test a combinational logic using this scan chain, from the result of the test, we can show that this testability circuit can work very well. This chapter 5 is the conclusion of this thesis.
Chapter 2

Review of State-of-The-Art Dual-Edge Triggered Flip-Flops

Dual-Edge triggered flip-flops consists of pulse generator and a latch that captures the pulse, some dual-edge triggered flip-flops have an additional sensing stage to accelerate the speed of the flip-flops. In recent years, several low-power high-speed dual-edge triggered flip-flop structures have been proposed [15-22,9,11,12,14] Here, we study some state-of-the-art dual-edge triggered flip-flops which are in the recently reported publications.

2.1 Explicit-Pulse Data-Close-to-Output Flip-Flop[9]

Fig.1 and Fig.2 show the schematic of the Explicit-Pulse Data-Close-to-Output flip-flop (ep-DCO) which is considered as one of the fastest flip-flops due to its semi-dynamic nature [9]. Fig.1 is the pulse generator of the Explicit-Pulse Data-Close-to-Output flip-flop. It uses the delay of three inverters to generate the pulse at the double edge of the clock. In the ep-DCO, there are two stages, the first stage is dynamic and the second stage is static. The clock pulse drives three transistors-M1,M3 and M5. The input data is connected to M2 and the circuit captures the data through M2. When the flip-flop is transparent, the input data propagates to the output, after the transparent period, M3 and M5 will turn off because of the low voltage of the pulse, at the same time, point X change to the high voltage because that M1 is on at this time. So M4 is off after the transparent period. Hence, any change at the input cannot be passed to the output.

Now, we begin to analyze the disadvantages of Explicit-Pulse Data-Close-to-Output flip-flop. The internal node X will be charged or discharged at every clock cycle especially when the input data does not change, a lot of power is consumed at this point. Moreover, while the output is high, the repeated charging/discharging of node X in each clock cycle causes glitches to appear at the output. These glitches propagate to the driven gates not only to increase their switching power consumption but also to cause noise problems that may lead to system malfunctioning.[10]
2.2 Dual-Edge Triggered Static Pulsed Flip-Flop[11]

Figure 3 is the schematic of the dual-edge triggered static pulsed flip-flop. Four inverters in the pulse generator are used to generate the delayed signals. Two NMOS transistor are controlled by the different delayed pulse and generate a narrow sampling window at both the rising edge of the clock and the falling edge of the clock. After generating the narrow pulse, the two NMOS transistor in the static latch, N1 and
N2, are turned on by the pulse in a very short time. At this time, the input data can be captured by the static latch, so notes SB and RB will be charged or discharged which is determined by the input data. A smaller delay can be obtained because D and DB directly provide the signal to RB and SB respectively. Two PMOS transistors P1 and P2 transfer the Vdd to RB and SB respectively and two NMOS transistors N3 and N4 can connect GND to RB and SB respectively if they are on. So P1, P2, N3 and N4 can effectively avoid the floating of the nodes RB and SB. The size of N3 and N4 should be small in order to make the Clock-to-Q delay to be smaller.

Now, we begin to analyze the disadvantages of the dual-edge triggered static pulsed flip-flop. Because capacitive loads at nodes RB and SB are very large, the flip-flop latency may be degraded. Moreover, because there is a high-voltage drop across either transistor N3 or N4 when they are off, they dual-edge triggered static pulsed flip-flop suffers from high leakage current.

Figure 3. Dual edge-triggered static pulsed flip-flop (DSPFF): (a) dual pulse generator (b) static latch.
2.3 Adaptive Clocking Dual-Edge Sense-Amplifier Flip-Flop

[12]

Figure 4 is the schematic diagram of the adaptive clocking dual-edge sense-amplifier flip-flop. As seen in the figure, it consists three stages: the adaptive clock inverting stage, the front-end sensing stage and the Nikolic’s latch [13] stage. The adaptive clocking inverter chain is designed to disable some transistors in the chain when the data switching activity is low. The node NC in the sensing stage is design to generate adaptive clocking. When the output and input data are same, NC will become to be
low voltage and turn off the NMOS transistors N1 and N2, the adaptive clocking inverter chain will generate a pulse. When the output of the flip-flop and input data are different, it will become to be high voltage and turn on the NMOS transistor N1 and N2, then a pulse will be generated. Therefore, the adaptive clocking inverter chain will generate the pulse or will not generate the pulse according to the input and output of the flip-flop. During the transparent period of the adaptive clocking dual-edge sense-amplifier flip-flop, either SB or RB will be discharged due to the input data. Then the output of the flip-flop will be changed in the latching stage.

Now, we begin to analyze the disadvantages of the adaptive clocking dual-edge sense-amplifier flip-flop. As seen in the figure, the adaptive clocking dual-edge sense-amplifier flip-flop requires more transistors to realize the adaptive clocking, and the circuit is very complex, so the speed of the flip-flop will be slower; Moreover, if the switching activity of the circuit is very high, the adaptive clocking dual-edge sense-amplifier flip-flop will consume a lot of power due to the more used transistors in the circuit.

### 2. 4 Dual-Edge Triggered Sense-Amplifier Flip-Flop [14]

The schematic diagram of dual-edge triggered sense-amplifier flip-flop is presented in Figure 5. In the dual-edge triggered sense-amplifier flip-flop, there are three stages: the pulse generating stage, the sensing stage and the latching stage. The pulse generator in this flip-flop is the same as the pulse generator in [23]. This dual-edge triggered pulse generator can generate the pulse at both the rising edge and falling edge of the clock. For a sense amplifier based flip-flop, when input data is high, RB will connect to Vdd and to be set to high, when input data is low, SB will connect to Vdd and to be set to high. When pulse is high, RB will follow D and SB will follow DB, although this structure can help reduce discharging time, it has some disadvantage and we will analyze it in the following paragraph. Similar to the Nikolic’s latch[13] and Strollo’s latch[24], the new latch makes use of SB and RB to pull up the output nodes. When SB is low, output Q will be high, when RB is low, QB will be high. In this latching stage, there are two pulse-controlled NMOS pass transistor, these two transistors can let D and DB feed to Q and QB directly. This is the advantage of this structure. Because under the help of D and DB, Q and QB can get to high voltage of low voltage quicker, this can help decrease the Clock-to-Q delay of the flip-flop. The four transistors LP3, LP4, LN3, and LN4 are used to hold the data in the flip-flop and maintain the output state when there is no pulse.

Now we begin to analyze the disadvantage of the dual-edge triggered sense-amplifier flip-flop. In the pulse generator, the two inverters are used to generate delay for the clock, when the clock is from 0 to 1(rising edge), because of the delay of the inverters,
CLK2 cannot change from 0 to 1 immediately when CLK gets to 1, so there is a short time that when CLK is 1, CLK2 is 0. At this time, CP4 is on and the voltage of CLK will be transferred to pulse, so pulse can get to Vdd, then the pulse will drop down because CN3 is on at this time and CLK1 is low, but when pulse is rising, CN3 is already on and the voltage of pulse will drop, because CLK1 can finish to change from 1 to 0 when pulse is rising, the pulse cannot get to Vdd and magnitude of the pulse will be lower than Vdd. If we use this pulse generator to drive more flip-flops, it is possible that the magnitude of the pulse cannot get to the value which can open the NMOS in the sensing stage and latch.

In the sensing stage of the flip-flop, when there is no pulse fed by the pulse generator and input data D is high, point SB will be floating, if the frequency of the clock is very low and D remains high for n cycles, the charges stored in point SB will leak out and SB will drop down from high voltage to low voltage, in this case, the logic of the flip-flop will be wrong. This structure of the sensing stage assumes that the frequency of the clock is very high and even if the point SB is floating, the voltage at point SB will keep high and will never drop down in this case.

Figure 5. Dual edge-triggered sense-amplifier flip-flop: (a) dual pulse generator; (b) sensing stage (c) symmetric latch.
Chapter 3

Design of Dual-Edge Triggered Pulsed Flip-Flops with high performance and high soft-error tolerance

3.1 Design of Dual-Edge Triggered Flip-Flop With High Performance

In this section, a dual-edge triggered flip-flop with high performance is proposed. In this flip-flop, there are two stages: dual-edge triggered pulse generator stage and latching stage. Comparing to the flip-flops which are in the latest publications, the pulse generator in this thesis can generate narrower pulse at both the rising edge and falling edge of the clock, and the pulse magnitude can still get to the Vdd rather than the pulse in [14] that cannot get to Vdd. This character can effectively reduce the setup time and hold time of the flip-flop. In the latching stage, the output of the latch can follow the input data quickly when there is a pulse, because the D and DB can help the Q and QB charge or discharge directly, this architecture can reduce the Clock-to-Q delay effectively and improve the performance of the flip-flop. In the following section, we will introduce and discuss this novel dual-edge triggered flip-flop in details.

3.1.1 Design of Dual-Edge Triggered Pulse Generator

When we plan to design a dual-edge triggered pulse generator, the most commonly used method is to use the inverter to generate the clock delay and use this little difference of the clock to generate the pulse. This pulse generator has improved two disadvantages of the pulse generator in the [23]. The first improvement is that this pulse generator can produce two narrower pulses at both the rising edge and falling edge of the clock, this can help the flip-flop reduce the setup time and hold time
effectively. The second improvement is that this pulse generator can produce a pulse which can get to the Vdd, however, the pulse that produced in [23] cannot get to the Vdd, when we use this pulse generator to drive more latches, this improvement is very important.

Now we begin to analyze this pulse generator and discuss how it works. When CLK is from low to high (rising edge of the clock), because of the delay which is generated by two inverters, the voltage of CLK2 is still low and CLK3 is still high, at this time, transistor N1 is on and P1 is off because of the high voltage of the CLK, transistor P2 is on because of the low voltage of CLK2, transistor N2 is on because of the high voltage of the CLK3, so the transistors N1, N2, P1 will transfer the high voltage to the point pulse, and pulse will rise at this time. After a very short time, the voltage of CLK2 will change to be high and the voltage of CLK3 will change to be low, transistor P1 is still off and transistor N1 is still on, but transistor P2 will turn off because of the high voltage of the CLK2, and transistor N2 will turn off because of the low voltage of CLK3, so the pulse will fall down at this time. In this very short period of time, this pulse generator generates a pulse at the rising edge of the clock.

Figure 6. Dual-Edge Triggered Pulse Generator
When CLK is from high to low (falling edge of the clock), because of the delay which is generated by the two inverters, the voltage of CLK2 is still high, at this time, transistor P1 is on and transistor N1 is off because of the low voltage of the CLK, transistor P2 is off because of the high voltage of CLK2, transistor N2 is off because of the low voltage of CLK3, so the transistor P1 will transfer the voltage of CLK2 to the point pulse, and pulse will rise to the Vdd. After a very short time, the voltage of CLK2 will change to be low, and the voltage of CLK3 will change to be high, at this time, transistor P1 is still on and transistor N1 is still off, however, transistor P2 will turn on and transistor N2 will turn on, so transistors P1, P2, N2 will transfer the voltage of CLK to the point pulse, although the transistors P1 and P2 are not good candidates for transferring the low voltage, they can help the pulse to fall down quickly, and transistor N2 can help the pulse go the voltage of zero volt. In this very short period of time, this pulse generator generates a pulse at the falling edge of the clock.

Figure 7. Pulse of the flip-flop
Figure 7 is the pulse which is generated by the pulse generator. We use the Hspice to simulate the flip-flop, the power supply is 1.1 volt here. In figure 7, we can see that the pulse generator generates two very narrow pulses at the rising edge and falling edge of the clock. And the pulses can still get to the Vdd. So this pulse can help the flip-flop reduce the setup time and hold time effectively because of the narrow pulse of the flip-flop. About the measurement of the setup time and hold time of the flip-flop, we will discuss in the following chapters. We do not discuss it in details here. Moreover, because there are more than one transistors to transfer the high voltage or low voltage of the clock to the point pulse, the pulse rises and falls quickly, and the Clock-to-Q delay is very small.

### 3.1.2 The Comparison between Proposed Pulse Generator And The Pulse Generator In The Latest Publication

![Pulse comparison](image_url)

Figure.8. Pulse comparison with the pulse in [14]
To demonstrate the advantage said before, we use the pulse generator in the latest publication to compare the pulse generator in this thesis. The comparison of the pulse between the pulse proposed in this thesis and the pulse in [14] is shown in the Figure 8. Both of the flip-flops are optimized in size and simulated under the same temperature (25°C) and same power supply (1.1v). On the top of Figure 8, there is a clock and we can see that both of the pulse generators generate two pulses at the rising edge and falling edge of the clock. In the middle of Figure 8, it is the pulse which is generated by the pulse generator that proposed in this thesis. We can see that the width of the pulse is 29.4ps and the magnitude of the pulse is 1.085 volt. In the bottom of the figure, it is the pulse which is generated by the pulse generator [14], we can see that the width of the pulse is 38ps, and the magnitude of the pulse in [14] is 1.06 volt.

From the comparison between the pulse that generated by the flip-flop in the thesis and the pulse that generated by the flip-flop in [14], we can see that the width of the pulse in this thesis has reduced 22.6% and the magnitude of the pulse in this thesis has increased 0.025 volt.

From Figure 6 we can see that the pulse generator in this thesis only has one more transistor than the pulse generator in [14], why can the pulse generator generate a better pulse than the pulse of the dual-edge triggered sense amplifier flip-flop [14]?
We should analyze the little difference between the delay and transistor size of the inverters in the pulse generators. We first analyze the pulse generator in [14]. When CLK is from high to low (falling edge of the clock), because of the delay which is generated by the two inverters, the voltage of CLK1 is still low and the voltage of CLK2 is still high. At this time, transistor CP3 is on and transistor CN3 is off, transistor CP4 is off and transistor CN4 is off. So transistor CP3 will transfer the voltage of CLK2 to the point PULS, and pulse can rise at this time. After a very short period of time, the voltage of CLK1 will change to be high and the voltage of CLK2 is still high because of the delay of the second inverter. At this time, transistor CP3 is on and transistor CN3 is off, transistor CP4 is off but transistor CN4 is on, so transistor CN4 will transfer the voltage of CLK to the point PULS, and transistor CP3 can still transfer the voltage of CLK2 to the point PULS, although the voltage of the CLK2 is high, the voltage of the CLK is low, so turning on of the CN4 at this time has a bad effect on the magnitude of the pulse, and the pulse generator in [14] cannot generate a pulse that can reach at Vdd at the falling edge of the clock. Moreover, in order to increase the magnitude of the pulse at the falling edge of the clock, we must increase the delay of the first inverter as big as possible and decrease the delay of the second inverter as small as possible, in this way, the magnitude of the pulse can be increased in maximum extent. In other words, we must make the first inverter to be very slow, and the total delay of the two inverters are very big, so the rising time for the pulse is very big and it still cannot rise to the Vdd, the pulse width will be very big because of the long time for the rising time of the pulse. Through the analysis above, we can know the disadvantage of the pulse generator in [14]. Just because of these
disadvantages, we add one more inverter in the pulse generator in the thesis. In this way, we can change the delay of each CLK which is received by transistors, and we can also change the size of the first inverter, in this way, we can change the pulse width of the flip-flop.

Now we begin to analyze the advantage for adding this one more transistor in the pulse generator of this thesis in Figure 6. When the CLK is from high to low (falling edge of the clock), because of the delay which is generated by the three inverters, the voltage of CLK2 is still high and the voltage of the CLK3 is still low, at this time, transistor P1 is on and transistor N1 is off, transistor P2 is off and transistor N2 is off, at this time, only transistor P1 is on and it will transfer the voltage of the CLK2 to the point pulse, because the voltage of CLK2 is high at this time, the voltage of the pulse will rise. After a very short period of time, the voltage of CLK2 will change to be low and the voltage of CLK3 is still low, this is the difference between the pulse generator in this thesis and the pulse generator in [14]. Because the transistor N2 will turn on after the voltage of CLK2 change from high to low, N2 will now has a bad effect on the magnitude of the pulse at this time. So the magnitude of the pulse can get to the Vdd at the falling edge of the clock. This is one improvement in this thesis. The second advantage of this one more inverter is that because we do not need to make the delay of the first inverter as big as possible, we can make the first transistor faster than that in [14], the total delay of the first and second inverters will change to be smaller. So the rising time of the pulse will change to be smaller and the pulse will rise faster at the falling edge of the clock. Because the rising time of the pulse has reduced effectively, the pulse width of the flip-flop in this thesis will change to be narrower, this is the second improvement in this thesis and it can reduce the setup time and hold time of the flip-flop effectively. About the improvement of the setup time and hold time, we will discuss and compare in the following chapters. We will not discuss it in details here.

3.1.3 The Output Of The Pulse Generator Working In Different Process Corners

In semiconductor manufacturing, a process corner refers to a variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer. Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly. If the circuit does not function at all at any of these process extremes the design is considered to have inadequate design margin [25]. An intentional pulse is used to sample the input around an edge. Generally, the design of such circuits requires careful timing analysis.
across all process corners [26]. So it is possible that in certain corner, the pulse generator cannot work normally. For example, it is possible that the magnitude of the pulse cannot reach at a certain value, and the pulse cannot be used by the latch or the pulse cannot get to the zero volt because of the low voltage of the pulse. So whether the pulse generator can work in certain is an important element for the pulse generator.

![Figure 9. Pulse generator working in FF corner](image)

From Figure 9 we can see that the magnitude of the pulse at falling edge of the clock is about 1.05 volt, the magnitude of the pulse at the rising edge of the clock is a little higher than that of the falling edge of the clock, because in FF corner, the parameters of the transistors are different with the parameters in the nominal corner, under the
same temperature and power supply as that of the nominal corner, the speed of PMOS and NMOS are different with that of the nominal corner. Because the power supply we gave is 1.1 volt, this pulse generator can work correctly in FF corner. Moreover, this pulse generator can generate two narrow pulses at the rising edge and falling edge of the clock.

Figure 10 is the output of the pulse generator which is working in FS corner. From the figure we can see that the magnitude of the pulse at the falling edge of the clock is about 1.06 volt. Because in the FS corner, the NMOSs are working in fast corner and the PMOSs are working in slow corner, the parameters of the transistors are different from the parameters of the transistors which are working in the nominal corner. So the magnitude of the pulse at the rising edge and falling edge of the clock has a little difference. In Figure 6 we can see that, when at the rising edge of the clock and the falling edge of the clock, the pulse generator uses different transistors to transfer the high voltage to the point pulse, the in FS corner, it is reasonable that the two pulse
which are at the rising edge of the clock and the falling edge of the clock have different magnitude. If we observe this Figure carefully, we can see that the width of the pulse at the rising edge of the clock and the falling edge of the clock is a little different, the pulse at the falling edge of the clock is a little wider, but the magnitude of both of the pulse can reach a certain value which can maintain the flip-flop work correctly. Moreover, the 1.06 volt magnitude at the falling edge of the clock basically has no bad effect on the output of the flip-flop, this pulse generator is still a good candidate to generate the pulse for the flip-flop.

![Figure.11. Pulse generator working in SF corner](image)

When the pulse generator is working in the SF corner, the output of the pulse generator is proposed in the Figure 11. In the figure, we can see that the pulse generator can still generate two narrow pulses at the rising edge of the clock and the falling edge of the clock. In the lower half of the figure, we can see that the magnitude of the pulse at the falling edge of the clock is about 1.09 volt and the pulse at the
rising edge of the clock is a little higher than 1.1 volt. We can also see that the pulse at
the falling edge of the clock is a little narrower than that of the pulse at the rising edge
of the clock. But in the SF corner, this little difference with the pulse of the flip-flop
which is working in nominal corner has eligible effect on the output of the flip-flop.
This pulse generator is still a good candidate for the flip-flop to generate the pulses in
the SF corner.

![Figure 12. Pulse generator working in SS corner](image)

Figure 12 is the pulse which is generated by the pulse generator of the flip-flop
working in SS corner. When the flip-flop is working in SS corner, it means that both
the NMOSs and PMOSs are working in the SS corner. So the parameters of the
transistors have changed and it will run slower than the flip-flop which is working in
nominal corner. In Figure 12, comparing with the pulse generator that is working in
nominal corner, we can see that both the magnitude and the width of the pulse have
changed. The magnitude of pulse at the falling edge of the clock is about 1.09 volt and
the magnitude of the pulse at the rising edge of the clock is a little higher than 1.1 volt.
Moreover, the width of the pulse at the falling edge of the clock is a little wider than the pulse at the rising edge of the clock. But all these little difference will not affect the flip-flop and it can still work correctly. Because even if the width of the pulse at the falling edge of the clock has changed to be wider, it is still narrow enough comparing with the clock and input data of the flip-flop. The magnitude of the pulse will not affect the output of the inverter and the pulse is also good enough for the flip-flop to work correctly.

3.1.4 Design of The Latching Stage With High Performance

![Latching stage diagram]

Figure.13. Latching stage
We discussed the pulse generator in the last section; this pulse generator has many advantages that can help the flip-flop improve the performance. To further improve the speed of the flip-flop, a fast symmetric latch is developed. Figure 13 is the schematic of the latching stage of the flip-flop.

One big difference of this latching stage with other latch is that the input D and $\overline{D}$ can help charge or discharge Q and $\overline{Q}$ directly, in this way, the Clock-to-Q delay will reduce effectively. When the voltage of the pulse is high, if the voltage of the D is high and the voltage of $\overline{D}$ is low, transistor P1 is off and transistor P2, P3 and P4 are on, so transistor P3 and P4 will transfer the voltage Vdd to the point Q, and the output of the flip-flop Q will follow the input D to change to be high. Moreover, transistor N1 and N2 will turn on at this time, so transistor N1 can transfer the low voltage to the point $\overline{Q}$ and transistor N2 will transfer the high voltage to the point Q, although transistor N2 is not a good candidate for transferring the high voltage, it can help the point Q accelerate to go from low voltage to high voltage. This structure can help the flip-flop reduce the Clock-to-Q delay at the low-to-high transition of the output Q. In the whole process of the low-to-high transition of the output Q, because of the voltage of the pulse is high, transistors P5 and P7 turn off, so the two inverters which are composed by transistor P6 and N3, transistor P8 and N4 stop working, in this way, we can save more power when the output is following the input D.

When the voltage of the pulse is high, if the voltage of the D is low and the voltage of $\overline{D}$ is high, transistor P3 is off and transistor P1, P2 and P4 are on, so transistor P1 and P2 will transfer the voltage Vdd to the point $\overline{Q}$, at this time, transistor N1 and N2 are turning on and they will transfer the voltage of D and $\overline{D}$ to the point Q and $\overline{Q}$ respectively. Because the voltage of D is low, the voltage of Q will change to be low. At the high-to-low transition of the output Q, the input data discharge the point Q directly, so the Clock-to-Q delay is very small. In the whole process of the high-to-low transition of the output Q, because of the voltage of the pulse is high, transistors P5 and P7 turn off, so the two inverters which are composed by transistor P6 and N3, transistor P8 and N4 stop working, in this way, we can save more power when the output is following the input D.

When the voltage of the pulse is low, transistors P2, P4, N1 and N2 turn off, whatever the voltage of the output is high or low, Vdd cannot be transferred to the point Q, and
The transistors N1 and N2 will not transfer the voltage of \( \overline{D} \) and D to the point \( \overline{Q} \) and Q either. Because of the voltage of the pulse is low, the transistors P5 and P7 will turn on, the two inverters which are composed by transistor P6 and N3, transistor P8 and N4 start working at this time. The two inverters connect in a loop, so the latching stage will hold previous status when the voltage of the pulse is low. When the voltage of the pulse change to high, then the two inverters will stop working and the output Q will follow the input data again.

<table>
<thead>
<tr>
<th>Pulse</th>
<th>D</th>
<th>Q</th>
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<tr>
<td>0</td>
<td>0</td>
<td>hold</td>
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<tr>
<td>0</td>
<td>1</td>
<td>hold</td>
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<td>1</td>
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Table.1. Truth Table of the Latching Stage

Now we begin to analyze the size of the latching stage and how can the latching stage work in the best performance. Because the structure of the latching stage is symmetric, we only discuss right half of the latching stage, and the left half of the latching stage is the same as the right half part.

We first analyze the size of the NMOS transistor N4. When the voltage of the pulse is from low to high, the PMOS transistor P7 will turn off, and the inverter which is composed by P8 and N4 will stop working, it seems that this latching stage has no conflict between N4 and P3, P4 which usually exist in the common latch in other papers, however, when we scrutinize the latching stage, we will find that the point between transistors P7 and P8 is floating when the voltage of the pulse is low, and the voltage at this point will discharge for a short time, in other words, the inverter that composed by P8 and N4 will work for a short time after the voltage of the pulse change from high to low. So there is still a conflict between N4 and P3, P4. In order to
make the Clock-to-Q delay to be small, the size of NMOS transistor N4 should be small enough comparing with the size of P3 and P4, in this way, when transistors P3 and P4 are on, the voltage of the point Q can change to be high quickly.

Now we discuss the size of transistor P8 in order to improve the performance of the flip-flop. When the voltage of the point Q is from low to high, the voltage of D is high and the voltage of pulse is low. At this time, the voltage at the source of P8 decreases because P7 is turning off. The voltage at the drain of P8 is high and the voltage at the gate of P8 is low. At this time the transistor P8 is on but the current will flows from the drain of P8 to the source of P8, because the voltage at drain of P8 is higher than the voltage at the source of P8. If the size of P8 is small, the capacitance at the source of P8 will be small, then the capacitance can store less charges. So it is easier for point Q to get to the high voltage because less charge will flow from the point Q to the source of P8. If the size of P8 is big, point Q needs to provide more charges to the source of P8, and the rising time of point Q will be longer.

The size of transistor P7 should not be too big. Because of the capacitance at the source of P8, we have discussed that the capacitance at the source of P8 should be small in order to accelerate the low-to-high transition of point Q. But the size of M7 should be big enough that when the voltage of pulse is low, the voltage at the source of P8 can get to Vdd quickly, So the inverter can start working quickly.

Then we will discuss the size of transistor P4. We assume that the capacitance at the drain of P4 is C1 and the capacitance at the source of P4 is C2. After analyzing the size of P7, P8 and N4, we know that the size of transistors that connect to C1 are all very small, so C1 is very small. If C2 is big, when the voltage of pulse is high, transistor P4 turns on, C1 and C2 connect together, there is going to be a current between C1 and C2, because the charges in C1 and C2 should be equivalent. Therefore, the output of the flip-flop Q will have a little vibration because of the flowing current, if C2 is small, the current will be small and then the vibration will be small, but the size of P4 cannot be too small, because P4 needs to transfer the voltage of Vdd and let the point Q get to the high voltage quickly, if the size is too small, the speed of P4 will be slow, the Clock-to-Q delay will be longer.

Transistor N2 is a NMOS, the size of N2 should be smaller than P4. Because the transistor N2 can help point Q get to high voltage when the voltage of D is high and the voltage of pulse is high, and help point Q get to low voltage when the voltage of D is low and the voltage of pulse is high, the size of N2 should not be too small, because it needs to transfer the voltage, the speed of N2 is also very important.

The size of transistor P3 should not be too big, because C2 should be small which we discussed before, but the size of P3 should be big enough that when the voltage of D is high and the voltage of pulse is high, the drain of P3 can get to the high voltage quickly, this is good for reducing the Clock-to-Q delay of the flip-flop.
3.2 Design of Dual-Edge Triggered Flip-Flop With High Soft-Error Tolerance

In recent years, the density of the integrated circuits are becoming higher and higher. As the technology we used in the industry manufacturing scales down to the deep submicron/nano ranges, the circuits are more sensitive to the externally induced phenomena, which we usually called it soft-error. In this section, a dual-edge triggered flip-flop with high soft-error tolerance is designed. We will discuss the related contents in the following sections.

3.2.1 Introduction to The Soft Error

As the development of the technology, the density of the chip that we produced has increased rapidly. Moreover, in order to save more power, the operating voltage has become lower and lower. All these changes bring us more portable electronic devices and it gave us a more comfortable life. However, as the dimensions and operating voltages of electronic devices are reduced to satisfy the ever-increasing demand for higher density and lower power, the circuit has become more sensitive to the externally induced phenomena. Due to the lower Vdd and the smaller node capacitance, the amount of charge stored on a circuit node is becoming increasingly smaller; the result of this is that the circuits have become more susceptible to spurious voltage variations caused by externally induced phenomena such as cosmic ray neutrons and α-particles [27]. These energy particles travel through the silicon bulk and create minority carriers that may be collected by the source/drain diffusion, thus altering the voltage value of the nodes [28]. This phenomenon is extremely bad for the flip-flop we designed in this thesis, because the output of the flip-flop need to follow the input data, if the flip-flop is sensitive to the externally phenomena, the data integrity will be affected, and the flip-flop cannot work correctly. The occurrence of this kind of fault may result in transient faults. If the transient fault is latched by a sampling element (latch), then this may result in a so-called soft-error [29]. Soft Error Rate (SER) is an important parameter which can help us make a model for the soft error, then we can calculate the critical charge and compare the critical charge of the proposed circuit to that of other circuit. All these content will be discussed in the next section. Now we need to know the definition of the Soft Error Rate. Soft Error Rate is defined as the rate at which a device encounters on a predictive basis Soft-Errors. Soft-Error occurrence is expected to be significantly higher for deep submicron/nano CMOS [30]
In the high density logic circuit, the Soft-Errors have been considered as a serious influence because it can affect the overall operating of VLSI chips. Usually, people use error detecting/correcting codes [31] to avoid the transient faults in the flip-flop. However, when the density of the circuit has increased, only a single particle can result in many errors. In industry, the cost for avoiding the transient faults is significant every year. So how to design a circuit which is a good candidate for avoiding the Soft-Error is popular in nowadays. For Soft-Errors due to transient faults affecting a sampling element, hardening has been proposed for low-cost robust design of latches [32] - [36].

### 3.2.2 Soft Error Metric

When the total energy Q of the externally induced phenomena such as the cosmic ray neutrons and [27] at a particular node is greater than the critical charge $Q_{\text{crit}}$, the soft error will occur. In other word, the critical charge $Q_{\text{crit}}$ is the minimum charge that needs to be deposited at the sensitive node of the flip-flop to change the stored bit. In the model proposed in [38] - [39], the Soft Error rate (SER) is given by

$$
\text{SER} \propto N_{\text{flux}} \times CS \times \exp\left(-\frac{Q_{\text{crit}}}{Q_s}\right)
$$

$N_{\text{flux}}$ is the intensity of the neutron flux, $CS$ is the area of the cross section of the node, $Q_s$ is the charge collection efficiency. $Q_{\text{crit}}$ is proportional to the node capacitance and the supply voltage. In the function above, because that $Q_{\text{crit}}$ has an exponential relationship with Soft Error Rate, $Q_{\text{crit}}$ is widely used as a metric for assessing the occurrence of Soft Error Rate. As we said before, the soft error occurs when the externally induced phenomena such as the cosmic ray neutrons and $\alpha$-particles at a particular node is greater than the critical charge $Q_{\text{crit}}$, so the critical charge generated on some node can be modeled as a current pulse for HSPICE simulation. Figure 14 is the equivalent circuits [37] used for simulation of (a) negative and (b) positive glitches. Figure (a) can model the case that the output of the flip-flop is high, at this time the PMOS transistor is on and NMOS transistor is off, and a Soft Error occurs at the NMOS transistor which generate a negative pulse. Figure (b) can model the case that the output of the flip-flop is low, at this time the PMOS transistor is
Figure 14. Equivalent circuits [37] used for simulation of (a) negative and (b) positive glitches.
off and NMOS transistor is on, a Soft Error occurs at the NMOS transistor which generate a positive pulse. So the critical charge is that $Q_{crit} = I \times t$.

3.2.3 Review of State-of-The-Art hardened latch

In this section, we will review one state-of-the-art and most commonly used hardened latch: Schmitt trigger based hardening latch [40].

Figure 15 (b) is the Schmitt trigger based hardening latch. Comparing it to the Figure 15 (a), this latch has only two more transistors than the normal latch. When we scrutinize the Figure 15 (b), we can realize that these two transistors compose an inverter in fact. When the voltage of CLK is high, the transmission gate A will work and transfer the voltage of the input to the output, at this time, transmission gate B will stop working and the latch will stop holding the previous status, after going though the transmission gate A, the input data will go though two inverters. The output will follow the input data. At this time, if the point Q is hit by $\alpha$-particles, the voltage at point Q maybe change effectively. If the voltage at point Q is high at this time, the voltage of the output is low, then the transistor P1 will turn on and transistor N1 will turn off. So the transistor P1 will transfer Vdd to the point Q, the voltage at point Q will keep at Vdd. If the voltage at point Q is low at this time, the voltage of the output is high, then the transistor N1 will turn on and transistor P1 will turn off. So the point Q connects to the Ground through transistor N1, and the voltage at point Q can still keep at zero. Through this procedure, this Schmitt trigger based hardening latch has increased the tolerance of the Soft-Error. In fact, when the latch is transferring the input data to the output, the effect of Soft-Error is not as big as that when the latch is holding the previous status. Because when the latch is holding the previous status, if the $\alpha$-particles are more enough and the total charge of the $\alpha$-particles are more than the charge at the point Q, the logic of the latch will change and it will never be changed back. When the voltage of clock is low, the transmission gate A will stop working and transmission gate B start working. So the latch will hold the status until the voltage of the clock change to be high. At this time, if the point Q is hit by $\alpha$-particles, the voltage at point Q maybe change effectively. If the voltage at point Q is high at this time, the voltage of the output is low, then the transistor P1 will turn on and transistor N1 will turn off. So the transistor P1 will transfer Vdd to the point Q, the voltage at point Q will keep at Vdd. If the voltage at point Q is low at this time, the voltage of the output is high, then the transistor N1 will turn on and transistor P1 will turn off. So the point Q connects to the Ground through transistor N1, and the voltage at point Q can still keep at zero. Through this procedure, this
Schmitt trigger based hardening latch has increased the tolerance of the Soft-Error when the latch is holding the previous status.

Figure 15. (a) Normal Latch (b) Schmitt trigger based hardening latch
3.2.4 Design of Dual-Edge Triggered Flip-Flop With High Soft-Error Tolerance

In this section, a dual-edge triggered flip-flop with high soft error tolerance is proposed. The pulse generator is the same as the pulse generator in 3.1.1. The latching is design on the basis of the latching stage in 3.1.4. Figure 16 is the whole circuit of this thesis: dual-edge triggered flip-flop with high performance and high soft-error tolerance. In Figure 16 (b) we can find that the soft-error masking latching stage has only six more transistors than the latching stage in 3.1.4. The little circuit which is composed by this six transistors are is put at point X, because the size of the transistors which is near point X are all very small, the capacitance at point X is also very small, the total charges stored at point X is very small, the voltage at point X is very easy to be changed by the externally induced particles; So the point X is the most sensitive point to the soft-error in the circuit.

Now we begin to analyze this soft-error masking latching stage in detail. From Figure 16 (b) we can see that most part of this latching stage is the same as the latching stage in 3.1.4. So the working principle of this latching stage is the same as the latching stage in 3.1.4. When the voltage of the pulse is high, if the voltage of the D is high and the voltage of \( \overline{D} \) is low, transistor P3 is off and transistor P4, P5 and P6 are on, so transistor P5 and P6 will transfer the voltage Vdd to the point Q, and the output of the flip-flop Q will follow the input D to change to be high. Moreover, transistor N3 and N4 will turn on at this time, so transistor N3 can transfer the low voltage to the point \( \overline{Q} \) and transistor N4 will transfer the high voltage to the point Q, although transistor N4 is not a good candidate for transferring the high voltage, it can help the point Q accelerate to go from low voltage to high voltage. This structure can help the flip-flop reduce the Clock-to-Q delay at the low-to-high transition of the output Q. In the whole process of the low-to-high transition of the output Q, because of the voltage of the pulse is high, transistors P7 and P9 turn off, so the two inverters which are composed by transistor P8 and N5, transistor P10 and N6 stop working, in this way, we can save more power when the output is following the input D.

When the voltage of the pulse is high, if the voltage of the D is low and the voltage of \( \overline{D} \) is high, transistor P5 is off and transistor P3, P4 and P6 are on, so transistor P3 and P4 will transfer the voltage Vdd to the point \( \overline{Q} \), at this time, transistor N3 and N4 are turning on and they will transfer the voltage of D and \( \overline{D} \) to the point Q and \( \overline{Q} \)
Figure 16. (a) Dual-Edge Pulse Generator (b) Soft-Error Masking Latching Stage
respectively. Because the voltage of D is low, the voltage of Q will change to be low. At the high-to-low transition of the output Q, the input data discharge the point Q directly, so the Clock-to-Q delay is very small. In the whole process of the high-to-low transition of the output Q, because of the voltage of the pulse is high, transistors P7 and P9 turn off, so the two inverters which are composed by transistor P8 and N5, transistor P10 and N6 stop working, in this way, we can save more power when the output is following the input D.

When the voltage of the pulse is low, transistors P4, P6, N3 and N4 turn off, whatever the voltage of the output is high or low, Vdd cannot be transferred to the point Q, and transistor N3 and N4 will not transfer the voltage of $\overline{D}$ and D to the point $\overline{Q}$ and Q either. Because of the voltage of the pulse is low, the transistors P7 and P9 will turn on, the two inverters which are composed by transistor P8 and N5, transistor P10 and N6 start working at this time. Because the two inverters connect in a loop, the latching stage will hold previous status when the voltage of the pulse is low. When the voltage of the pulse change to high, then the two inverters will stop working and the output Q will follow the input data again.

The only difference between the soft-error masking latching stage and the latching stage in 3.1.4 is that the soft-error masking latching stage has six more transistors than the latching stage in 3.1.4. When the voltage of the pulse is low, the flip-flop will stop sampling the input D and start to hold the previous status until the voltage of the pulse is high. The size of the transistor P11, N7, inverter 1 and inverter 2 are all very small, because we want to reduce the Clock-to-Q delay as small as possible. Now we assume that the point X is hit by $\alpha$-particles. If the voltage of the output is high, the voltage at point X is low, both outputs of the INV1 and INV2 are high voltage, so PMOS transistor P11 will turn off and NMOS transistor N7 will turn on, at this time, the point X connects to the Ground, the ability to keep the voltage at zero volt has increased at point X, so the flip-flop can have a higher tolerance of the soft-error when the output of the flip-flop is high voltage. If the voltage of the output is low, the voltage at point X is high, both outputs of the INV1 and INV2 are low voltage, so PMOS transistor P11 will turn on and NMOS transistor N7 will turn off, at this time, the point X connects to the Vdd, the Vdd can provide the high voltage continuously to the point X, so the flip-flop can have a higher tolerance of the soft-error when the output of the flip-flop is low voltage.

Figure 17 is the result of HSPICE simulation when there is a soft-error at the point of X, the upper half of the figure is the case that when the output Q is high and the voltage at point X is low, there is a occurrence of soft-error at the point X, the lower half of the figure is the case that when the output Q is low and the voltage at point X is high, there is a occurrence of soft-error at the point X.

Figure 18 is the comparison of the critical charge between different dual-edge
triggered flip-flop, we can see from the Figure 18 that after adding the six transistors to the latching stage in 3.1.4, the critical charge of the flip-flop has increased dramatically. Comparing between the latching stage in 3.1.4 and the latching stage in 3.2.4, the critical charge in the 3.2.4 has increased 117.69%.

![Figure 17. Soft-Error simulation using equivalent circuit.](image)

![Figure 18. Comparison between different circuits](image)

<table>
<thead>
<tr>
<th>Circuit Description</th>
<th>Critical Charge ($f_c$)</th>
<th>Power Consumption ($w$)</th>
<th>Clock-to-Q Delay (ps)</th>
<th>Setup Time (ps)</th>
<th>Hold Time (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual-edge triggered FF in 3.1.4</td>
<td>1.696</td>
<td>2.086E-5</td>
<td>24.465</td>
<td>-29.252</td>
<td>46.294</td>
</tr>
<tr>
<td>Dual-edge triggered FF in [14]</td>
<td>2.000</td>
<td>2.592E-5</td>
<td>28.632</td>
<td>-34.142</td>
<td>53.614</td>
</tr>
<tr>
<td>Dual-edge triggered FF in 3.2.4</td>
<td>3.692</td>
<td>2.246E-5</td>
<td>24.483</td>
<td>-28.724</td>
<td>46.737</td>
</tr>
</tbody>
</table>
From Figure 18 we can also see that the power consumption of the flip-flop in this thesis is smaller than that of the flip-flop in [14]. The main reason is that when the flip-flop is in the transparent mode, the inverters which is composed by P8, N5 and P10, N6 are stop working, because at that time, the PMOS transistor P7 and P9 turn off, so the flip-flop can save power at that time. However, the flip-flop in [14] does not have this kind of structure. When the flip-flop is in the transparent mode, the inverters which are used to hold the previous status when the flip-flop is in the hold mode still works, this is why the flip-flop in [14] will consume more power.

The reason why the flip-flop in 3.2.4 consumes more power than the flip-flop in 3.1.4 is that the flip-flop in 3.2.4 has six more transistors in the latching stage, which are used to increase the tolerance of the soft-error. But we can see that although the power consumes 7.7% more, the critical charge of the flip-flop in 3.2.4 has increased 117.69%.

Figure 19. Output of the Flip-Flop
Figure 19 is the output of this dual-edge triggered flip-flop. When we simulate this circuit by HSPICE, all signals (clock, input D) are buffered, in order to make the working environment of the flip-flop to be more realistic. On the top of the figure, it is CLK. The input D is in the middle of the figure. The output Q is the on the bottom of the figure. From Figure 19, we can see that because the CLK and D are not ideal, they are buffered before being used, the CLK and D will be affected by the output Q. But this affect is not big and it will not affect the flip-flop to work correctly.

From Figure 19 we can see, at the rising edge of the clock, the output Q rises when the voltage of the input D is high, at the falling edge of the clock, the output Q falls when the voltage of the input D is low. Through Figure 19, we can believe that this dual-edge triggered flip-flop can work very well.

3.3 PVT Variations of The Dual-Edge Triggered Flip-Flop With High Soft-Error Tolerance And High Performance

In this section, we will measure the PVT (process, voltage, temperature) of the flip-flop we designed in 3.2.4. Usually, the circuits do not work in a particular environment; all the parameters of the PVT will change within a certain range, so the performance of the flip-flop in different environments will change. This is why we want to know the effect of the PVT on the flip-flop. In this section, we will compare the clock-to-Q delay, setup time and hold time in different situations, and discuss what effects the PVT will have on the flip-flop. After knowing these, we can know whether the circuit is suitable to work in certain environment, and how the performances of the flip-flop in certain environment are.

3.3.1 Clock-to-Q Delay of the Flip-Flop in Different Power Supplies

Figure 20 is the Clock-to-Q delay of the flip-flop under 1.0v power supply, the standard power supply we gave of the flip-flop is 1.1v, but sometimes the power supply will be affected by external or internal environment and the power supply is not constant in 1.1v, sometimes it will vibrate. From Figure 20 we can see that when the flip-flop is working in all kinds of corners, the Clock-to-Q delay will increase when the temperature increase. Because the mobility of the electron will decrease when the temperature increase, the transistors will be slower when the temperature
increase. Figure 21 is the Clock-to-Q delay of the flip-flop under 1.1v power supply (standard power supply). The same as Figure 20, when the flip-flop is working in all kinds of corners, the Clock-to-Q delay will increase when the temperature increase. But we can see that in each corner, comparing to Figure 20, under the same temperature, the Clock-to-Q delay has decreased. Figure 22 is the Clock-to-Q delay of the flip-flop under 1.2v power supply. The same as Figure 21, when the flip-flop is working in all kinds of corners, the Clock-to-Q delay will increase when the temperature increase. Comparing to Figure 21, under the same corner and same temperature, the clock-to-q delay has decreased. So we can summarize that the clock-to-q delay will decrease when the power supply increase. Because

\[
I_D = \frac{\mu C_{ox}}{2(1 + \frac{V_{DS}}{E_c})} \cdot \frac{W}{L} \left[2(V_{GS} - V_t) - V_{DS}^2 \right], [41].
\]

When the power supply increase, the voltage between gate and source \( V_{GS} \) will increase, the drain current of the transistor will increase, so the circuit will charge quicker. We can also see from the three figures that when the circuit works in the FF corner, the Clock-to-Q delay is the smallest, and when the circuit works in the SS corner, the Clock-to-Q delay is the biggest.

![Figure 20. Clock-to-Q delay under 1.0v power supply](image)

<table>
<thead>
<tr>
<th>Voltage (°C)</th>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>27.817</td>
<td>21.697</td>
<td>27.889</td>
<td>26.591</td>
<td>35.698</td>
</tr>
<tr>
<td>100</td>
<td>40.418</td>
<td>29.064</td>
<td>38.979</td>
<td>38.837</td>
<td>55.135</td>
</tr>
</tbody>
</table>

\( V=1.0V \) Clock-to-Q delay
Figure. 21. Clock-to-Q delay under 1.1v power supply

<table>
<thead>
<tr>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0°C</td>
<td>21.617</td>
<td>17.69</td>
<td>21.594</td>
<td>20.78</td>
</tr>
<tr>
<td>T=100°C</td>
<td>35.121</td>
<td>25.586</td>
<td>33.329</td>
<td>33.768</td>
</tr>
</tbody>
</table>

V=1.1v Clock-to-Q delay

Figure. 22. Clock-to-Q delay under 1.2v power supply

<table>
<thead>
<tr>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0°C</td>
<td>19.735</td>
<td>16.322</td>
<td>19.536</td>
<td>18.838</td>
</tr>
<tr>
<td>T=100°C</td>
<td>31.141</td>
<td>22.968</td>
<td>29.178</td>
<td>30.152</td>
</tr>
</tbody>
</table>

V=1.2v Clock-to-Q delay
3.3.2 Clock-to-Q Delay of the Flip-Flop in Different Temperatures

Figure 23. Clock-to-Q delay under 0°C

![Figure 23. Clock-to-Q delay under 0°C](image1)

Figure 24. Clock-to-Q delay under 25°C

![Figure 24. Clock-to-Q delay under 25°C](image2)
Figure 23 is the Clock-to-Q delay of the flip-flop when the circuit works in 0°C. In each certain corner, we can see that the clock-to-q delay decrease when the power supply increase. This demonstrate our analysis in 3.3.1, because when the power supply increase, the voltage between gate and source of the transistor will increase, so the drain current of the transistor will increase, the circuit will charge quicker than the lower power supply. Figure 24 is the Clock-to-Q delay of the flip-flop when the circuit works in 25°C and Figure 25 is the Clock-to-Q delay of the flip-flop when the circuit works in 100°C. Comparing these three figures we can see that for the same process corner and same power supply, when the temperature increase, the clock-to-q delay will increase, as we said before, when the temperature increase, the mobility of the electron will decrease, the drain current of the transistor will decrease, so the circuit needs more time to be charged. The clock-to-q delay will increase. From Figure 23, Figure 24, and Figure 25, we can find that the circuit work fastest in the FF corner and work slowest in the SS corner. When circuit works in the nominal corner, FS corner and SF corner, the Clock-to-Q delay is almost the same.
3.3.3 Clock-to-Q Delay of the Flip-Flop in Different Process Corners

![Clock-to-Q delay (Nominal Corner)](image1)

Figure 26. Clock-to-Q delay in Nominal Corner

![Clock-to-Q delay (FF Corner)](image2)

Figure 27. Clock-to-Q delay in FF Corner
Figure 28. Clock-to-Q delay in FS Corner

Figure 29. Clock-to-Q delay in SF Corner
Figure 26-30 are the Clock-to-Q delays when the circuit work in the Nominal Corner, FF Corner, FS Corner, SF Corner and SS Corner respectively. In each figure, we can see that the Clock-to-Q delay will increase when the temperature increase or the when the power supply decrease. We have discussed the reason of this result before. These five figures have demonstrated that out analysis of the 3.3.1 and 3.3.2 are right. When the temperature increase, the mobility of the electron will decrease, so the drain current of the transistors will decrease, the circuit needs more time to charge or discharge, so the Clock-to-Q delay will decrease. When the power supply increase, the voltage between the gate and source of a transistor will increase, from the formula in [41], we can find that the drain current of the transistor will increase, so the circuit needs less time to charge or discharge. Moreover, after comparing the five figures, we can find that when the circuit work in the SS corner, its clock-to-q delay is the biggest, the circuit is also most sensitive to the changing of temperature and power supply. When the circuit work in the FF corner, its clock-to-q delay is the smallest, the circuit is also most insensitive to the changing of temperature and power supply.
3.3.4 Setup Time of the Flip-Flop in Different Power Supplies

Figure 31-33 are the setup time of the flip-flop when the power supply of the circuit is 1.0v, 1.1v and 1.2v respectively. In the figures, we can see that the setup time of this circuit is negative. Because of the master-slave counterparts, the edge triggered flip-flops employ time borrowing across cycle boundaries which results in zero or negative setup time [42]. The negative setup time is an advantage of this flip-flop. In Figure 31 we can see that the absolute value of the setup time increase when the temperature increase. Because

\[ I_D = v_{sat}C_{ox}W(V_{GS} - V_T - \frac{V_{DSAT}}{2}) \]

when \( E \leq E_C \), \( v = \mu_n E \),

when \( E \geq E_C \), \( v = v_{sat} = \mu_n E_C \) [26],

When the temperature increase, the mobility of the electron will decrease, if the value of \( \mu_n \) decreased, the drain current \( I_D \) will decrease, so the circuit needs more time to charge or discharge, the setup time will increase.

When we scrutinize the Figures 31-33, we can find that when the temperature is 0°C, the setup time has changed very small if the power supply changed, it is possible that the circuit is in the velocity saturation in that situation, so whatever the power supply has changed, \( v = v_{sat} = \mu_n E_C \). In other words, the drain current of the transistors in this situation is almost a constant, so whatever the power supply has increased of decreased, the drain current of the transistor will not change. So the time that the circuit needs to charge or discharge will not change. So the setup time of the flip-flop in this situation has almost not changed.

When we compare between the Figure 31, Figure 32 and Figure 33, we can find that in a certain process corner, especially when the circuit works in 100°C, it is obviously that the setup time will decrease if the power supply increase. Because when the power supply increases, the voltage between gate and source of a MOS transistor increase, so the drain current of the transistor will increase. The circuit needs less time to charge or discharge, so the setup of the flip-flop will decrease when the power supply increase.
Figure 31. Setup Time under 1.0v Power Supply

Figure 32. Setup Time under 1.1v Power Supply
### 3.3.5 Setup Time of the Flip-Flop in Different Temperatures

![Graph showing setup time under different voltages and temperatures](image)

<table>
<thead>
<tr>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0°C</td>
<td>-27.932</td>
<td>-25.209</td>
<td>-22.987</td>
<td>-33.278</td>
</tr>
</tbody>
</table>

![Graph showing setup time under 0°C](image)

<table>
<thead>
<tr>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V=1.0v</td>
<td>-30.317</td>
<td>-27.124</td>
<td>-23.419</td>
<td>-36.414</td>
</tr>
<tr>
<td>V=1.1v</td>
<td>-28.43</td>
<td>-26.101</td>
<td>-23.257</td>
<td>-34.315</td>
</tr>
<tr>
<td>V=1.2v</td>
<td>-27.932</td>
<td>-25.209</td>
<td>-22.987</td>
<td>-33.278</td>
</tr>
</tbody>
</table>

**Figure 33. Setup Time under 1.2v Power Supply**

**Figure 34. Setup Time under 0°C**
Figure 35. Setup Time under 25°C

<table>
<thead>
<tr>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V=1.0v</td>
<td>-30.387</td>
<td>-27.417</td>
<td>-23.606</td>
<td>-38.041</td>
</tr>
<tr>
<td>V=1.1v</td>
<td>-28.724</td>
<td>-26.667</td>
<td>-23.478</td>
<td>-34.967</td>
</tr>
<tr>
<td>V=1.2v</td>
<td>-27.987</td>
<td>-25.809</td>
<td>-23.057</td>
<td>-33.903</td>
</tr>
</tbody>
</table>

Figure 36. Setup Time under 100°C

<table>
<thead>
<tr>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V=1.1v</td>
<td>-29.915</td>
<td>-27.326</td>
<td>-23.823</td>
<td>-40.211</td>
</tr>
<tr>
<td>V=1.2v</td>
<td>-28.257</td>
<td>-26.411</td>
<td>-23.542</td>
<td>-35.135</td>
</tr>
</tbody>
</table>
Figure 34-36 are the setup time of the flip-flop when the temperature is 0°C, 25°C and 100°C respectively. In Figure 34, we can see that the absolute value of the setup time decrease when the power supply of the flip-flop increase. According to the function in 3.3.4, when the power supply increases, the voltage between gate and source of a MOS transistor increase, so the drain current of the transistor will increase. The circuit needs less time to charge or discharge, so the setup of the flip-flop will decrease when the power supply increase.

In Figure 34, we can find that when the temperature is 0°C, the setup time has changed very small if the power supply changed, and it has demonstrated what we have discussed in 3.3.4. It is possible that the circuit is in the velocity saturation in that situation, so whatever the power supply has changed, \( v = v_{sat} = \mu_n E_c \). In other words, the drain current of the transistors in this situation is almost a constant, so whatever the power supply has increased or decreased, the drain current of the transistor will not change. So the time that the circuit needs to charge or discharge will not change. So the setup time of the flip-flop in this situation has almost not changed.

After comparing between Figure 34, Figure 35 and Figure 36, we can find that the setup time of the flip-flop will increase when the temperature increase. Because if the temperature increase, the mobility of the electron will decrease, if the value of \( \mu_n \) decreased, the drain current \( I_D \) will decrease, so the circuit needs more time to charge or discharge the circuit, the setup time will increase.

### 3.3.6 Setup Time of the Flip-Flop in Different Process Corners

Figure 37-41 are the Setup Time of the flip-flop when the circuit work in the Nominal Corner, FF Corner, FS Corner, SF Corner and SS Corner respectively. In each figure, we can see that the setup time will increase when the temperature increase or the when the power supply decrease. These five figures have demonstrated that out analysis of the 3.3.4 and 3.3.5 are right. When the temperature increase, the mobility of the electron will decrease, so the drain current of the transistors will decrease, the circuit needs more time to charge or discharge, so the setup time will decrease. When the power supply increase, the voltage between the gate and source of a transistor will increase, from the function in 3.3.4, we can find that the drain current of the transistor will increase, so the circuit needs less time to charge or discharge.

When we scrutinize the five figures, we can see that when the circuit works in the
Nominal Corner, FS Corner, SF Corner and SS corner, the change of temperature from 0°C to 25°C has not much affect on the circuit if the power supply is 1.2v (high power supply). When the power supply is high, and the range of temperature is about from 0°C to 25°C, the change of temperature has little effect on the mobility of the electron, so the drain current of the transistor will be affected very small, at this time, the change of temperature has very little effect on the setup time.

When the circuit works in the Nominal Corner, FS Corner, SF Corner and SS corner, we can see that the change of power supply from 1.1v to 1.2v has not much affect on the circuit if the temperature is 0°C (low temperature). It is possible that the circuit is in the velocity saturation in that situation, so whatever the power supply has changed, 

\[ v = v_{sat} = \mu_n E_C \]

In other words, the drain current of the transistors in this situation is almost a constant, so whatever the power supply has increased of decreased, the drain current of the transistor will not change. So the time that the circuit needs to charge of discharge will not change. So the setup time of the flip-flop in this situation has almost not changed.

![Figure 37. Setup Time in Nominal Corner](image-url)
Figure.38. Setup Time in FF Corner

Figure.39. Setup Time in FS Corner
Figure 40. Setup Time in SF Corner

Figure 41. Setup Time in SS Corner
### 3.3.7 Hold time of the Flip-Flop in Different Power Supplies

The following figures illustrate the hold time of the flip-flop under different power supplies and temperatures.

#### V=1.0v Hold Time

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Temp °C</th>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0°C</td>
<td></td>
<td>44.458</td>
<td>38.347</td>
<td>50.501</td>
<td>42.241</td>
<td>53.268</td>
</tr>
<tr>
<td>T=25°C</td>
<td></td>
<td>49.067</td>
<td>42.258</td>
<td>57.537</td>
<td>44.96</td>
<td>61.837</td>
</tr>
<tr>
<td>T=100°C</td>
<td></td>
<td>71.693</td>
<td>61.753</td>
<td>93.228</td>
<td>70.23</td>
<td>98.623</td>
</tr>
</tbody>
</table>

**Figure 42. Hold Time under 1.0v Power Supply**

#### V=1.1v Hold Time

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Temp °C</th>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0°C</td>
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<td>42.18</td>
<td>36.045</td>
<td>46.43</td>
<td>40.368</td>
<td>48.73</td>
</tr>
<tr>
<td>T=25°C</td>
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<td>46.737</td>
<td>41.727</td>
<td>55.668</td>
<td>43.015</td>
<td>58.813</td>
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<tr>
<td>T=100°C</td>
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<td>70.872</td>
<td>57.549</td>
<td>84.635</td>
<td>67.42</td>
<td>91.81</td>
</tr>
</tbody>
</table>

**Figure 43. Hold Time under 1.0v Power Supply**
Figure 42-44 are the hold time of the flip-flop when the power supply of the circuit is 1.0v, 1.1v and 1.2v respectively. In Figure 42 we can see that the hold time increase when the temperature increase. Because when the temperature increase, the mobility of the electron will decrease, from the function in 3.3.4, if the value of $\mu_n$ decreased, the drain current $I_D$ will decrease, so the circuit needs more time to charge or discharge the circuit, the hold time will increase.

When we compare between the Figure 42, Figure 43 and Figure 44, we can find that when the circuit works in 0°C (low temperature), the hold time has almost not change when the power supply changes. It is possible that the circuit is in the velocity saturation at that time, so whatever the power supply has changed, $V = v_{sat} = \mu_n E_C$. In other words, the drain current of the transistors in this situation is almost a constant, so whatever the power supply has increased or decreased, the drain current of the transistor will not change. So the time that the circuit needs to charge or discharge will not change. So the hold time of the flip-flop in this situation has nearly not changed.

Figure 44. Hold Time under 1.0v Power Supply
3.3.8 Hold time of the Flip-Flop in Different Temperatures

![Hold Time Graph](image)

Figure 45. Hold Time under 0°C

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0V</td>
<td>44.458</td>
<td>38.347</td>
<td>50.501</td>
<td>42.241</td>
<td>53.268</td>
</tr>
<tr>
<td>1.1V</td>
<td>42.18</td>
<td>36.045</td>
<td>46.43</td>
<td>40.368</td>
<td>48.73</td>
</tr>
<tr>
<td>1.2V</td>
<td>39.965</td>
<td>34.032</td>
<td>43.462</td>
<td>38.268</td>
<td>44.447</td>
</tr>
</tbody>
</table>

![Hold Time Graph](image)

Figure 46. Hold Time under 25°C

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0V</td>
<td>49.067</td>
<td>42.258</td>
<td>57.537</td>
<td>44.96</td>
<td>61.837</td>
</tr>
<tr>
<td>1.1V</td>
<td>46.737</td>
<td>41.727</td>
<td>55.668</td>
<td>43.015</td>
<td>58.813</td>
</tr>
<tr>
<td>1.2V</td>
<td>45.193</td>
<td>41.31</td>
<td>53.291</td>
<td>42.778</td>
<td>55.214</td>
</tr>
</tbody>
</table>
Figure 45-47 are the hold time of the flip-flop when the temperature is 0°C, 25°C and 100°C respectively. In Figure 45 we can see that the hold time decrease when the power supply of the flip-flop increase. According to the function in 3.3.4, when the power supply increases, the voltage between gate and source of a MOS transistor increase, so the drain current of the transistor will increase. The circuit needs less time to charge or discharge, so the hold of the flip-flop will decrease when the power supply increase.

After comparing between Figure 45, Figure 46 and Figure 47, we can find that the hold time of the flip-flop will increase when the temperature increase. Because if the temperature increase, the mobility of the electron will decrease, if the value of $\mu_n$ decreased, from the function in 3.3.4, the drain current $I_d$ will decrease, so the circuit needs more time to charge or discharge the circuit, the hold time will increase.
3.3.9 Hold time of the Flip-Flop in Different Process Corners

Figure 48. Hold Time in Nominal Corner

Figure 49. Hold Time in FF Corner
Figure 50. Hold Time in FS Corner

Figure 51. Hold Time in SF Corner
Figure 48-52 are the Hold Time of the flip-flop when the circuit works in the Nominal Corner, FF Corner, FS Corner, SF Corner and SS Corner respectively. In each figure, we can see that the hold time will increase when the temperature increase or the when the power supply decrease. These five figures have demonstrated that out analysis of the 3.3.7 and 3.3.8 are right. When the temperature increase, the mobility of the electron will decrease, so the drain current of the transistors will decrease, the circuit needs more time to charge or discharge, so the hold time will decrease. When the power supply increase, the voltage between the gate and source of a transistor will increase, from the function in 3.3.4, we can find that the drain current of the transistor will increase, so the circuit needs less time to charge or discharge.

When we scrutinize the five figures, we can see that the change of power supply has very small effect on the hold time. The definition of the hold time is that the time the data input must remain valid after the clock edge. So it is possible that the circuit is in the saturation region of there is velocity saturation effect in the circuit, in other words, even if the power supply has increased, the drain current of the transistors will not change much, so the time that the circuit needs to charge of discharge has not changed. So the change of the power supply has very small effect on the hold time.
Chapter 4

The Application of Dual-Edge Triggered Flip-Flops with high performance and high soft-error tolerance

4.1 Design for Testability

Testing and validation is an important issue in IC design. A correct design does not mean that there is no fault in the manufactured components. In industry, there are many defects has to be taken into account: impurities in the silicon crystal, short circuits between wires or layers, broken interconnections, etc. So it is necessary to validate the circuit after the manufacturing process. Usually, to test a circuit and make sure that there is no fault in the circuit is very expensive in the manufacturing of chips. So how to design a good and cheap testability circuit is an important element in recent years.

When we consider test capabilities in a design, there are two important properties:
- CONTROLLABILITY: An internal node of the circuit can be set to a certain value according to the requirement.
- OBSERVABILITY: A specific circuit node can be observed at the output of the integrated circuit. Ideally, it should be possible to observe every single gate output either directly or indirectly (within some clock cycles).

Design For Testability is a design technique, of which the objective is to improve controllability and observability in the circuit. The two main approaches are:
- BIST (Built In Self Test)
- Scan Design
4.2 Design of The Scan Chain Using Dual-Edge Triggered Flip-Flop With High Soft-Error Tolerance And High Performance

In this section, a high performance scan chain is designed. Because the flip-flop we used will be triggered at the dual edge of the clock, in the process of testing, we can reduce the clock frequency to half that of the single edge-triggered flip-flops while maintaining the same data throughput more power will be saved. In the following section, we need to design a scan cell first, because the scan chain is composed of scan cell, then we need to use the scan chain to test the faults in a combinational circuit.

4.2.1 Scan Cell

Figure 53 is the schematic of the scan cell. There are two multiplexers and two flip-flops in the scan cell. Now we are going to explain the function of each input of the scan cell

- SIN: This is the interface from where we can scan a test vector into the scan cell.
- SOUT: This is used to connect to the next scan cell in the scan chain.

Figure 53. Scan Cell
• OUT: This interface is used to connect to the combinational circuit which we are going to test.

• UPDATE: This interface is used to control the second flip-flop whether transfer the output of first flip-flop into the combinational circuit.

• SHIFT/LOAD: This interface is used to control the multiplexer which signal should be scanned into the scan cell. If it is 1, it is in the load mode, the input data will be transferred into the scan cell. If it is 0, it is in the shift mode, the test vector will be scanned into the scan cell.

• MODE: This interface is used to control the multiplexer. If it is 0, then the circuit is in the test mode. If it is 1, then the circuit will work as usual.

4.2.2 Scan Chain

In this section, we will design a scan chain for testing a combinational circuit. Not as the scan chain in [43], the scan chain in this thesis has the function of Shift, Load and Update. In this scan chain, each little box is the scan cell we have introduced in 3.2.1. The OUT of the each scan cell connects to the combinational circuit, and the SOUT of the each scan cell connect to the input D of the next scan cell. All SHIFT/LOAD of the scan cells are all controlled by one same signal. All UPDATE of the scan cells are all controlled by one signal. And all CLOCK of the scan cells are all controlled by one signal. If we want to scan a combinational circuit and want to know whether there is a fault in the circuit, we need to do in the next steps:

• Shift: Scan the test vectors into the scan cell.

• Update: Update the data in the scan cell into the combinational circuit.

• Load: Load the output of combinational circuit into the scan cell.

• Shift: We can look at the output of the combinational circuit at OUT

To avoid the occurrence of the clock skew, we resize the pulse generator of the flip-flop, to make sure that one pulse generator can drive five latching stages. So the size of the pulse generator increased and the pulse width has increased, so the clock-to-q delay, setup time and hold time of the flip-flop in the scan chain has changed, we will analyze these parameters in the following section.
Figure 54. Scan Chain
In Figure 55, we can clearly see that the pulse generator is on the top of the figure, under the pulse generator, there are five latching stages, which are drove by the pulse generator.

Figure 55. Layout of the flip-flop in the scan chain

Figure.56. The combinational logic in the scan chain
Figure 56 is the combinational circuit which we want to test using the scan chain. In manufacturing process, all the points in the combinational circuits possibly has the faults, such as the stuck-at-1 and stuck-at-0 faults. Now we will use the HSPICE to simulate whether the scan chain can work correctly and can test the faults in the combinational circuit. The sequence of the test vector is $A_1 A_2 B_1 B_2 C_{in}$. Figure 57-60 is the result of simulation. In each figure, the lower five signal from up to low are the Sout1, Sout2, Sout3, Sout4 and Sout5 respectively. Figure 57 is the case that when the test vector is 10101, if there is no fault in the adder, the output is 101. Figure 58 is the case that when the test vector is 10101, if there is a stuck-at-1 fault at the point 4 in Figure 56, the output of the scan chain is 101. Figure 59 is the case that when the test vector is 11100, if there is no fault in the adder, the output of scan chain is 101. Figure 60 is the case that when the test vector is 11100, if there is a stuck-at-0 fault at point 4 in Figure 56, the output of the scan chain is 100. After verifying the results of the simulation, we can demonstrate that this scan chain can work correctly. If there is a fault in the combinational circuit, it can detect it out and we can see the output of the scan chain at the point OUT.

Figure 57. No fault in the combinational logic when test vector is 10101
Figure 58. Stuck-at-1 fault in the combinational logic when test vector is 10101

Figure 59. No fault in the combinational logic when test vector is 11100
4.3 PVT VARIATIONS OF THE DUAL-EDGE TRIGGERED FLIP-FLOP IN SCAN CHAIN

In the scan chain, we have resized the pulse generator of the flip-flop and let the pulse generator drive five latching stages. Because the size of the pulse generator has changed, the pulse width much has changed. So the Clock-to-Q delay, Setup Time and Hold time of flip-flop in the scan chain much have changed. In this section, we will repeat all the job we have done in 3.3, and analyze the effect of process, voltage and temperature on the flip-flop in the scan chain.
4.3.1 Clock-to-Q Delay of The Flip-Flop in Different Power Supplies

Figure 6.1: Clock-to-Q delay of the FF in scan chain under 1.0V power supply

<table>
<thead>
<tr>
<th>Temperature °C</th>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0</td>
<td>22.763</td>
<td>19.329</td>
<td>24.334</td>
<td>22.725</td>
<td>29.54</td>
</tr>
<tr>
<td>T=25</td>
<td>27.354</td>
<td>21.448</td>
<td>27.981</td>
<td>26.21</td>
<td>34.835</td>
</tr>
<tr>
<td>T=100</td>
<td>40.04</td>
<td>29.801</td>
<td>40.926</td>
<td>38.537</td>
<td>54.761</td>
</tr>
</tbody>
</table>

Figure 6.2: Clock-to-Q delay of the FF in scan chain under 1.1V power supply

<table>
<thead>
<tr>
<th>Temperature °C</th>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=100</td>
<td>35.377</td>
<td>26.626</td>
<td>36.317</td>
<td>34.187</td>
<td>46.832</td>
</tr>
</tbody>
</table>

V=1.0V Clock-to-Q delay

V=1.1V Clock-to-Q delay
Figure 61 is the Clock-to-Q delay of the flip-flop in the scan chain under 1.0v power supply, the standard power supply we gave of the flip-flop is 1.1v. From Figure 61 we can see that when the flip-flop is working in all kinds of corners, the Clock-to-Q delay will increase when the temperature increase. The mobility of the electron will decrease when the temperature increase. So the drain current of the transistor will decrease. Figure 62 is the Clock-to-Q delay of the flip-flop in scan chain under 11v power supply (standard power supply). The same as Figure 61, when the flip-flop is working in all kinds of corners, the Clock-to-Q delay will increase when the temperature increase. Moreover, we can see that in each corner, comparing to Figure 61, under the same temperature, the Clock-to-Q delay has decreased. Figure 63 is the Clock-to-Q delay of the flip-flop under 1.2v power supply. The same as Figure 62, when the flip-flop is working in all kinds of corners, the Clock-to-Q delay will increase when the temperature increase. Comparing to Figure 61, under the same corner and same temperature, the clock-to-q delay has decreased. So we can summarize that the clock-to-q delay will decrease when the power supply increase. From the formula in 3.3.4 we can know that when the power supply increase, the voltage between gate and source $V_{GS}$ will increase, the drain current of the transistor will increase, so the circuit will charge quicker. We can also see from the three figures that when the circuit works in the FF corner, the Clock-to-Q delay is the smallest, and when the circuit works in the SS corner, the Clock-to-Q delay is the biggest.

![Figure 63. Clock-to-Q delay of the FF in scan chain under 1.2v power supply](image-url)
4.3.2 Clock-to-Q Delay of The Flip-Flop in Different Temperatures

Figure 64. Clock-to-Q delay of the FF in scan chain under 0°C

Figure 65. Clock-to-Q delay of the FF in scan chain under 25°C
Figure 64 is the Clock-to-Q delay of the flip-flop in scan chain when the circuit works in 0°C. In each certain corner, we can see that the clock-to-q delay decrease when the power supply increase. This demonstrate our analysis in 4.3.1, because when the power supply increase, the voltage between gate and source of the transistor will increase, so the drain current of the transistor will increase, the circuit will charge quicker than the circuit which is provide by lower power supply. Figure 65 is the Clock-to-Q delay of the flip-flop when the circuit works in 25°C and Figure 66 is the Clock-to-Q delay of the flip-flop when the circuit works in 100°C. Comparing these three figures we can see that for the same process corner and same power supply, when the temperature increase, the clock-to-q delay will increase, as we said before, when the temperature increase, the mobility of the electron will decrease, the drain current of the transistor will decrease, so the circuit needs more time to be charged or discharge. The clock-to-q delay will increase. From Figure 64, Figure 65, and Figure 66, we can find that the circuit work fastest in the FF corner and work slowest in the SS corner. When circuit works in the nominal corner, FS corner and SF corner, the Clock-to-Q delay is almost the same.
4.3.3 Clock-to-Q Delay of The Flip-Flop in Different Process Corners

![Clock-to-Q delay (Nominal Corner)](image1)

Figure.67. Clock-to-Q delay of the FF in scan chain in Nominal Corner

![Clock-to-Q delay (FF corner)](image2)

Figure.68. Clock-to-Q delay of the FF in scan chain in FF Corner
Figure. 69. Clock-to-Q delay of the FF in scan chain in FS Corner

Figure. 70. Clock-to-Q delay of the FF in scan chain in SF Corner
Figure 67-71 are the Clock-to-Q delays when the flip-flop in the scan chain works in the Nominal Corner, FF Corner, FS Corner, SF Corner and SS Corner respectively. In each figure, we can see that the Clock-to-Q delay will increase when the temperature increase or when the power supply decrease. We have discussed the reason of this result before. These five figures have demonstrated that out analysis of the 4.3.1 and 4.3.2 are right. When the temperature increase, the mobility of the electron will decrease, so the drain current of the transistors will decrease, the circuit needs more time to charge or discharge, so the Clock-to-Q delay will decrease. When the power supply increase, the voltage between the gate and source of a transistor will increase, from the formula in 4.3.4, we can find that the drain current of the transistor will increase, so the circuit needs less time to charge or discharge. Moreover, we can see that these five figures are more sensitive to the temperature than the power supply. It possible that the circuit is already working in the saturation region at that time, so the change of power supply do not have much effect on the drain current of the transistor, so it does not have much effect on the clock-to-q delay. After comparing the five figures, we can find that when the circuit work in the SS corner, its clock-to-q delay is the biggest, the circuit is also most sensitive to the changing of temperature and power supply. When the circuit work in the FF corner, its clock-to-q delay is the smallest, the circuit is also most insensitive to the changing of temperature and power supply.
4.3.4 Setup Time of the Flip-Flop in Different Power Supplies

**Figure 72. Setup Time of the FF in scan chain under 1.0v Power Supply**

<table>
<thead>
<tr>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0 °C</td>
<td>-52.397</td>
<td>-48.469</td>
<td>-50.13</td>
<td>-64.254</td>
</tr>
<tr>
<td>T=100 °C</td>
<td>-66.336</td>
<td>-61.299</td>
<td>-51.623</td>
<td>-86.118</td>
</tr>
</tbody>
</table>

**Figure 73. Setup Time of the FF in scan chain under 1.1v Power Supply**

<table>
<thead>
<tr>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0 °C</td>
<td>-51.034</td>
<td>-47.492</td>
<td>-47.598</td>
<td>-62.555</td>
</tr>
<tr>
<td>T=25 °C</td>
<td>-54.293</td>
<td>-52.32</td>
<td>-50.327</td>
<td>-64.55</td>
</tr>
<tr>
<td>T=100 °C</td>
<td>-64.845</td>
<td>-57.862</td>
<td>-51.313</td>
<td>-77.88</td>
</tr>
</tbody>
</table>
Figure 72-74 are the setup time of the flip-flop in the scan chain when the power supply of the circuit is 1.0v, 1.1v and 1.2v respectively. In Figure 72 we can see that the absolute value of the setup time increase when the temperature increase. From the formula in 3.3.4, when the temperature increase the mobility of the electron will decrease, if the value of $\mu$ decreased, the drain current $I_D$ will decrease, so the circuit needs more time to charge or discharge the circuit, the setup time will increase.

When we scrutinize the Figures 72-74, we can find that in the Nominal Corner and FF Corner, when the temperature is 0°C, the setup time has changed very small if the power supply changed, this is the same reason we have discussed in 3.3.5. It is possible that the circuit is in the velocity saturation in that situation, so whatever the power supply has changed, $v = v_{sat} = \mu_c E_C$. In other words, the drain current of the transistors in this situation is almost a constant, so whatever the power supply has increased of decreased, the drain current of the transistor will not change. So the time that the circuit needs to charge or discharge will not change. So the setup time of the flip-flop in this situation has almost not changed.
4.3.5 Setup Time of the Flip-Flop in Different Temperatures

![Figure 75. Setup Time of the FF in scan chain under 0°C](image)

![Figure 76. Setup Time of the FF in scan chain under 25°C](image)
Figure 75-77 are the setup time of the flip-flop in the scan chain when the temperature is 0°C, 25°C and 100°C respectively. In Figure 75 we can see that the absolute value of the setup time decrease when the power supply of the flip-flop increase. According to the formula in 3.3.4, when the power supply increases, the voltage between gate and source of a MOS transistor increase, so the drain current of the transistor will increase. The circuit needs less time to charge or discharge, so the setup of the flip-flop will decrease when the power supply increase.

In Figure 75, we can find that in the Nominal Corner and FF Corner, the setup time has changed very small if the power supply changed, and it has demonstrated what we have discussed in 4.3.4. It is possible that the circuit is in the velocity saturation in that situation, so whatever the power supply has changed, \( v = v_{sat} = \mu_n E_c \), the drain current of the transistor will not change. So the time that the circuit needs to charge or discharge will not change. So the setup time of the flip-flop in this situation has almost not changed.

After comparing between Figure 75, 76 and 77, we can find that the setup time of the flip-flop will increase when the temperature increase. Because when the temperature increase, the mobility of the electron will decrease, if the value of \( \mu_n \) decreased, the drain current \( I_D \) will decrease, so the circuit needs more time to charge or discharge the circuit, the setup time will increase.
4.3.6 Setup Time of the Flip-Flop in Different Process Corners

Figure 78. Setup Time of the FF in scan chain in Nominal Corner

Figure 79. Setup Time of the FF in scan chain in FF Corner
Figure 80. Setup Time of the FF in scan chain in FS Corner

Figure 81. Setup Time of the FF in scan chain in SF Corner
Figure 78-82 are the Setup Time of the flip-flop in the scan chain when the flip-flop works in the Nominal Corner, FF Corner, FS Corner, SF Corner and SS Corner respectively. In each figure, we can see that the setup time will increase when the temperature increase or the when the power supply decrease. These five figures have demonstrated that our analysis of the 4.3.4 and 4.3.5 are right. When the temperature increase, the mobility of the electron will decrease, so the drain current of the transistors will decrease, the circuit needs more time to charge or discharge, so the setup time will decrease. When the power supply increase, the voltage between the gate and source of a transistor will increase, from the formula in 3.3.4, we can find that the drain current of the transistor will increase, so the circuit needs less time to charge or discharge.

When we scrutinize the five figures, we can see that the change of temperature from 25°C to 100°C has a big effect on the circuit. It is possible that when the range of temperature is about from 25°C to 100°C, the change of temperature has a big effect on the mobility of electron, so the temperature will have a big effect on the drain current of the transistor.

From the five figures, we can see that the change of power supply has not much effect on the circuit. It is possible that the circuit is in the velocity saturation in that situation, so whatever the power supply has changed, \( v = v_{sat} = \mu_s E_C \). In other words, the drain current of the transistors in this situation is almost a constant, so whatever the
power supply has increased or decreased, the drain current of the transistor will not change. So the time that the circuit needs to charge or discharge will not change. So the setup time of the flip-flop in this situation has almost not changed.

4.3.7 Hold time of the Flip-Flop in Different Power Supplies

Figure 83-85 are the hold time of the flip-flop in the scan chain when the power supply of the circuit is 1.0v, 1.1v and 1.2v respectively. In Figure 83 we can see that the hold time increase when the temperature increase. Because when the temperature increase, the mobility of the electron will decrease, from the formula in 3.3.4, if the value of $\mu_n$ decreased, the drain current $I_D$ will decrease, so the circuit needs more time to charge or discharge the circuit, the hold time will increase.

When we compare between the Figure 83, Figure 84 and Figure 85, we can find that when the circuit works in 0°C, the hold time has almost not change when the power supply changes. It is possible that the circuit is in the velocity saturation at that time, so whatever the power supply has changed, $v = v_{sat} = \mu_n E_C$. In other words, the drain current of the transistors in this situation is almost a constant, so whatever the power supply increase or decrease, the drain current of the transistor will not change. So the time that the circuit needs to charge or discharge will not change. So the hold time of the flip-flop in this situation has almost not changed.

![Figure 83. Hold Time of the FF in scan chain under 1.0v Power Supply](image)

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Nominal</th>
<th>FF</th>
<th>FS</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>T=0 °C</td>
<td>77.449</td>
<td>70.776</td>
<td>75.644</td>
<td>83.727</td>
<td>91.479</td>
</tr>
<tr>
<td>T=25 °C</td>
<td>82.972</td>
<td>74.785</td>
<td>80.11</td>
<td>89.107</td>
<td>94.873</td>
</tr>
<tr>
<td>T=100 °C</td>
<td>102.92</td>
<td>91.23</td>
<td>97.849</td>
<td>116.43</td>
<td>128.47</td>
</tr>
</tbody>
</table>
Figure 84. Hold Time of the FF in scan chain under 1.1v Power Supply

Figure 85. Hold Time of the FF in scan chain under 1.2v Power Supply
4.3.8 Hold time of the Flip-Flop in Different Temperatures

Figure 86. Hold Time of the FF in scan chain under 0°C

Figure 87. Hold Time of the FF in scan chain under 25°C
Figures 86-88 are the hold time of the flip-flop in the scan chain when the temperature is 0°C, 25°C and 100°C respectively. In Figure 86 we can see that the hold time decreases when the power supply of the flip-flop increases. According to the formula in 3.3.4, when the power supply increases, the voltage between gate and source of a MOS transistor increases, so the drain current of the transistor will increase. The circuit needs less time to charge or discharge, so the hold of the flip-flop will decrease when the power supply increases.

In the three figures, we can find that the change of the power supply has not much effect on the change of the hold time. It is possible that the transistors are working in the saturation region or there is a velocity saturation effect in the circuit. So even if the power supply has increased, it has not much effect on the drain current of the transistors. If the drain current does not change,

After comparing between Figure 86, Figure 87 and Figure 88, we can find that the hold time of the flip-flop will increase when the temperature increases. Because if the temperature increases, the mobility of the electron will decrease, if the value of $\mu_n$ decreased, from the formula in 3.3.4, the drain current $I_D$ will decrease, so the circuit needs more time to charge or discharge the circuit, the hold time will increase.
4.3.9 Hold time of the Flip-Flop in Different Process Corners

Figure 89. Hold Time of the FF in scan chain in Nominal Corner

Figure 90. Hold Time of the FF in scan chain in FF Corner
Figure 91. Hold Time of the FF in scan chain in FS Corner

Figure 92. Hold Time of the FF in scan chain in SF Corner
Figures 89-93 are the Hold Time of the flip-flop in the scan chain when the circuit works in the Nominal Corner, FF Corner, FS Corner, SF Corner and SS Corner respectively. In each figure, we can see that the hold time will increase when the temperature increase or when the power supply decrease. These five figures have demonstrated that our analysis of 4.3.7 and 4.3.8 are right. When the temperature increase, the mobility of the electron will decrease, so the drain current of the transistors will decrease, the circuit needs more time to charge or discharge, so the hold time will decrease. When the power supply increase, the voltage between the gate and source of a transistor will increase, from the formula in 3.3.4, we can find that the drain current of the transistor will increase, so the circuit needs less time to charge or discharge.

When we scrutinize the five figures, we can see that the change of power supply has very small effect on the hold time. The definition of the hold time is that the time the data input must remain valid after the clock edge. So it is possible that the circuit is in the saturation region of there is velocity saturation effect in the circuit, in other words, even if the power supply has increased, the drain current of the transistors will not change much, so the time that the circuit needs to charge or discharge has not changed. So the change of the power supply has very small effect on the hold time.

In the figures, we can find that when the flip-flop works in the SS corner, it is very sensitive to the change of temperature.
Chapter 5

Conclusion

In the thesis, a dual-edge triggered pulsed flip-flop with high performance and high soft-error tolerance is designed. Dual-edge triggered flip flop offers the same data throughput of single edge-trigger flip-flops at half of the clock frequency, this thereafter translates to better performance in terms of both power dissipation and speed. The flip-flop in this thesis has two stages, pulse generator and latching stage. The pulse generator can generates very narrow pulse at both the rising edge of the clock and falling edge of the clock. Therefore, we can reduce both the setup time and hold time of the flip-flop. In the latching stage of the flip-flop, the input $D$ and $\overline{D}$ can help the output $Q$ and $\overline{Q}$ charge or discharge directly. In this way, we can reduce the Clock-to-Q delay, moreover, in the latching stage, we use two PMOS transistors P7 and P9 in Figure 16 to control the two inverters, when the flip-flop is in the transparent mode, the two inverters under P7 and P9 will stop working, in this way, we can save more power.

In this thesis, a soft-error masking structure is added to the latching stage. We can see this structure in Figure 16. If the voltage of the output is high, transistor N7 will turn on, the most sensitive point in the circuit will connect to the ground. If the voltage of the output is low, transistor P11 will turn on, the most sensitive point in the circuit will connected to the Vdd. So the flip-flop can have a higher tolerance of the soft-error.

Comparing to the other flip-flops in the latest publications, the Clock-to-Q delay, setup time and hold time of this flip-flop have all improved. Moreover, this flip-flop can have a much higher soft-error tolerance than the flip-flops in other publications.

In chapter 4 of this thesis, a scan chain which is used to test faults in combinational logic is designed using the dual-edge triggered flip-flop in this thesis. We used a 2-bit full adder to verify whether the scan chain can work correctly and can test the faults out. The result of the simulation demonstrates that this dual-edge triggered flip-flop can work correctly and can be applied in practice.
Reference


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