LOW-POWER HIGH-SPEED LOW-OFFSET FULLY DYNAMIC CMOS LATCHED COMPARATOR

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ABSTRACT

A new fully dynamic latched comparator which shows lower offset voltage and higher load drivability than the conventional dynamic latched comparators has been designed. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented. As a result, the circuit shows up to 19% less offset voltage and 62% less sensitivity of the delay versus the input voltage difference (delay/log(ΔV_{in})), which is about 17ps/decade, than the conventional double-tail latched comparators at approximately the same area and power consumption. Along with the proposed design, this thesis provides a comprehensive review about a variety of traditional dynamic latched comparator designs - in terms of performance, power, area and input-referred offset voltage.
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Chapter 1

Introduction

1.1 Motivation

Due to fast-speed, low-power consumption, high-input impedance and full-swing output, CMOS dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time. However, an input-referred latch offset voltage (hence offset voltage), resulting from the device mismatches such as threshold voltage $V_{th}$, current factor $\beta$ ($=\mu C_{ox} W/L$) and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators [5], [6]. Because of this reason, the input-referred latch offset voltage is one of the most important design parameters of the latched comparator. If large devices are used for the latching stage, a less mismatch can be achieved at the cost both of the increased delay (due to slowing the regeneration time) and the increased power dissipation.

More practically, the input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output-latch stage as shown in Figure 1. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise [11]. However, the pre-amplifier based comparators suffer not only from large static power consumption for a large bandwidth but
also from the reduced intrinsic gain with a reduction of the drain-to-source resistance $r_{ds}$ due to the continuous technology scaling [7].

In the literature, various kinds of CMOS comparators can be found. The types of the comparators can be classified largely into three: *Open-loop Comparators* (op-amps without compensation), *Pre-amplifier Based Latched Comparators* (open-loop comparator combined with dynamic regenerative latch), and *Fully Dynamic Latched Comparator*. In this paper, various kinds of fully dynamic latched comparators will be fully analyzed in terms of their advantages and disadvantages along with operating principles and experimental results of the speed, power consumption, and offset voltage at a limited area. Then, a new dynamic latched comparator which shows lower offset voltage and higher load drivability than the conventional dynamic latched comparators is proposed.

**Figure 1** Typical block diagram of a high-speed voltage comparator
1.2 Thesis Organization

This thesis provides a new dynamic latched comparator which shows lower offset voltage and higher load drivability than the conventional dynamic latched comparators. The remaining parts of the thesis are organized as follows. Chapter 2 reviews the important features (design considerations) of voltage comparators, introduces and classifies popular structures of voltage comparators. Chapter 3 explains the operation principles of each structure and compares them in terms of speed, power consumption, offset voltage and area. Chapter 4 presents the proposed fully dynamic latched comparator and conclusion and future works are drawn in Chapter 5. The used 90 nm PTM (Predictive Technology Model) files and HSPICE netlist files for each comparator circuit are attached in the Appendix.
Chapter 2

Literature Review

In this chapter, important features and design considerations of a voltage comparator will be reviewed. In addition, a different kind of comparator architectures will be reviewed after classifying them into three: Open-loop Comparator, Pre-amplifier Based Latched comparator, and Fully Dynamic Latched Comparator. Especially, fully dynamic latched comparators will be analyzed in detail.

2.1 Design Considerations for Voltage Comparator

The basic function of a comparator is to compare an analog signal with another analog signal or reference and output a binary signal based on comparison. Since it is easier to distribute voltages to a large number of comparators than to distribute currents, most converters employ voltage comparison [9]. A voltage comparator can be simply regarded as a 1-bit ADC.

The circuit symbol and ideal and practical voltage transfer functions of a comparator are shown in Figure 2. As shown in Figure 2 (b), the ideal comparator outputs $V_{OH}$ (logic high “1” = $V_{DD}$) if $V_{in+} - V_{in-} > 0$ and else it outputs $V_{OL}$ (logic low “0” = 0V (or $-V_{SS}$)) since it has infinite gain, zero offset voltage and zero RMS noise. However, for a practical comparator shown in Figure 2 (c), it outputs $V_{OH}$ only if $V_{in+} - V_{in-} > V_{IH} + V_{OS} (+ |V_{noise}|)$ and it outputs $V_{OL}$ only if $V_{in+} - V_{in-} < V_{IL} (- |V_{noise}|)$ because it has a finite gain ($A_{V} = \frac{V_{OH}-V_{OL}}{V_{IH}-V_{IL}}$), non-zero offset voltage and RMS noise (for latched comparators, $V_{IL}$ and $V_{IH}$ are limited by its sampling (or Clk) frequency due to meta-stability.)
Therefore, design considerations for voltage comparators are can be summarized as high-speed (maximum clock rate $f_s$, which is related to small signal bandwidth, slew rate, and settling time), accuracy (high-resolution, which is related to gain, offset voltage [27], [29], [34] RMS and kickback noise [11], [32], [33], overdrive recovery, and linearity of input capacitance), wide input common–mode range, CMR (common-mode rejection), low-power consumption, small-area and so on [35]. In the next section, architectures of voltage comparators will be classified in to into three: Open-loop Comparators (op-amps without compensation), Pre-amplifier Based Latched Comparators (open-loop comparator combined with dynamic regenerative latch), and Fully Dynamic Latched Comparator and will be reviewed in terms of their advantages and disadvantages.

**Figure 2** Comparator (a) Circuit symbol, (b) Ideal voltage transfer curve, and (c) Practical voltage transfer curve with finite gain, offset voltage and RMS noise [8].
2.2 Comparator Architectures

2.2.1 Open-Loop Comparators [8], [30], [31]

Open-loop, continuous time comparators, shown in Figure 3 [8], are an operational amplifier without frequency compensation to obtain the largest possible bandwidth, hence improving its time response. Since the precise gain and linearity are of no interest in comparator design, no-compensation does not pose a problem. However, due to its limited gain-bandwidth product, open-loop comparators are too slow for many applications. One the other hand, a cascade of open-loop amplifiers usually has a significantly larger gain-bandwidth product than a single-stage amplifier with the same gain. However, since it costs more area and power consumption, cascading does not give practical advantages for many applications.

**Figure 3 (a)** Two-stage open-loop comparator **(b)** Push-pull output open-loop comparator (lower gain but able to sink/source large amount of current in the output capacitance)
2.2.2 Pre-amplifier Based Latched Comparators

![Diagram of pre-amplifier based latched comparators](image)

**Figure 4** (a) A static latched comparator (b) A class-AB latched comparator

**Figure 4** shows typical types of pre-amplifier based latched comparators [11]. The main advantages of the pre-amplifier based latched comparators are their fast speed and low input referred latch offset voltage. Typically, pre-amplifier, which consists of one or two stages of an open-loop comparator, has a gain of 4 - 10 V/V and it can reduce the input-referred latch offset voltage by its gain. For example, if a pre-amplifier has gain of 10 V/V and a latch stage has an offset voltage of 50mV, then the input-referred latch offset voltage will be 5 mV. In addition, by using pre-amplification stage, kickback noise [11] can be considerably reduced (by isolation between the drains of the differential pair transistors and the regeneration nodes) and meta-stability problem also can be relaxed.

Latched comparators commonly employ one or two clock signals (Clk and Clkb) to determine the modes of operation: *Track Mode (Reset)*: output is reset and input is tracked, *Latch Mode (Evaluation)*: output is toggled by using a positive feedback. For the operation of the circuit shown in **Figure 4 (a)** [12-17], during reset phase (Clkb=0V), both complementary output $V_{out+}$ and $V_{out-}$ are reset to 0V by reset (switch) transistor M10 and M11. During
evaluation phase \((\text{ClkB}=V_{DD})\), as the reset transistors are off, the comparison will be performed by a positive feedback from transistor M7 and M9. While this comparator present low kickback noise, relatively large static power consumption and slow regeneration due to its limited current operation make it less attractive \cite{11}. Similarly, the operation for the circuit shown in Figure 4 (b) \cite{18-22}, during reset phase \((\text{Clk}=0V)\), PMOS reset transistor M7 will be shorted and make both outputs equal: \(V_{out+} = V_{out-}\) while NMOS transistor M8 is off. During evaluation phase \((\text{Clk}=V_{DD})\), as the reset transistor M7 is off and the tail transistor of the latch M8 is on, the comparison will be made by a positive feedback formed from back-to-back cross coupled inverter pairs (M4/M6 and M5/M7). While this comparator shows faster speed and consumes less power, it generates more kickback noise and during reset phase both outputs \((V_{out+}, V_{out-})\) are not reset exactly to either \(V_{DD}\) or \(0V\) \cite{11}.

It can be concluded that pre-amplifier based latched comparators, which is a combination of a pre-amplifier and a latch, offer fast speed and low offset while they still consume static power.
2.2.3 Fully Dynamic Latched Comparators

A. Resistor Divider Comparator (or Lewis-Gray Comparator)

The comparator shown in Figure 5 (a) was introduced in [23]. Since the input transistor M1A/B and M2A/B operate in the triode region and act like voltage controlled resistors, this comparator is called “Resistive Divider Comparator.” The advantage of this comparator is its low power consumption (No DC power consumption) and adjustable threshold voltage (decision level) which is defined as

\[ V_{\text{in}}(\text{threshold}) = \left( \frac{W_B}{W_A} \right) V_{\text{ref}} \]  \hspace{1cm} (1)

where \( W_A = W_{1A} = W_{2A} \) \( W_B = W_{1B} = W_{2B} \)

\[ V_{\text{in}} = V_{\text{in}+} - V_{\text{in}-} \quad V_{\text{ref}} = V_{\text{ref}+} - V_{\text{ref}-} \]
For the analysis, the simpler form of the comparator shown in Figure 5 (b) will be used. During reset phase (Clk=0V), PMOS reset transistor M9 and M10 charge Out nodes up to $V_{DD}$ (this makes NMOS transistor M3 and M4 on and the node voltage at $V_{D3,4}$ discharge to ground) and input transistor M1 and M2 discharge $Di$ nodes to ground while NMOS transistor M5 and M6 are off. During evaluation phase (Clk=$V_{DD}$), as both switch transistor M5 and M6 are on, each node voltage at $Di+$ and $Di-$ instantly rises up to the certain values, which are defined as

\[
V_{Di+} = \frac{r_{ds1\,on}}{r_{ds1\,on} + r_{ds3,4\,on} + r_{ds5,6\,on}} \times V_{out-} \approx V_{DD} \quad (2)
\]

\[
V_{Di-} = \frac{r_{ds2\,on}}{r_{ds2\,on} + r_{ds3,4\,on} + r_{ds5,6\,on}} \times V_{out+} \approx V_{DD} \quad (3)
\]

Then, each Out node voltage starts to discharge from $V_{DD}$ to ground inversely proportional to the applied input voltage such a way; $V_{in+} \rightarrow V_{Di-} \rightarrow V_{GS3} \rightarrow I_{D3} \rightarrow V_{out-} \rightarrow V_{GS4} \rightarrow V_{out+} \rightarrow (\rightarrow V_{GS3} \rightarrow \ldots)$. With positive feedback operation from the back-to-back cross-coupled inverter pairs (M7/M3 and M8/M4), one Out node will discharge to ground and the other Out node will charge up to $V_{DD}$ again and this comparator will finish its comparison. Since the input transistor M1 and M2 are operated in the linear region during evaluation phase, the transconductance for those transistors are can be approximately written as

\[
g_{m1,2} = \mu_n C_{ox} \left( \frac{W_{1,2}}{L} \right) V_{ds1,2} \quad (4)
\]

Also, because transistor M3 and M4 are operated in the saturation region during evaluation phase, the transconductance for those transistors are can be written as
\[ g_{m3,4} = \mu_n C_{ox} \left( \frac{W_{3,4}}{L} \right) (V_{gs3,4} - V_{tn}) \] (5)

The transconductance of transistor M3 and M4 is much larger than that of the input transistor pair; hence the differential voltage gain built between \( Di \) nodes from the input transistor pair is not big enough to overcome an offset voltage caused from such a small mismatch between transistor M3 and M4 pair. As a result, those transistors are the most critical mismatch pair in this comparator and needed to be sized big enough to minimize the offset voltage at the cost of the increased power consumption. Besides, the mismatch between transistor M5 and M6 pair (which is switches and operated in the linear region) also causes the considerable input-referred offset voltage. Furthermore, as the common mode voltage \( V_{com} \) of the input transistor pair increases, the relative difference between the voltage controlled resistors \( (r_{ds1,2}) \) becomes smaller at the same amount of the input voltage difference \( \Delta V_{in} \) and this in turn increases the offset voltage.

It can be concluded that despite its advantages such as zero-static power consumption and adjustable threshold voltage, since Lewis-Gray comparator shows a high offset voltage and its high offset voltage dependency on a different common mode voltage \( V_{com} \), it is only suitable for low resolution comparison.
B. Differential Pair Comparator/Latch-type Voltage SA

Figure 6 (a) Differential pair comparator [24, 25] (b) Latch-type voltage SA (sense amplifier) [1], [2] (will be referred as Comparator 2)

The comparator shown in Figure 6 (a) was first proposed in [24] (without extra switching transistor M10 and M11 shown in grey-colored.) Similar to Resistive Divider Comparator, this comparator also has an adjustable threshold voltage and it can be defined as

$$V_{in}(threshold) = \alpha \cdot V_{ref}$$  \hspace{1cm} (6)

$$\text{where } 2d\alpha^2I_{D1A} \left( \frac{W_A}{L} \right) - \mu_n C_{ox} \alpha^2 V_{ref}^2 \left( \frac{W_A}{L} \right)^2 = 2I_{D0} \left( \frac{W_B}{L} \right) - \mu_n C_{ox} V_{ref}^2 \left( \frac{W_B}{L} \right)^2$$

$$V_{in} = V_{in+} - V_{in-} \quad V_{ref} = V_{ref+} - V_{ref-} \quad I_{1A} = d \cdot I_{1B}$$

For the analysis, the simpler form of the comparator shown in Figure 6 (b) will be used and extra switching transistor M10 and M11 are added to improve its characteristics; since those additional PMOS switch transistors increase the time the input transistor pair M2 and M3 being operated in the saturation region during evaluation phase (Clk=V_{DD}), hence the amplification from the differential input pair increases.
The operation of the comparator can be simply described as follows. During reset phase ($Clk=0V$), Out nodes of the cross-coupled inverters (M6-M9) are reset to $V_{DD}$ through the reset transistors M4 and M5. During evaluation phase ($Clk=V_{DD}$), the tail transistor M1 is turned on at the rising $Clk$ edge. The input transistor pair (M2 and M3) starts to discharge each $Di$ node voltage with a different time rate proportional to the each applied input voltage from $V_{DD}$ to $0V$. Once either of $Di$ node voltages drops around $V_{DD}-V_{in}$, then the NMOS transistors of the cross-coupled inverters M6 and M7 turn on and this initiates the positive feedback. Once either of Out node voltage reaches around $V_{DD}-|V_{tp}|$, the PMOS transistors of the inverters M2 and M4 also turn on; further enhancing the positive feedback and enabling the regeneration of a small differential voltage $\Delta V_{in}$ to a full swing differential output.

Comparing with Lewis-Gray comparator, this comparator shows faster operation and less overall offset voltage. However, still its structure which consists of a stack of 4 transistors requires large voltage headroom; it is problematic in low-voltage deep-submicron CMOS technologies. Furthermore, in order to increase the drive currents of the latch, it is inevitable to size up the transistor M1 since this comparator has only one tail transistor M1. If the size of transistor M1 is increased, the drain currents of both input transistors M2 and M3 will increase during evaluation phase ($Clk=V_{DD}$). This, in turn, means the reduction of the time duration for transistor M2 and M3 being operated in saturation region because $Di$ nodes discharge from $V_{DD}$ to ground in a very short period. Consequently, lower amplification of the input voltage difference will be made and such a small $V_{th}$ variation from mismatch between transistor M6 and M7 can yield high input-referred offset. In addition, since it shows the strong dependency on speed and offset voltage with a different common-mode input voltage $V_{com}$ [2], it is less attractive in applications with wide common-mode ranges such as ADCs [3].
C. Double-Tail Dynamic Latched Comparators

To mitigate the drawbacks (strong dependency on speed and offset with a different common-mode input voltage $V_{\text{com}}$ and problem in low power supply voltage operation due to its structure: a stack of four transistors) from the comparator shown in Figure 6 (b), a comparator with separated input-gain stage and output-latch stage, shown in Figure 7 (a), was first introduced in [3]. This separation made this comparator have a lower and more stable offset voltage over wide common-mode voltage ($V_{\text{com}}$) ranges and operate at a lower supply voltage ($V_{\text{DD}}$) as well. It is because by controlling the sizes of the tail transistors (M1 and M12) of the input- and output-stage such a way that a small tail current for the differential input pair to obtain a long integration time and a better $g_{m}/I_{D2,3}$ ratio for a bigger gain (hence, less offset voltage) and a large tail current for the output latch-stage for fast regeneration, one can get fast speed and low offset voltage with less dependence on $V_{\text{com}}$. 

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{comparator_diagram}
\caption{(a) Double-tail latch-type voltage SA [3] (Comparator 3) (b) Energy efficient two-stage comparator [26] (Comparator 4)}
\end{figure}
For its operation, during reset phase \((\text{Clk}=0V, \text{Clkb}=V_{DD})\), PMOS transistor pair M4 and M5 pre-charge \(D_i\) node capacitances up to \(V_{DD}\) (sequentially, the input transistor pair for the output stage M10 and M11 are turned on and \(\text{Out}\) nodes are reset to 0V) while the both tail transistors (M1 and M12) in the input stage and output latch-stage are off. During evaluation phase \((\text{Clk}=V_{DD}, \text{Clkb}=0V)\), once the input-stage tail transistor M1 is turned on, each \(D_i\) node voltage starts to discharge from \(V_{DD}\) to ground with a different time rate proportional to each input voltage. Then, the voltage difference built between \(D_i\) nodes is passed to \(\text{Out}\) nodes in the output latch-stage through the input transistor pair (M10 and M11) of the output latch-stage. The cross-coupled inverters start to regenerate the voltage difference formed between \(\text{Out}\) nodes as soon as the common-mode voltage at the \(D_i\) nodes is not big enough to clamp \(\text{Out}\) nodes to ground and the PMOS output tail transistor M12 is on.

As expected, since this comparator requires both \(\text{Clk}\) and \(\text{Clkb}\) signals for its operation, high accuracy timing between \(\text{Clk}\) and \(\text{Clkb}\) is required because the second stage has to detect the voltage difference between the differential outputs of the first gain stage at very limited time. If a simple inverter replaces \(\text{Clkb}\), \(\text{Clk}\) has to be able to drive an additional large inverter (heavier clock load) in order to drive the largest transistor M12 in a small delay. If \(\text{Clkb}\) is lagging \(\text{Clk}\), it results in increased delay and if \(\text{Clkb}\) is leading \(\text{Clk}\), it results in increased power dissipation due to existing the short circuit current path M12 to M10/M11 though M8/M9 and it can even increase the latch offset voltage if the device mismatch between M8 and M9 is significant.

The comparator shown in Figure 7 (b) is a different version of two-stage dynamic latched comparator. The operation is similar to the comparator shown in Figure 7 (a). By modifying the output latch-stage, during reset phase \((\text{Clk}=0V, \text{Clkb}=V_{DD})\), its \(D_i\) node capacitances, mostly drain diffusion capacitances of PMOS transistor (M10 and M11) and NMOS transistors (M2 and M3), are reduced, which is much less than the \(D_i\) node
capacitances, mostly gate capacitances of NMOS transistor M10 and M11, in the comparator in [3]; therefore, it can be operated at less power consumption and faster speed. However, since it still has $Clk$ and $Clkb$ for its operation, high accuracy timing between $Clk$ and $Clkb$ is required and due to reduced $Di$ node capacitances the relative capacitance mismatch $\Delta C_{Di}/C_{Di}$ and the input referred RMS noise are also increased.

![Two-stage Dynamic comparator (without offset calibration)](figure8)

**Figure 8** Two-stage Dynamic comparator (without offset calibration) [4] (Comparator 5)

The comparator from [4] without offset calibration technique, shown in **Figure 8**, resolved the problem by replacing $Clkb$ with $Di$ nodes. As a result, $Clk$ load was lessened and the input-referred offset was reduced because the output latch-stage obtains the gain from the both second-input transistor pairs (M10/M11 and M12/M13). However, the improved offset has to trade off with the increased delay since the current drivability of the output load was
weakened due to the fact that transistor M12 and M13 use $Di$ node voltages as their $Ck_b$ signal, which show slow exponential decay shape, and that the maximum drive current of each $Out$ node was reduced to half of the single output tail current of M12 comparing with Comparator 1 since it was separated into two transistors M12 and M13.
Chapter 3

Proposed Dynamic Latched Comparator

3.1 Operation Principles of Proposed Comparator

Figure 9 (a) Schematic of proposed comparator; (b) Signal behavior of proposed comparator ($\Delta V_{in}=100\text{mV}$ (Grey), 10mV (Black) with $V_{DD}=1V$, $f_{clk}=3\text{GHz}$, $C_{load}=7fF$, Temp.$=25^\circ\text{C}$ and $V_{com}=0.7V$)
The schematic and simulated waveforms of the proposed comparator are shown in Figure 9. The circuit is designed and simulated with HSPICE using 90nm PTM (Predictive technology Model) [28], and the design and simulation conditions are $V_{DD}=1\text{V}$, $f_{clk}=3\text{GHz}$, $C_{load}=7\text{fF}$, $Temp.=25^\circ\text{C}$, and common mode voltage $V_{com}=0.7\text{V}$. The basic structure of the proposed comparator stems from the comparators from [3] and [4]. Therefore, the proposed comparator provides better input offset characteristic and faster operation in addition to the advantages of those comparators such as less kickback noise, reduced clock load and removal of the timing requirement between $Clk$ and $Clkb$ over a wide common-mode and supply voltage range.

For its operation, during the pre-charge (or reset) phase ($Clk=0\text{V}$), both PMOS transistor M4 and M5 are turned on and they charge $Di$ nodes’ capacitance to $V_{DD}$, which turn both NMOS transistor M16 and M17 of the inverter pair on and $Di'$ nodes discharge to ground. Sequentially, PMOS transistor M10, M11, M14 and M15 are turned on and they make $Out$ nodes and $Sw$ nodes to be charged to $V_{DD}$ while both NMOS transistors M12 and M13 are being off.

During the evaluation (decision-making) phase ($Clk=V_{DD}$), each $Di$ node capacitance is discharged from $V_{DD}$ to ground in a different time rate in proportion to the magnitude of each input voltage. As a result, an input dependent differential voltage is formed between $Di+$ and $Di$- node. Once either $Di+$ or $Di$- node voltage drops down below around $V_{DD} - |V_q|$, the additional inverter pairs M18/M16 and M19/M17 invert each $Di$ node signal into the regenerated (amplified) $Di'$ node signal. Then the regenerated and different phased $Di'$ node voltages are amplified again and relayed to the output-latch stage by transistor M10–M13. As the regenerated each $Di'$ node voltage is rising from 0V to $V_{DD}$ with a different time interval (or a phase difference, which increases with the increasing input voltage difference $\Delta V_{in}$), M12 and M13 turn on one after another and the output-latch stage starts to regenerate the
small voltage difference transmitted from $Di'$ nodes into a full-scale digital level: $Out+$ node will output logic high ($V_{DD}$) if the voltage difference at $Di'$ nodes $\Delta Di'(t)$ is negative ($Di+ '(t) < Di- '(t)$) and $Out+$ will be low (0V) otherwise. Once either of the $Out$ node voltages drops below around $V_{DD} - |V_{tp}|$, this positive feedback becomes stronger because either PMOS transistor M8 or M9 will turn on.
3.2 Offset Voltage Analysis for Proposed Comparator

3.2.1 Dynamic Differential Input Gain-Stage

The simplified first stage of the proposed comparator is shown in Figure 10. During evaluation phase \((Clk=V_{DD})\), the input differential pair discharges each \(Di\) node voltage from \(V_{DD}\) down to 0V with a different time rate proportional to each input voltage. By assuming that \(\lambda = \gamma = 0\) for simplicity, since both transistor M2 and M3 operate in the saturation region between the time \(t_1\) and \(t_2\) \((t_1: \text{time at which transistor M1 is just turned on at the rising Clk edge and transistor M2 and M3 start to operate in the saturation region,} \ t_2: \text{time at which either of transistor M2 or M3 moves out of the saturation region operation and goes into the linear region operation})\), the drain-to-source current of M2 and M3 are constant over \([t_1, t_2]\).

Therefore, the currents can be expressed as

![Figure 10 Simplified schematic of the dynamic differential input gain stage. (The time point from the tail transistor M1 is just turning on at the rising Clk edge during evaluation phase.)(Image: Simplified schematic of the dynamic differential input gain stage.)](image-url)
\[ C_{Di-} \frac{dV_{Di-}(t)}{dt} = i_{C_{Di-}}(t) = -I_{D2} \]  
(7)

\[ C_{Di+} \frac{dV_{Di+}(t)}{dt} = i_{C_{Di+}}(t) = -I_{D3} \]  
(8)

By integrating both sides of (7) and (8) over \([t_1, t]\) and applying the initial condition: \(V_{Di}(t_1) = V_{DD}\), the following equations are obtained:

\[ V_{Di-}(t) = V_{DD} - \frac{I_{D2}}{C_{Di-}} t \quad V_{Di+}(t) = V_{DD} - \frac{I_{D3}}{C_{Di+}} t \]  
(9)

\[ \Delta V_{Di}(t) = V_{Di-}(t) - V_{Di+}(t) \]  
(10)

Then, under the assumption that \(\Delta V_{in} (= V_{in+} - V_{in-})\) is constant over the integration time \([t_1, t]\) (t is between \(t_1 \) and \(t_2\)), the dynamic gain of the first stage can be defined as

\[ A_{V1}(t) = \frac{\Delta V_{Di}(t)}{\Delta V_{in}} \]  
(11)

By applying the small signal approximation: \(2(V_{GS2,3} - V_{tn}) \gg \Delta V_{in}\) and assuming that \(C_{Di-} = C_{Di+} = C_{Di}\), Equation (11) can be expressed as

\[ A_{V1}(t) = -\frac{g_{m2,3}}{C_{Di}} \frac{I_{D2}}{I_{D2}} \]  
(12)

*where \(g_{m2,3} = \mu_n C_{ox} \frac{w_{2,3}}{L} (V_{com} - V_{D1}(t) - V_{tn2,3})\) *

\[ V_{D1}(t) = (I_{D2} + I_{D3}) \cdot r_{ds1} \approx \text{Const.} \]

Equation (12) reveals that as long as the input transistor pair M2 and M3 operates in the saturation region and \(\Delta V_{in}\) does not change over \([t_1, t_2]\), the dynamic gain \(A_{V1}(t)\) keeps increasing with the increasing time. To maximize the gain \(|A_{V1}(t)|\), \(\frac{g_{m2,3}}{I_{D2}}\) should be maximized because the integration time \(t\) is proportional to \(C_{Di}/I_{D2,3}\) from (9). Simply, this
can be done with reducing the size of transistor M1. However, as equation (9) also indicates, the reduced $I_{D2,3}$ increases the discharging time of $D_i$ node voltages during evaluation phase. Therefore, the higher gain can be achieved at the cost of the increased delay.

Furthermore, by increasing the channel length of the input transistor, for example 90nm to 120nm in 90nm technology, one can get higher gain with the same $W_{2,3}/L$ ratio by reducing short-channel effects such as a dynamic conductance variation due to DIBL. If a negative supply voltage is available, by replacing the ground of the input differential pair with a negative supply voltage and further reducing the size of transistor M1, one can get wider common mode input range. Therefore, this differential input stage can be designed in a different way depending on the requirements such as the speed, offset voltage and common mode input voltage range.

To calculate the offset voltage ($V_{O_{S, pre1}}$) of the input differential pair, both input transistors and $D_i$ node capacitances are assumed to be mismatched. Then, the device parameters and $D_i$ node capacitances can be express as;

\[
\left( \mu_n C_{ox} \frac{W}{L} \right)_2 = \beta \quad \left( \mu_n C_{ox} \frac{W}{L} \right)_3 = \beta + \Delta \beta
\]

\[
V_{tn2} = V_{tn} \quad V_{tn3} = V_{tn} + \Delta V_{tn}
\]

\[
C_{D_{t-}} = C \quad C_{D_{t+}} = C + \Delta C
\]

Then, the value $\Delta V_{in}(=V_{in+} - V_{in-})$ which make $\Delta V_{D_i} = 0$ is the offset voltage ($V_{O_{S, pre1}}$), which is equal to $V_{GS2} - V_{GS3}$. From equation (9), (10) and $\Delta V_{D_i} = 0$, it can be derived that $I_{D2} C_{D_{i+}} = I_{D3} C_{D_{i-}}$. Since we assumed that $D_i$ node capacitances were mismatched ($C_{D_{i+}} \neq C_{D_{i-}}$), $I_{D2}$ cannot be equal to $I_{D3}$. By assuming that $I_{D2} = I_D$ and $I_{D3} = I_D + \Delta I_D$, $\Delta I_D/I_D = \Delta C/C$ is obtained. Therefore, the offset voltage is derived by following way [9].

\[
V_{OS,pre1} = V_{OS,pre2} = V_{GS2} - V_{GS3}
\]
\[
V_{OS,pre1} = \sqrt{\frac{2I_{D2}}{\beta_2}} + V_{tn2} - \sqrt{\frac{2I_{D3}}{\beta_3}} - V_{tn3}
\]

\[
= \sqrt{\frac{2I_D}{\beta}} \left[ 1 - \frac{1 + \frac{\Delta I_D}{I_D}}{1 + \frac{\Delta \beta}{\beta}} \right] - \Delta V_{tn}
\]

(For \( \alpha \ll 1 \), \( \sqrt{1 + \alpha} \approx 1 + \frac{\alpha}{2} \) and \( (\sqrt{1 + \alpha})^{-1} \approx 1 - \frac{\alpha}{2} \))

Assuming \( \Delta I_D/I_D \ll 1 \) and \( \Delta \beta/\beta \ll 1 \), equation (16) is reduced to

\[
V_{OS,pre1} = \sqrt{\frac{2I_D}{\beta}} \left[ 1 - \left(1 + \frac{\Delta I_D}{2I_D}\right)\left(1 - \frac{\Delta \beta}{2\beta}\right) \right] - \Delta V_{tn}
\]

\[
= \sqrt{\frac{I_D}{2\beta}} \left[ - \frac{\Delta I_D}{I_D} + \frac{\Delta \beta}{\beta} \right] - \Delta V_{tn}
\]

\[
= \frac{V_{GS2,3} - V_{tn}}{2} \left[ - \frac{\Delta C}{C} + \frac{\Delta \beta}{\beta} \right] - \Delta V_{tn}
\]

Considering the charge injection mismatch \( \Delta Q \) between PMOS switch transistor M4 and M5, the additional term \( \Delta Q/C_{Di} \) has to be added to equation (19). Since mismatches are independent statistical variables, the random offset voltage \( V_{OS,pre1} \) can be expressed as the variance of (19)

\[
V_{OS,pre1}^2 = \Delta V_{tn}^2 + \left(\frac{V_{GS2,3} - V_{tn}}{2}\right)^2 \left\{ \left(\frac{\Delta C}{C_{Di}}\right)^2 + \left(\frac{\Delta \beta}{\beta}\right)^2 \right\} + \left(\frac{\Delta Q}{C_{Di}}\right)^2
\]

Equation (20) shows that (1) the threshold voltage mismatch is directly referred to the input, (2) \( Di \) node capacitance mismatch (which consists of the mismatch between the gate
capacitances of inverter pair (M18/M16 and M19/M17) and the mismatch between the drain diffusion capacitances of the input transistor pair (M2 and M3)) and the current factor β mismatch increases with the increasing common mode voltage $V_{com}$, and (3) the influence of the charge injection mismatch ($\Delta Q$) on the offset voltage is related to Di node capacitance [9], [28]. Since all terms are related to the size of transistors, from (29) and (30) in Section 3.2.3, the offset voltage can be reduced at the cost of the increasing size of the transistors, hence increasing area and power consumption.
3.2.2 Output Latch-Stage

The inputs of the output latch stage are the gates of transistor M10-13 which are connected to $Di^-$ and $Di^+$ nodes. During evaluation phase ($Clk = V_{DD}$), if $V_{in^+} \neq V_{in^−}$, each $Di'$ node voltage rises from 0V to $V_{DD}$ with a different time interval. Thus, the output stage can make a decision whether logic high or low. However, if $V_{in^+} = V_{in^−}$ and no mismatch exists, both $Di'$ node voltages rise up exactly at the same time rate. This makes both branches of the output stage maintain in a balanced state, which means $V_{out^+}(t) = V_{out^−}(t)$ during all the transient time.

However, if a mismatch exits in the output latch stage, the circuit will be unbalanced making $V_{out^+}(t) \neq V_{out^−}(t)$. In order for the circuit to be balanced, a voltage $V_{OS, latch}$ should be applied between the output of the inverter (M18/M16) and $Di^-$ node to compensate the mismatch when $Di'$ nodes rises. In order to calculate the offset voltage $V_{OS, latch}$ of the output stage, the mismatch in current factor $\beta$ and threshold voltage $V_{th}$ are assumed to be the dominant factors to cause the offset voltage for our analysis.

Figure 11 Simplified schematic of the output stage combined with latch when $Di'$ node voltages ($V_{Di'}$) are reaching around $V_{tn12,13}$ during evaluation phase.
The operation regions of the transistors of the output stage vary with time, however, at the time point when $Di'$ node voltage is around $V_{out12}$, transistor M12 and M13 just turn on and operate in the saturation region. Once $V_{D12,13}$ node voltages drop down below $V_{DD}-V_{tn}$ from $V_{DD}$, transistor M6 and M7 also start to turn on and operate in the saturation region since both their drain and gate voltages are dropping down at the same rate under the balanced condition. Also, transistor M10 and M11 operate in linear region since both $V_{out+}$ and $V_{out-}$ are still around $V_{DD}$. Since the reset transistor M14 and M15 are designed to be much smaller than transistor M12 and M13, their effects on node $V_{D12,13}$ are negligible. Also, the effect on $Out\pm$ nodes from transistor M8 and M9 are ignored since they are in the cut-off region. Therefore, the output latch stage can be drawn in Figure 11 for the time of our analysis.

First, mismatch between transistor M12 and M13 is considered and other pairs are assumed to be perfectly matched. In our analysis, the load capacitance $C_{L1}$ and $C_{L2}$ include the parasitic capacitances at $Out\pm$ nodes. At this time, $C_{L1}$ and $C_{L2}$ are assumed to be the same as $C$.

\begin{align}
I_{D12} &= I_1 \\
I_{D13} &= I_2 \triangleq I_1 + \Delta I_1 \\
I'_1 &= -C_{L1} \frac{dV_{out-}}{dt} \\
I'_2 &= -C_{L2} \frac{dV_{out+}}{dt}
\end{align}

(21)

Since in the balanced condition, $V_{out-} = V_{out+}$, $dV_{out-}/dt = dV_{out+}/dt$, it is fair to say that

\begin{align}
I'_1 &= I'_2 \equiv I''
\end{align}

(23)

Also, from KCL and KVL, the followings are obtained.

\begin{align}
I'_1 &= I_1 - I''_1 \\
I'_2 &= I_2 - I''_2
\end{align}

(24)
\[ I'_1R_{10} = I'_2R_{11} \]  \hspace{1cm} (25)

where,  
\[ R_{30} \approx \frac{1}{\mu p C_{ox} \left( \frac{W_{10}}{L} \right) \left( V_{DD} - V_{Di'} - V_{OS} - |V_{tp}| \right)} \]

\[ R_{11} \approx \frac{1}{\mu p C_{ox} \left( \frac{W_{10}}{L} \right) \left( V_{DD} - V_{Di'} - |V_{tp}| \right)} \]

From (21) and (23) - (25),

\[ \frac{\Delta I_1}{I_1} = \frac{\Delta I_D}{I_D} = \frac{R_{10} - R_{11}}{R_{10}} \left( 1 - \frac{I''}{I_1} \right) \]  \hspace{1cm} (26)

By applying (26) into (18),

\[ V_{OS,12,13}^2 = \left[ \left( \frac{V_{Di'} - V_{tn}}{\sqrt{2}} \right)^2 \left( \frac{\Delta \beta}{\beta} \right)^2 + \Delta V_{in}^2 \right] \cdot \left\{ 1 + \frac{V_{Di'} - V_{tn}}{2(V_{DD} - V_{Di'} - |V_{tp}|)} \left[ 1 - \frac{I''}{I_1} \right] \right\}^{-2} \]  \hspace{1cm} (27)

The equation (27) shows the influence of transistor M10 and M11, which are both reset switches and input transistors for the output-latch stage, on the output-latch stage offset voltage \( V_{OS,latch} \). In the comparators from [3], [26], since both the output branches in the output-latch stage are activated simultaneously by Clkb (not by the signals generated from the pre-amplifier stage), the only pair of the input transistors transfers the gain generated from the previous stage. However, since the proposed comparator and comparator from [4] have two pairs of the input transistors which are linked each other, the offset voltages caused from one pair are compensated by the other input transistor pair. Therefore, as shown in equation (27), the additional term, followed by the square bracket term, compensates the former offset voltage term caused from transistor mismatch between M12 and M13. In addition, as \( V_{Di'} \) increases from \( V_{tn} \) to around \( V_{DD} - |V_{fp}| \), \( V_{OS,latch} \) is further reduced. Therefore, we can only consider the worst case offset voltage \( V_{OS,latch} \) when \( V_{Di'} \) is around \( V_{tn} \).
For mismatch between transistor M6 and M7, from the fact that $I_{D12} = I_{D6}$ and $I_{D13} = I_{D7}$, we have

$$V_{O56,7}^2 = \frac{W_6}{W_{12}} \left[ \left( \frac{\Delta \mu_n C_{ox}}{\mu_n C_{ox}} \right)^2 \frac{(V_{out+} - V_{D13} - V_{tn})^2}{4} + (V_{D13} - V_{D12})^2 + \Delta V_{tn}^2 \right]$$

(28)

where,

$$I_{D12} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W_{12}}{L} \right) (V_{D1'} - V_{tn} - V_{OS})^2$$

$$I_{D13} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W_{12}}{L} \right) (V_{D1'} - V_{tn})^2$$

$$I_{D6} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W_6}{L} \right) (V_{out+} - V_{D12} - V_{tn})^2$$

$$I_{D7} = \frac{1}{2} (\mu_n C_{ox} + \Delta \mu_n C_{ox}) \left( \frac{W_6}{L} \right) (V_{out-} - V_{D13} - V_{tn} - \Delta V_{tn})^2$$

Equation (28) shows that the offset voltage caused by the mismatch between the transistor M6 and M7 is the function size of transistor M6(M7) and M12(M13). Therefore, there is a particular W/L ratio which makes an optimum tradeoff between random offset voltage and transistor size of WxL.

In a similar way, the offset voltage $V_{OS10,11}$ caused by the transistor mismatch between M10 and M11 can be found

$$V_{O510,11}^2 = \left( \frac{\Delta V_{tp}^2}{V_{DD} - V_{D1'} - |V_{tp}|} \right)^2 \cdot \left\{ 1 + \frac{(V_{DD} - V_{D1'} - |V_{tp}|) \left( \frac{g_{m12}}{I_1 - I} \right)}{I_1} \right\}^2$$

(29)

where $g_{m12} = \mu_n C_{ox} \left( \frac{W_{12}}{L} \right) (V_{D1'} - V_{tn})$

To calculate the offset voltage caused from the capacitance mismatches at Out nodes (which includes the load capacitance and parasitic capacitance), it is necessary to assume that $C_{L1} = C$ and $C_{L2} = C + \Delta C$. Applying them to equation (22),

$$I_1'' = I'' \quad I_2'' = I'' + \Delta I''$$

(30)

From (18), (24), (25) and (30),
\[ V_{O_{S\, \text{cloud}}}^2 = \left( \frac{V_{D_{i'}} - V_{th}}{2} \right)^2 \left( \frac{\Delta C}{C} \right)^2 \left\{ 1 + \frac{V_{D_{i'}} - V_{tn}}{2(V_{DD} - V_{D_{i'}} - |V_{tp}|)} \left[ 1 - \frac{I}{I} \right] \right\}^{-2} \] \tag{31}

Equation (31) shows that the offset voltage caused by the capacitance mismatch at between the output nodes is more affected by the relative capacitance mismatch $\Delta C/C$ than the absolute capacitance mismatch $\Delta C$. In addition, the equation (31) can be added to (27) since it has the same additional term in (27).

### 3.2.3 Simulation Results for Output Latch-Stage Offset Voltage

The proposed comparator is designed using 90nm PTM technology [37] and the offset voltages of the output latch stage caused by mismatches in the transistor pairs (M6/7, M10/11, M12/13) are simulated with HSPICE. For our simulation, all variations are assumed to be normally distributed about nominal values and the random mismatch in threshold voltage $V_{th}$ and current factor $\beta (=\mu C_{ox}W/L)$ were modeled as follows [27], [34].

\[ \sigma_{V_{th}} = \frac{A_{V_{th}}}{\sqrt{WL}} \text{ where } W, L \text{ are in } \mu m \] \tag{32}

\[ \sigma_{\beta} = \frac{A_{\beta}}{\sqrt{WL}} \text{ where } W, L \text{ are in } \mu m \] \tag{33}

$A_{V_{th}}$ and $A_{\beta}$ are process dependent parameters and assumed to be $3mV \cdot \mu m$ and $1\% \cdot \mu m$ respectively in our mismatch analysis.

To verify the equation (27)–(29), the nominal design values, $V_{outk} \sim 0.998V$, $V_{D_{i2}}-V_{D_{i3}}=0.702$, $V_m=|V_{tp}|=0.2V$, at the balanced state when $V_{D_{i'}}=0.46V$, were used. The calculated and simulated offset voltages of the output latch stage and input-referred offset voltages caused from the threshold voltage $V_{th}$ mismatches and current factor $\beta$ mismatches are listed in Table I. For simulated results, 100 iterations of Monte Carlo transient simulations.
were performed for each mismatch critical pair with a $\sigma_{Vth}$ and $\sigma_\beta$ standard deviation modeled by equation (32) and (33) at the operation conditions of $V_{DD}=1V$, $f_{CLK}=3GHz$, $V_{com}=0.7V$ and $C_L=7fF$. With the gain (~12V/V) of the dynamic pre-amplifier, the input-referred offset voltages for each mismatch pair are reduced by a factor of 12 where around 1.7 times of the gain is produced by the inverter pairs (M18/16 and M19/M17) followed by the $Di$ node gain of around 7. The simulated results show a good agreement with our calculation and the input referred latch offset voltages can be reduced by the gain of the dynamic pre-amplifier stage when the mismatches of inverter pairs are ignored.

Table 1 Offset Voltages from Mismatch Critical Pairs

<table>
<thead>
<tr>
<th>Mismatched Tr. Pairs</th>
<th>$\sigma_{Vth}$</th>
<th>$\sigma_\beta$</th>
<th>Calculated Latch $\sigma_{Vos}$</th>
<th>Simulated Latch $\sigma_{Vos}$</th>
<th>Calculated Input-referred $\sigma_{Vos}$</th>
<th>Simulated Input-referred $\sigma_{Vos}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>M12/M13</td>
<td>7.74 mV</td>
<td>2.58 %</td>
<td>6.96 mV</td>
<td>8.71 mV</td>
<td>0.58 mV</td>
<td>0.73 mV</td>
</tr>
<tr>
<td>M10/M11</td>
<td>9.49 mV</td>
<td>3.16 %</td>
<td>0.867 mV</td>
<td>1.67 mV</td>
<td>0.072 mV</td>
<td>0.12 mV</td>
</tr>
<tr>
<td>M6/M7</td>
<td>10.6 mV</td>
<td>3.54 %</td>
<td>8.2 mV</td>
<td>8.82 mV</td>
<td>0.68 mV</td>
<td>0.76 mV</td>
</tr>
</tbody>
</table>
Chapter 4

Simulation Results

To compare the performances of the proposed comparator with the previous works, each circuit was designed using 90nm PTM technology with $V_{DD}=1V$ and simulated with HSPICE. In order to compare their relative speeds and total offset voltages, the multi-stage dynamic comparators (Comparator 3–4 and Proposed Comparator) which has a separate input-stage and output-latch stage were designed to have the same $C_{Di}/I_{D2,3}$ ($Di$ nodes capacitance/drain current of M1 and M2) ratio at the same area. All sizes of the input transistor pairs were designed as $W/L (=2\mu m/0.12\mu m)$ to have a relatively the same transconductance and offset voltage, which causes the largest portion of the total offset voltage except for resistive divider comparator [19]. After setting the widths of the mismatch

![Figure 12](image)

**Figure 12** Simulated delay (ps) versus $\Delta V_{in}=|V_{in+}-V_{in-}|$ [V] for selected multi-stage dynamic comparators with different load capacitances of 7fF and 10fF ($V_{DD}=1V$, $V_{com}=0.7V$, $f_{clk}=3GHz$ and Temp.=25°C).
critical transistors to have relatively large size (>1\(\mu\)m), the rest sizes of transistors are optimized for high speed, low offset and less power consumption.

**Figure 11** shows the simulated delay (ps) versus the input voltage difference (V) with the different load capacitance of 7fF and 10fF for the selected multi-stage dynamic latched comparators. Their absolute delays were measured between the 30\% of the rising \(Clk\) edge to 70\% of the rising output edge for the comparator from [3] and [4] and to 30\% of the falling output edge for the proposed comparator. Even with the additional inverter delays formed from transistor M16-19, the proposed comparator outputs faster decision over the comparator from [3] when \(\Delta V_{in}\) is less than around 25mV with 7fF capacitance load and less than around 50mV with 10fF capacitance load since the delay of the proposed comparator is less sensitive to the reduction of \(\Delta V_{in}\) which is around 17ps/decade. As the size of the load gets larger, the proposed comparator shows better overall speed over the comparator [3] since the proposed comparator can drive more current to the load than the comparator [3] and [4] at the same area of the output-stage.

To compare the offset voltages of each comparator, random mismatch in threshold voltage \(V_{th}\) and current factor \(\beta (=\mu C_{ox}W/L)\) were modeled as follows from (29) and (30). \(A_{vth}\) and \(A_\beta\) are process dependent parameters and assumed to be 3mV\(\cdot\mu\)m and 1\%\(\cdot\mu\)m respectively in our mismatch analysis. The overall performance comparison of each comparator is summarized in **Table 2**. The fifth column in **Table 2** shows the resulting input-referred total offset voltage (\(V_{OS}\)) from 500 iterations of Monte Carlo transient simulations with 7fF capacitance load, \(V_{com}=0.7V\) and \(V_{DD}=1V\). The simulated result shows that the resulting \(V_{OS}\) of the proposed one is 16.3mV which is 3.8mV less than that of the comparator [3] while which is 0.5 mV bigger than that of the comparator [4]; however, as shown in **Figure 11** since the proposed comparator shows much faster operation than comparator [4], by simply reducing the size of the input tail transistor M1, the proposed comparator can get
an even less offset voltage than comparator [4] at faster operation. The second and third columns show the number of transistors and total channel widths of the transistors, which can be considered as approximate measures of circuit complexity and chip area. The fourth column is the delays (ps) per the input voltage differences ($\log(AV_{in})$ or decade) of each comparator. The sixth and last column in Table 2 shows that the proposed comparator consumes even less energy than the comparator [3] while presenting more stable delay/log($AV_{in}$), which means that the highest gain is delivered to the output latch stage. From the simulation results, the dynamic voltage gain up to around 12 V/V can be easily obtained, where around 1.7 times of the gain is produced by the inverter pairs (M18/M16 and M19/M17) followed by $Di$ node gain of around 7 V/V. That means that the input referred offset voltage caused from the output latching stage mismatch is reduced by 12 (1.7 X 7) times. Therefore, for the proposed dynamic comparator design, since the output-latch stage is relatively offset insensitive and is able to drive larger current than other multi-stage dynamic comparators at the same area, it does not need to be designed too big. Instead, both inverter pairs inserted between input- and output-stage need to be designed big to lower the overall offset voltage since they are the second dominant component of the total offset voltage.

<table>
<thead>
<tr>
<th>Comparator 1 [19]</th>
<th>Number of Transistors</th>
<th>Width [µm]</th>
<th>Delay [ps]/log($AV_{in}$)</th>
<th>Offset Voltage [mV]</th>
<th>Energy [fJ/Decision]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparator 2 [1]</td>
<td>10</td>
<td>18.4</td>
<td>~59 ps/decade</td>
<td>52 mV</td>
<td>40.2 fJ</td>
</tr>
<tr>
<td>Comparator 3 [3]</td>
<td>11</td>
<td>18.4</td>
<td>~61 ps/decade</td>
<td>20 mV</td>
<td>39.8 fJ</td>
</tr>
<tr>
<td>Comparator 4 [26]</td>
<td>14</td>
<td>18.4</td>
<td>~33 ps/decade</td>
<td>20.1 mV</td>
<td>57.4 fJ</td>
</tr>
<tr>
<td>Comparator 5 [4]</td>
<td>15</td>
<td>18.4</td>
<td>~32 ps/decade</td>
<td>19.1 mV</td>
<td>46.7 fJ</td>
</tr>
<tr>
<td>Proposed Comparator</td>
<td>19</td>
<td>18.3</td>
<td>~17 ps/decade</td>
<td>16.3 mV</td>
<td>52.8 fJ</td>
</tr>
</tbody>
</table>

Table 2 Performance Comparison
Chapter 5

Conclusion and Future Work

5.1 Conclusion

A new dynamic latched comparator which shows lower offset voltage and higher load drivability than the conventional dynamic latched comparators has been designed. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented. As a result, the circuit shows up to 19% less offset voltage and 62% less sensitivity of the delay versus the input voltage difference (delay/log(ΔV_{in})), which is about 17ps/decade, than the conventional double-tail latched comparators at approximately the same area and power consumption.

5.2 Future Work

As mentioned earlier, since the proposed fully dynamic latched comparator can be optimized for either the minimum offset voltage or the maximum load drivability at a limited area according to the design specification, searching for the most suitable application can be one topic for the future works. In addition, offset cancellation techniques can be considered for further reduction of the offset voltage.
REFERENCES


Appendix A

90nm PTM Model File:

*************************************************** ***************************************
* Customized PTM 90nm NMOS
*************************************************** ***************************************
.model  nmos  nmos  level = 54
+version = 4.0  binunit = 1  paramchk = 1  mobmod = 0
+capmod = 2  igcmod = 1  igbmod = 1  geomod = 1
+diomod = 1  rdsmod = 0  rbbodymod = 1  rgatemod = 1
+permod = 1  acnqsmod = 0  trnqsmod = 0

* parameters related to the technology node
+tnom = 27  epsrox = 3.9
+eta0 = 0.0074  nfactor = 1.7  wint = 5e-09
+cgso = 1.9e-10  cgdo = 1.9e-10  xl = -4e-08

* parameters customized by the user
+toxe = 2.05e-09  toxp = 1.4e-09  toxm = 2.05e-09  toxref = 2.05e-09
+dtox = 6.5e-10  lint = 7.5e-09
+vth0 = 0.408  k1 = 0.486  u0 = 0.05383  vsat = 113760
+rdsw = 180  ndep = 2.02e+18  xj = 2.8e-08

* secondary parameters
+ll = 0  w1 = 0  lln = 1  wln = 1
+lw = 0  ww = 0  lwn = 1  wwn = 1
+lwl = 0  wwl = 0  xpart = 0
+k2 = 0.01  k3 = 0
+k3b = 0  w0 = 2.5e-006  dvt0 = 1  dvt1 = 2
+dvt2 = -0.032  dvt0w = 0  dvt1w = 0  dvt2w = 0
+dsub = 0.1  minv = 0.05  voffl = 0  dvt0p = 1.0e-009
+dvt1p = 0.1  lpe0 = 0  lpeb = 0
+ngate = 2e+020  nsd = 2e+020  phin = 0
+cdsc = 0.000  cdscb = 0  cdscd = 0  cit = 0
+voif = -0.13  etab = 0
+vcfb = -0.55  ua = 6e-010  ub = 1.2e-018
+uc = 0  a0 = 1.0  ags = 1e-020
+al = 0  a2 = 1.0  b0 = 0  b1 = 0
+keta = 0.04  dwg = 0  dwb = 0  pelm = 0.04
+pdib1c = 0.001  pdiblc2 = 0.001  pdiblb = -0.005  drout = 0.5
+pvag = 1e-020  delta = 0.01  pscbe1 = 8.14e+008  pscbe2 = 1e-007
+fprot = 0.2  pdits = 0.08  pditsd = 0.23  pditsl = 2.3e+006
+rsch = 5  rsww = 85  rdw = 85
+rdswmin = 0  rdsmin = 0  rswhmin = 0  prw = 0
+prwb = 6.8e-011  wr = 1  alpha0 = 0.074  alpha1 = 0.005
+beta0 = 30  agidl = 0.0002  bgidl = 2.1e+009  cgidl = 0.0002
+egidl = 0.8

+aigbacc = 0.012  bigbacc = 0.0028  cigbacc = 0.002
+nigbacc = 1  aigbinc = 0.014  bigbinc = 0.004  cigbinc = 0.004
+eigbinc = 1.1  nfigbinc = 3  aigec = 0.012  bige = 0.0028
+cigc = 0.002  aigsd = 0.012  bigsd = 0.0028  cigsd = 0.002
+nigc = 1  poxedge = 1  pigcd = 1  ntxo = 1
+xrcgl = 12  xrcgl = 5  cgd = 2.635e-10
+cgsd = 2.635e-10  ckappas = 0.03  ckappad = 0.03  acde = 1
+moin = 15  noff = 0.9  voffc = 0.02
+kt1 = -0.11  kt1l = 0  kt2 = 0.022  ute = -1.5
+ua1 = 4.31e-009  ub1 = 7.61e-018  uc1 = -5.6e-011  ptr = 0
+at = 33000
+fnoimod = 1  tnoimod = 0
+jss = 0.0001  jsws = 1e-011  jswgs = 1e-010  njs = 1
+ijthfw = 0.01  ijsre = 0.001  bvs = 10  jxbvs = 1
+jsd = 0.0001  jswd = 1e-011  jswgd = 1e-010  njd = 1
+ijthd = 0.01  ijsrd = 0.001  bvd = 10  jxbvd = 1
+pbs = 1  cjs = 0.0005  mjs = 0.5  psbws = 1
+cjsxs = 5e-010  mjsxs = 0.33  pbswgs = 1  cjsxs = 3e-010
+pmsxs = 0.33  pdb = 1  cjd = 0.0005  mjds = 0.5
+pmswd = 1  cjswd = 5e-010  mjswd = 0.33  pbswgd = 1
+cjswsd = 5e-010  mjswsd = 0.33  tkbsw = 0.005  tcj = 0.001
+tpbsw = 0.005  tcjw = 0.001  pbswgs = 1  cjswgs = 0.0001
+xtis = 3  xtid = 3
+rdmc = 0e-006  dmci = 0e-006  dmdg = 0e-006  dmct = 0e-007
+dwj = 0.0e-008  xgw = 0e-007  xgl = 0e-008
+rshg = 0.4  gbmin = 1e-010  rbpb = 5  rbpd = 15
+rbps = 15  rdbd = 15  rbsb = 15  ngcon = 1
*************************************************** ***************************************
* Customized PTM 90nm PMOS
*************************************************** ***************************************
.model  pmos  pmos  level = 54
+version = 4.0  binunit = 1  paramchk = 1  mobmod = 0
+capmod = 2  igcmod = 1  igbmod = 1  geomod = 1
+diomod = 1  rdsmod = 0  rbodmod = 1  rgatemod = 1
+permod = 1  acnqmod = 0  trnqmod = 0
* parameters related to the technology node
+tnom = 27  epsrox = 3.9
+etal = 0.0074  nfactor = 1.7  wint = 5e-009
+cgs = 1.9e-10  cgs = 1.9e-10  xl = 4e-008
* parameters customized by the user
+toxe = 2.15e-09  toxp = 1.4e-09  toxm = 2.15e-09  toxref = 2.15e-09
+dtox = 7.5e-10  lint = 7.5e-09
+vth0 = -0.354  k1 = 0.422  u0 = 0.00678  vsat = 70000
+rdsw = 200  ndep = 1.52e+18  xj = 2.8e-08
* secondary parameters
+ll = 0  wl = 0  lln = 1  wln = 1
+lw = 0  ww = 0  lwn = 1  wwn = 1
+lwl = 0  wwl = 0  xpar = 0
+k2 = -0.01  k3 = 0
+k3b  = 0
+dvt2 = -0.032
+dsub = 0.1
+dvt1  = 0.05
+ngate = 2e+020
+cdsc = 0.000
+voff = -0.126
+vfb  = 0.55
+uc = 0
+a1 = 0
+keta = -0.047
+pdiblc1 = 0.001
+pavg = 1e-020
+fprout = 0.2
+rsh = 5
+rdswmin = 0
+prwb = 6.8e-011
+beta0 = 30
+egid = 0.8
+aigbacc = 0.012
+ngibacc = 1
+cibgnv = 1.1
+cigc = 0.0008
+nigc = 1
+xrcrg1 = 12
+cgbo = 2.56e-011
+cgsd = 2.653e-10
+moin = 15
+kt1 = -0.11
+ua1 = 4.31e-009
+at = 33000

+fnoimod = 1
tnoimod = 0

+jss = 0.0001
+ijsfwd= 0.01
+jsd  = 0.0001
+ijsfwd= 0.01
+pbs = 0.33
+pbswd = 1
+jssws = 5e-010
+msjsws = 0.33
+xtis = 3
+dmcg = 0e-006
+dwj = 0.0e-008
+rshg = 0.4
+rbps = 15
Appendix B

HSPICE Netlist Files for Simulated Comparator Circuits:

1. Comparator 1 [19]

*****************************************************************************
.title 'Optimized Lewis-Gray Dynamic Latched Comparator'
.include "..\models\90ntt.sp"
.include "..\models\90ptt.sp"
*****************************************************************************
*** key parameters *******************************************************
.param v_supply=1
.param vdiff=20m
.param vcom=0.7
.param clk_freq=3G

*** Netlist ****************************************************************************
v00  gnda  0 0
v0  vdda  gnda v_supply
v1  vcm  gnda  vcom
v2  vdd  gnd  v_supply

*** Clk ********************************************************************************
v_clk  clk  gnda  PULSE  ( v3 v4 td tr tf pw per )
.param v3=0  v4=1
+  td=50p  td2=50p
+  tr='trf_ratio*per'  tf='trf_ratio*per'
+  pw='per/2-(tr+tf)/2'
+  per='1/clk_freq'
+  trf_ratio=0.01

*** Clk buffers ***************************************************************
*mpb11  b_clk  vclk  vdd  vdd  pmos  L='lmin'  W=0.25*(wn1)*3*4'
*mnbb1  b_clk  vclk  0 0  nmos  L='lmin'  W=0.25*(wn1)*3'
*mpb12  clk  b_clk  vdd  vdd  pmos  L='lmin'  W=0.25*(wn1)*3*4'
*mnbb12  clk  b_clk  0 0  nmos  L='lmin'  W=0.25*(wn1)*3'

*** Diff Input ************************************
vin+  in+  vcm  PULSE  ( '-vdiff'  'vdiff'  td_in 0.01n 0.01n 0.32n 0.66n )
.vref in-  vcm  PULSE  ( 0 0  td_in 0.01n 0.01n 0.32n 0.66n )
.param td_in=0.3n

************ input stage *******************************************************
m1a  Di-  in+  0 0  nmos  L='lmin2'  W='wn1'
m1b  Di+  in-  0 0  nmos  L='lmin2'  W='wn1'
*mn2a  Di-  vref-  0 0  nmos  L='lmin2'  W='wn2'
*mn2b  Di+  vref+  0 0  nmos  L='lmin2'  W='wn2'
m3  1  out+  Di+  0 0  nmos  L='lmin3'  W='wn3'
m4  2  out-  Di-  0 0  nmos  L='lmin3'  W='wn3'
m5  out-  clk  1 0  nmos  L='lmin'  W='wn5'
m6  out+  clk  2  0  nmos  L='lmin'  W='wn5'
m7  out-  out+  vdd  vdd  pmos  L='lmin'  W='wp7'
m8  out+  out-  vdd  vdd  pmos  L='lmin'  W='wp7'
m9  out-  clk  vdd  vdd  pmos  L='lmin'  W='wp9'
m10 out+  clk  vdd  vdd  pmos  L='lmin'  W='wp9'

.param  lmin=100n
  +  lmin2=120n
  +  lmin3=120n
  +  wn1=1u
  +  wn3=5u
  +  wn5=1.8u
  +  wp7=1.4u
  +  wp9=1.8u

c1  out+  gnd  cload
c2  out-  gnd  cload
.param  cload=7f

** Analysis setup *************************************************************
.TEMP  25
.OPTIONS  POST
.WIDTH  OUT=80
 tran  1p  1n  sweep  5m  50m  5m
.print  di=par('abs(v(di-)-v(di+))')
.print  vout_pmn=par('abs(v(out+)-v(out-))')
.measure delay1
  +  trig  v(clk)  val='v_supply*0.3'  rise=2
  +  targ  v(out-)  val='v_supply*0.3'  fall=1
.measure delay2
  +  trig  v(clk)  val='v_supply*0.3'  rise=3
  +  targ  v(out+)  val='v_supply*0.3'  fall=2
.measure Delay_ave  param='(delay1+delay2)/2'
.meas tran  qtot  integral  i(v2)  from=373p  to=706p
.meas tran  iave  avg  i(v2)  from=373p  to=706p
.meas etot  param='v_supply*qtot'
.meas ptot  param='v_supply*iave'
.END
************************************************************************************
2. Comparator 2 [1]

***************************************************
.title 'Optimized Latch-type Voltage SA'
.include "..\models\90ntt.sp"
.include "..\models\90ptt.sp"

*** key parameters ***************************************************
.param v_supply=1
.param vdiff=20m
.param vcom=0.7
.param clk_freq=3G

*** Netlist ***************************************************
v00 gnda  0 0
v0 vdda  gnda v_supply
v1 vcm  gnda vcom
v2 vdd  gnd v_supply

*** Clk ***************************************************
v_clk clk gnda PULSE ( v3 v4 td tr tf pw per )
.param v3=0  v4=1
+ td=50p  td2=50p
+ tr='trf_ratio*per'  tf='trf_ratio*per'
+ pw='per/2-(tr+tf)/2'
+ per='1clk_freq'
+ trf_ratio=0.01

*** Clk buffers ***************************************************
*mpb11 b_clk vclk vdd vdd pmos L='lmin'  W=0.25*(wn1)*3*4'
*mbn11 b_clk vclk 0 0 nmos L='lmin'  W=0.25*(wn1)*3'
*mpb12 clk b_clk vdd vdd pmos L='lmin'  W=0.25*(wn1)*3*4'
*mbn12 clk b_clk 0 0 nmos L='lmin'  W=0.25*(wn1)*3'

*** Diff Input ***************************************************
vin+ in+ vcm PULSE ( '-vdiff'  'vdiff' td_in 0.01n 0.01n 0.32n 0.66n )

.vref in- vcm PULSE ( 0 0 td_in 0.01n 0.01n 0.32n 0.66n )
.param td_in=0.3n

************ input stage **********************************

mn1  l  clk  gnd  gnd  nmos L='lmin1'  W='wn1'
mn2  Di-  in+  l  gnd  nmos L='lmin2'  W='wn2'
mn3  Di+  in-  l  gnd  nmos L='lmin2'  W='wn2'
mp4  out-  clk  vdd  vdd  pmos L='lmin'  W='wp4'
mp5  out+  clk  vdd  vdd  pmos L='lmin'  W='wp4'
mn6  out-  out+  Di-  gnd  nmos L='lmin'  W='wn6'
mn7  out+  out-  Di+  gnd  nmos L='lmin'  W='wn6'
mp8  out-  out+  vdd  vdd  pmos L='lmin'  W='wp8'
mp9  out+  out-  vdd  vdd  pmos L='lmin'  W='wp8'
mp10 Di-  clk  vdd  vdd  pmos L='lmin'  W='wp10'
mp11 Di+  clk  vdd  vdd  pmos L='lmin'  W='wp10'
.param lmin=100n
+ lmin1=120n
+ lmin2=120n
+ wn1=2u
+ wn2=2u
+ wp4=2u
+ wn6=3u
+ wp8=0.8u
+ wp10=0.4u

C1 out+ gnd cload
C2 out- gnd cload
.param cload=7f

** Analysis setup *********************************************************
.TEMP 25
.OPTIONS POST
.WIDTH OUT=80

.tran 1p 1n sweep 5m 50m 5m
.print di=par('abs(v(di-)-v(di+))')
.print vout_pmn=par('abs(v(out+)-v(out-))')

.measure delay1
+ trig v(clk) val=v_supply*0.3' rise=2
+ targ v(out-) val=v_supply*0.3' fall=1

.measure delay2
+ trig v(clk) val=v_supply*0.3' rise=3
+ targ v(out+) val=v_supply*0.3' fall=2

.measure Delay_ave param='(delay1+delay2)/2'

.meas tran qtot integral i(v2) from=373p to=706p
.meas tran iave avg i(v2) from=373p to=706p
.meas etot param='v_supply*qtot'
.meas ptot param='v_supply*iave'

.END

********************************************************************************************
3. Comparator 3 [3]

.title 'Double-Tail SA'
.include "./models\90ntt.sp"
.include "./models\90ptt.sp"

*** key parameters ******************************************************************************
.param v_supply=1
.param vdiff=20m
.param vcom=0.7
.param clk_freq=3G

*** Netlist *******************************************************************************
\param v_supply=1
\param vdiff=20m
\param vcom=0.7
\param clk_freq=3G

*** Clk *******************************************************************************
\param v_supply=1
\param vdiff=20m
\param vcom=0.7
\param clk_freq=3G

*** Diff Input ******************************************************************************
\param v_supply=1
\param vdiff=20m
\param vcom=0.7
\param clk_freq=3G

************ input stage ******************************************************************************
.param lmin=100n
+ lmin1=120n
+ lmin2=120n
+ wn1=0.44u
+ wn2=2u
+ wp4=0.5u

*** output stage ***************************************************************************

mn6  out+  out-  gnd  gnd  nmos  L='lmin'  W='wn6'
mn7  out-  out+  gnd  gnd  nmos  L='lmin'  W='wn6'
mp8  out+  out-  2  vdd  pmos  L='lmin'  W='wp8'
mp9  out-  out+  2  vdd  pmos  L='lmin'  W='wp8'

mn10 out+  Di-  gnd  gnd  nmos  L='lmin'  W='wn10'
mn11 out-  Di+  gnd  gnd  nmos  L='lmin'  W='wn10'
mp12  2  clkb  vdd  vdd  pmos  L='lmin'  W='wp12'

.param wp12=4u
+ wn6=0.5u
+ wp8=1.8u
+ wn10=1.6u

c1  out+  gnd  clload
c2  out-  gnd  clload

.param clload=7f

** Analysis setup ***************************************************************************

.TEMP  25
.OPTIONS POST
.WIDTH  OUT=80

.tran 1p 1n sweep 5m 50m 5m

.print  di=par('abs(v(di-)-v(di+))')
.print  vout_pmn=par('abs(v(out+)-v(out-))')

.measure delay1
+ trig  v(clk)  val='v_supply*0.3'  rise=2
+ trig  v(out+)  val='v_supply*0.7'  rise=1

.measure delay2
+ trig  v(clk)  val='v_supply*0.3'  rise=3
+ trig  v(out-)  val='v_supply*0.7'  rise=2

.measure Delay_ave  param='(delay1+delay2)/2'

.meas tran qtot integral i(v2) from=373p to=706p
.meas tran iave avg i(v2) from=373p to=706p
.meas etot  param='v_supply*qtot'
.meas ptot  param='v_supply*iave'

.END
4. Comparator 4 [26]

.include "./models/90ntt.sp"
.include "./models/90ptt.sp"

*** key parameters ******************************************************************************
.param v_supply=1
.param vdiff=20m
.param vcom=0.7
.param clk_freq=3G

*** Netlist **************************************************************************
.v00 gnda 0 0
.v0 vdda gnda v_supply
.v1 vcm gnda vcom
.v2 vdd gnd v_supply

*** Clk ********************************************************************************
.v_clk clk gnda PULSE ( v3 v4 td tr tf pw per )
*v_clkb vclkb gnda PULSE ( v4 v3 td2 tr tf pw per )
.mp15 clkb clk vdd vdd pmos L='lmin' W='wp15'
.mn14 clkb clk 0 0 nmos L='lmin' W='wn14'
.param wp15=0.2u
+ wn14=0.2u
.param v3=0 v4=1
+ td=50p td2=50p
+ tr='trf_ratio*per' tf='trf_ratio*per'
+ pw='per/(2-(tr+tf)/2'
+ per='1/clk_freq'
+ trf_ratio=0.01

*** Diff Input **************************************************************************
.vin+ in+ vcm PULSE ( -vdiff 'vdiff' td_in 0.01n 0.01n 0.32n 0.66n )
.vref in- vcm PULSE ( 0 0 td_in 0.01n 0.01n 0.32n 0.66n )
.param td_in=0.3n

************* input stage ******************************************************************************
.mn1 1 clk gnd gnd nmos L='lmin1' W='wn1'
.mn2 Di- in+ 1 gnd nmos L='lmin2' W='wn2'
.mn3 Di+ in- 1 gnd nmos L='lmin2' W='wn2'
.mp4 Di- clkb vdd vdd pmos L='lmin' W='wp4'
.mp5 Di+ clkb vdd vdd pmos L='lmin' W='wp4'
.param lmin=100n + lmin1=120n + lmin2=120n + wn1=0.4u + wn2=2u + wp4=0.6u

************ output stage *******************************************************

mn6  out+  out-  gnd  gnd  nmos  L='lmin'  W='wn6'
mn7  out-  out+  gnd  gnd  nmos  L='lmin'  W='wn6'
mp8  2  out-  vdd  vdd  pmos  L='lmin'  W='wp8'
mp9  3  out+  vdd  vdd  pmos  L='lmin'  W='wp8'
mp10  out+  Di-  2  vdd  pmos  L='lmin'  W='wp10'
mp11  out-  Di+  3  vdd  pmos  L='lmin'  W='wp10'
mn12  out+  clkb  gnd  gnd  nmos  L='lmin'  W='wn12'
mn13  out-  clkb  gnd  gnd  nmos  L='lmin'  W='wn12'

.param  wn6=0.8u + wp8=2u + wp10=3u + wn12=0.4u

c1  out+  gnd  cload
c2  out-  gnd  cload

.param  cload=7f

** Analysis setup ***************************************************************

.TEMP     25
.OPTIONS   POST
.WIDTH     OUT=80

.tran  lp ln sweep 5m 50m 5m

.print  di=par('abs(v(di-)-v(di+))')
.print  vout_pmn=par('abs(v(out+)-v(out-))')

.measure delay1 + trig  v(clk)   val='v_supply*0.3'  rise=2 + targ  v(out+)  val='v_supply*0.7'  rise=1
.measure delay2 + trig  v(clk)   val='v_supply*0.3'  rise=3 + targ  v(out-)  val='v_supply*0.7'  rise=2

.measure Delay_ave   param='(delay1+delay2)/2'

.meas tran  qtot  integral i(v2)  from=373p  to=706p
.meas tran  iave  avg  i(v2)  from=373p  to=706p
.meas  etot   param='v_supply*qtot'
.meas  ptot   param='v_supply*iave'

.END

*******************************************************************************

.title 'Two-stage Dynamic Latched Comparator from JNP'

.include "..\models\90ntt.sp"
.include "..\models\90ptt.sp"

*** key parameters ******************************** ********************************************
.param v_supply=1
.param vdiff=20m
.param vcom=0.7
.param clk_frew=3G

*** Netlist ************************************************************************************
v00  gnda  0 0
v0  vdda  gnda  v_supply
v1  vcm  gnda  vcom
v2  vdd  gnd  v_supply

*** Clk ***********************************************************************************
v_clk  clk  gnda  PULSE  (v3 v4 td tr tf pw per)
*v_clk  vclkb  gnda  PULSE  (v3 v4 td2 tr tf pw per)
mpb15  clkb  clk  vdd  vdd  pmos  L='lmin'  W='wp15'
mnb14  clkb  clk  0 0  nmos  L='lmin'  W='wn14'
.param wp15=0.2u
+  wn14=0.2u
.param v3=0  v4=1
+  td=50p  td2=50p
+  tr='trf_ratio*per'
+  tf='trf_ratio*per'
+  pw='per/2-(tr+tf)/2'
+  per='1/clk_frew'
+  trf_ratio=0.01

*** Clk buffers ****************************************************************************
*mpb11  b_clk  vclk  vdd  vdd  pmos  L='lmin'  W=0.25*(wn1)*3*4'
*mpb11  b_clk  vclk  0 0  nmos  L='lmin'  W=0.25*(wn1)*3'
*mpb12  clkb  b_clk  vdd  vdd  pmos  L='lmin'  W=0.25*(wn1)*3*4*4'
*mbn12  clkb  b_clk  0 0  nmos  L='lmin'  W=0.25*(wn1)*3*4'

*** Diff Input ************************************ ******************************************
v_in+  in+  vcm  PULSE (vdiff)  'vdiff'  td_in  0.01n  0.01n  0.32n  0.66n
vref  in-  vcm  PULSE (0)  0  td_in  0.01n  0.01n  0.32n  0.66n
.param td_in=0.3n

*********** input stage  ************************************************************
mn1  1  clk  gnd  gnd  nmos  L='lmin1'  W='wn1'
mn2  Di-  in+  l  gnd  nmos  L='lmin2'  W='wn2'
mn3  Di+  in-  l  gnd  nmos  L='lmin2'  W='wn2'
mp4  Di-  clk  vdd  vdd  pmos  L='lmin'  W='wp4'
mp5  Di+  clk  vdd  vdd  pmos  L='lmin'  W='wp4'
**Analysis setup**

1. TEMP 25
2. OPTIONS POST
3. WIDTH OUT=80
4. tran 1p 1n sweep 5m 50m 5m
5. print di=par('abs(v(di-)-v(di+))')
6. print vout_pmn=par('abs(v(out+)-v(out-))')
7. measure delay1
   + trig v(clk) val='v_supply*0.3' rise=2
   + targ v(out+) val='v_supply*0.7' rise=1
8. measure delay2
   + trig v(clk) val='v_supply*0.3' rise=3
   + targ v(out-) val='v_supply*0.7' rise=2
9. measure Delay_ave param='(delay1+delay2)/2'
10. meas tran qtot integral i(v2) from=373p to=706p
11. meas tran iave avg i(v2) from=373p to=706p
12. meas etot param='v_supply*qtot'
13. meas ptot param='v_supply*iave'

.END

.include "..\models\90ntt.sp"
.include "..\models\90ptt.sp"

*** key parameters ****************************************************************************************************************************************
.param v_supply=1
.param vdiff=20m
.param vcom=0.7
.param clk_freq=3G

*** Netlist ****************************************************************************************************************************************
v00 gnda 0 0
v0 vdda gnda v_supply
v1 vcm gnda vcom
v2 vdd gnd v_supply

*** Clk ****************************************************************************************************************************************
v_clk clk gnda PULSE ( v3 v4 td tr tf pw per )
*v_clk vclkb gnda PULSE ( v4 v3 td2 tr tf pw per )

mpb15 clkb clk vdd vdd pmos L='lmin' W='wp15'
mnb14 clkb clk 0 0 nmos L='lmin' W='wn14'

.param wp15=0.2u
+ wn14=0.2u

.param v3=0
+ v4=1
+ td=50p
+ td2=50p
+ tr='trf_ratio*per'
+ tf='trf_ratio*per'
+ pw='per/2-(tr+tf)/2'
+ per='1/clk_freq'
+ trf_ratio=0.01

*** Clk buffers ****************************************************************************************************************************************
*mpb11 b_clk vclk vdd vdd pmos L='lmin' W=0.25*(wn1)*3*4'
*mnb11 b_clk vclk 0 0 nmos L='lmin' W=0.25*(wn1)*3'
*mpb12 clk b_clk vdd vdd pmos L='lmin' W=0.25*(wn1)*3*4*4'
*mnb12 clk b_clk 0 0 nmos L='lmin' W=0.25*(wn1)*3*4'

*** Diff Input ****************************************************************************************************************************************
v_in+ in+ vcm PULSE ( -vdiff 'vdiff' td_in 0.01n 0.01n 0.32n 0.66n )
v_ref in- vcm PULSE ( 0 0 td_in 0.01n 0.01n 0.32n 0.66n )

.param td_in=0.3n

----------- input stage -----------

mn1 l clk gnd gnd nmos L='lmin1' W='wn1'
mn2 Di- in+ l gnd nmos L='lmin2' W='wn2'
mn3 Di+ in- l gnd nmos L='lmin2' W='wn2'
mp4 Di- clk vdd vdd pmos L='lmin' W='wp4'
mp5 Di+ clk vdd vdd pmos L='lmin' W='wp4'

.param lmin=100n
+ lmin1=120n
+ lmin2=120n
+ wn1=0.5u
+ wn2=2u
+ wp4=0.6u

************************** output stage ****************************************************
mn6 out- out+ 2 gnd nmos L='lmin' W='wn6'
mn7 out+ out- 3 gnd nmos L='lmin' W='wn6'
mp8 out- out+ vdd vdd pmos L='lmin' W='wp8'
mp9 out+ out- vdd vdd pmos L='lmin' W='wp8'
mp10 out- Di-b vdd vdd pmos L='lmin' W='wp10'
mp11 out+ Di+b vdd vdd pmos L='lmin' W='wp10'
mn12 2 Di-b gnd gnd nmos L='lmin' W='wn12'
mn13 3 Di+b gnd gnd nmos L='lmin' W='wn12'
mp14 2 Di-b vdd vdd pmos L='lmin' W='wp14'
mp15 3 Di+b vdd vdd pmos L='lmin' W='wp14'
mn16 bDi-b Di- gnd gnd nmos L='lmin' W='wn16'
mn17 Di+b Di+ gnd gnd nmos L='lmin' W='wn16'
mp18 bDi-b Di- vdd vdd pmos L='lmin' W='wp18'
mp19 Di+b Di+ vdd vdd pmos L='lmin' W='wp18'

.param dvth0=0
.vmc0 Di-b bDi-b dvth0

.param wn16=0.6u
+ wp18=1.8u
+ wn6=0.8u
+ wp8=0.4u
+ wp10=1u
+ wn12=1.5u
+ wp14=0.2u

c1 out+ gnd cload
.c2 out- gnd cload

.param cload=7f

** Analysis setup ************************************************************
.TRAN 1p 1n sweep 5m 50m 5m
.MEAS tran qtot integral i(v2) from=0.380n to=0.713n
.MEAS tran iave avg i(v2) from=0.380n to=0.713n
.MEAS etot param='v_supply*qtot'
.MEAS ptot param='v_supply*iave'

.PRINT di=par('abs(v(di-)-v(di+))') dib=par('abs(v(di-b)-v(di+b))')
.PRINT vout_pmn=par('abs(v(out+)-v(out-))')

.MEASURE delay1
+ trig v(clk) val='v_supply*0.3' rise=2
+ targ v(out-) val='v_supply*0.3' fall=1

.MEASURE delay2
+ trig v(clk) val='v_supply*0.3' rise=3
+ targ v(out+) val='v_supply*0.3' fall=2

.MEASURE Delay_ave param='(delay1+delay2)/2'
.alter
.param cload=10f
.END

***************************************************  ***************************************

***************************************************  ***************************************

$title 'Monte Carlo Transient Simulation for Proposed Comparator'

.include  "../models/90ntt.sp"
.include  "../models/90ptt.sp"

*** key parameters ******************************** ******************************************
.param v_supply=1
.param vdiff=17m
.param vcom=0.7
.param clk_freq=3G
.param avth2=3m
+  avth3=3m
+  avth4=3m
+  avth5=3m
+  avth6=3m
+  avth7=3m
+  avth8=3m
+  avth9=3m
+  avth10=3m
+  avth11=3m
+  avth12=3m
+  avth13=3m
+  avth14=3m
+  avth15=3m
+  avth16=3m
+  avth17=3m
+  avth18=3m
+  avth19=3m
.param abeta2=0.01
+  abeta3=0.01
+  abeta4=0.01
+  abeta5=0.01
+  abeta6=0.01
+  abeta7=0.01
+  abeta8=0.01
+  abeta9=0.01
+  abeta10=0.01
+  abeta11=0.01
+  abeta12=0.01
+  abeta13=0.01
+  abeta14=0.01
+  abeta15=0.01
+  abeta16=0.01
+  abeta17=0.01
+  abeta18=0.01
+  abeta19=0.01
*** Netlist *************************************** *******************************************

v00  gnda  0 0
v0  vdda  gnda  v_supply
v1  vcm  gnda  vcom
v2  vdd  gnd  v_supply

*** Clk ***********************************************************************************

v_clk  clk  gnda  PULSE  ( v3 v4 td tr tf pw per )
*v_clk  clk  gnda  PULSE  ( v4 v3 td tr tf pw per )

mpb15  clkb  clk  vdd  vdd  pmos  L='lmin'  W='wp15'
  mnb14  clkb  clk  0 0  nmos  L='lmin'  W='wn14'

*.param wp15=0.2u
  + wn14=0.2u

*.param v3=0  v4=1
  + td=50p  td2=50p
  + tr='trf_ratio*per'  tf='trf_ratio*per'
  + pw='per/2-(tr+tf)/2'
  + per='1/clock_freq'
  + trf_ratio=0.01

*** Clk buffers ****************************************************************************

*mpb11  b_clk  vclk  vdd  vdd  pmos  L='lmin'  W='0.25*(wn1)*3*4'
*mn11  b_clk  vclk  0 0  nmos  L='lmin'  W='0.25*(wn1)*3'
*mpb12  clk  b_clk  vdd  vdd  pmos  L='lmin'  W='0.25*(wn1)*3*4*4'
*mn12  clk  b_clk  0 0  nmos  L='lmin'  W='0.25*(wn1)*3*4'

*** Diff Input ************************************ ******************************************

vin+  in+  vcm  PULSE  ( '-vdiff'  'vdiff'  td_in  0.01n  0.01n  0.32n  0.66n )
vref  in-  vcm  PULSE  ( 0 0  td_in  0.01n  0.01n  0.32n  0.66n )

*.param td_in=0.3n

************ input stage ************************** ******************************************

mn1  l  clk  gnd  gnd  nmos  L='lmin'  W='wn1'

mn2  Di-  vg2_shift  1  gnd  nmos  L='lmin2'  W='wn2'
  m'=1-multn2'

mn3  Di+  vg3_shift  1  gnd  nmos  L='lmin2'  W='wn2'
  m'=1-multn3'

*.param multn2=agauss(0, 'abeta2/sqrt(2*lmin2*wn2*1e+12)', 1)
*.param dvth2=agauss(0, 'avth2/sqrt(2*lmin2*wn2*1e+12)', 1)

vmc2  in+  vg2_shift  dvth2

vmc3  in-  vg3_shift  dvth3

mp4  Di-  vg4_shift  vdd  vdd  pmos  L='lmin'  W='wp4'
  m'=1-multn4'

mp5  Di+  vg5_shift  vdd  vdd  pmos  L='lmin'  W='wp4'
  m'=1-multn5'

*.param multn4=agauss(0, 'abeta4/sqrt(2*lmin*wp4*1e+12)', 1)
*.param dvth4=agauss(0, 'avth4/sqrt(2*lmin*wp4*1e+12)', 1)

vmc4  clk  vg4_shift  dvth4

vmc5  clk  vg5_shift  dvth5

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.param  lmin=100n
+  lmin1=120n
+  lmin2=120n
+  wn1=0.5u
+  wn2=2u
+  wp4=0.6u

************ output stage ****************************

mn6 out-  vg6_shift  2  gnd  nmos  L='lmin'  W='wn6'
m='1-multn6'

mn7 out+  vg7_shift  3  gnd  nmos  L='lmin'  W='wn6'
m='1-multn7'

.mparam  multn6=agauss(0, 'abeta6/sqrt(2*lmin*wn6*1e+12)', 1)
.
.mparam  dvth6=agauss(0, 'avth6/sqrt(2*lmin*wn6*1e+12)', 1)
vmc6 out+  vg6_shift  dvth6

.mparam  multn7=agauss(0, 'abeta7/sqrt(2*lmin*wn6*1e+12)', 1)
.mparam  dvth7=agauss(0, 'avth7/sqrt(2*lmin*wn6*1e+12)', 1)
vmc7 out-  vg7_shift  dvth7

mp8 out-  vg8_shift  vdd  vdd  pmos  L='lmin'  W='wp8'
m='1-multn8'

mp9 out+  vg9_shift  vdd  vdd  pmos  L='lmin'  W='wp8'
m='1-multn9'

.mparam  multn8=agauss(0, 'abeta8/sqrt(2*lmin*wp8*1e+12)', 1)
.
.mparam  dvth8=agauss(0, 'avth8/sqrt(2*lmin*wp8*1e+12)', 1)
vmc8 out+  vg8_shift  dvth8

.mparam  multn9=agauss(0, 'abeta9/sqrt(2*lmin*wp8*1e+12)', 1)
.mparam  dvth9=agauss(0, 'avth9/sqrt(2*lmin*wp8*1e+12)', 1)
vmc9 out-  vg9_shift  dvth9

mp10 out-  vg10_shift  vdd  vdd  pmos  L='lmin'  W='wp10'
m='1-multn10'

mp11 out+  vg11_shift  vdd  vdd  pmos  L='lmin'  W='wp10'
m='1-multn11'

.mparam  multn10=agauss(0, 'abeta10/sqrt(2*lmin*wp10*1e+12)', 1)
.
.mparam  dvth10=agauss(0, 'avth10/sqrt(2*lmin*wp10*1e+12)', 1)
vmc10 Di-b  vg10_shift  dvth10

.mparam  multn11=agauss(0, 'abeta11/sqrt(2*lmin*wp10*1e+12)', 1)
.mparam  dvth11=agauss(0, 'avth11/sqrt(2*lmin*wp10*1e+12)', 1)
vmc11 Di+b  vg11_shift  dvth11

mn12  2  vg12_shift  gnd  gnd  nmos  L='lmin'  W='wn12'
m='1-multn12'

mn13  3  vg13_shift  gnd  gnd  nmos  L='lmin'  W='wn12'
m='1-multn13'

.mparam  multn12=agauss(0, 'abeta12/sqrt(2*lmin*wn12*1e+12)', 1)
.
.mparam  dvth12=agauss(0, 'avth12/sqrt(2*lmin*wn12*1e+12)', 1)
vmc12 Di-b  vg12_shift  dvth12

.mparam  multn13=agauss(0, 'abeta13/sqrt(2*lmin*wn12*1e+13)', 1)
.mparam  dvth13=agauss(0, 'avth13/sqrt(2*lmin*wn12*1e+13)', 1)
vmc13 Di+b  vg13_shift  dvth13

mp14  2  vg14_shift  vdd  vdd  pmos  L='lmin'  W='wp14'
m='1-multn14'
mp15 3 vg15_shift vdd vdd pmos L='lmin' W='wp14'
m='1-multn15'

.param multn14=agauss(0, 'abeta14/sqrt(2*lmin*wp14*1e+12)', 1)
.param dvth14=agauss(0, 'avth14/sqrt(2*lmin2*wp14*1e+12)', 1)
vmc14 Di-b vg14_shift dvth14
.param multn15=agauss(0, 'abeta15/sqrt(2*lmin*wp14*1e+12)', 1)
.param dvth15=agauss(0, 'avth15/sqrt(2*lmin2*wp14*1e+12)', 1)
vmc15 Di+b vg15_shift dvth15

mn16  bDi-b vg16_shift gnd gnd nmos L='lmin' W='wn16'
m='1-multn16'

mn17  Di+b vg17_shift gnd gnd nmos L='lmin' W='wn16'

mp18  bDi-b vg18_shift vdd vdd pmos L='lmin' W='wp18'
m='1-multn18'

mp19  Di+b vg19_shift vdd vdd pmos L='lmin' W='wp18'
m='1-multn19'

.param dvth0=0

.vmc0 Di-b bDi-b dvth0

.param multn16=agauss(0, 'abeta16/sqrt(2*lmin*wn16*1e+12)', 1)
.param dvth16=agauss(0, 'avth16/sqrt(2*lmin*wn16*1e+12)', 1)
vmc16 Di- vg16_shift dvth16
.param multn17=agauss(0, 'abeta17/sqrt(2*lmin*wn16*1e+12)', 1)
.param dvth17=agauss(0, 'avth17/sqrt(2*lmin*wn16*1e+12)', 1)
vmc17 Di+ vg17_shift dvth17
.param multn18=agauss(0, 'abeta18/sqrt(2*lmin*wp18*1e+12)', 1)
.param dvth18=agauss(0, 'avth18/sqrt(2*lmin*wp18*1e+12)', 1)
vmc18 Di- vg18_shift dvth18
.param multn19=agauss(0, 'abeta19/sqrt(2*lmin*wp18*1e+12)', 1)
.param dvth19=agauss(0, 'avth19/sqrt(2*lmin*wp18*1e+12)', 1)
vmc19 Di+ vg19_shift dvth19

.param wn16=0.6u
+ wp18=1.8u
+ wn6=0.8u
+ wp8=0.4u
+ wp10=1u
+ wn12=1.5u
+ wp14=0.2u

c1  out+ gnd cload1

c2  out- gnd cload2

.param cload1=agauss(7f, 0.01, 1)
+     cload2=7f

** Analysis setup **
.TEMP   25
.OPTIONS POST
.WIDTH OUT=80
.tran 10p 2n sweep monte=500

.END

******************************************************************************************