Low-Power CMOS Relaxation Oscillator Design with an On-Chip Circuit for Combined Temperature-Compensated Reference Voltage and Current Generation

A Thesis Presented

by

Yuchi Ni

to

The Department of Electrical and Computer Engineering

in partial fulfillment of the requirements for the degree of

Master of Science

in

Electrical Engineering

Northeastern University
Boston, Massachusetts

November, 2013
ABSTRACT

Low-power oscillators are essential components of battery-powered medical devices for which the battery life must be maximized, such as pacemakers, blood glucose meters and heart monitors. Energy-efficient oscillators are also needed for devices in radio-frequency identification (RFID) systems and wireless sensor networks. Consequently, the design of reliable low-power oscillators has been a major challenge in many emerging applications in which low-frequency clock signals are generated within single-chip systems.

A relaxation oscillator with integrated voltage and current reference generation circuitry is presented in this thesis for on-chip clock signal generation in low-power applications. Designed and simulated in 0.11µm CMOS technology, the oscillator provides a clock signal at a frequency of 20KHz with a temperature coefficient of 314ppm/°C over a range from -20°C to 80°C. The oscillator’s output signal frequency has a simulated standard deviation of 7.9% under the influence of device mismatches and process variations. An integrated voltage and current reference generator was developed to provide two reference voltages at 484.6mV and 663.5mV with simulated temperature coefficients of 7.5ppm/°C and 16ppm/°C over a range from -20°C to 80°C respectively, as well as a reference current of 26.84nA with a temperature coefficient of 166ppm/°C over the same temperature range. A prototype chip was fabricated in 0.11µm CMOS process technology with a 1.2V supply. Measurements showed that the oscillator has a power consumption of 4.2µW, a temperature coefficient of 675ppm/°C, and a phase noise of -105dBc/Hz at 10KHz offset.
Firstly, I would like to express my gratitude to my advisor, Prof. Marvin Onabajo, for his patient guidance and constructive suggestions. He not only showed me the art of analog IC design, but also taught me how to be professional. He has broadened my mind, helped me to develop my future career, and he will always be one of my role models. I also want to thank Prof. Yong-Bin Kim for providing access to the silicon area for the prototype chip fabrication in 0.11\(\mu\)m CMOS technology through his research sponsor Techwin Corp. My sincere appreciation goes to the members of the AMSIC research group and the HPVLSI group at Northeastern University for their help and discussions, especially: Chun-hsiang Chang, Hari Chauhan, Junpeng Feng, Seyed Alireza Zahrai, Jing Lu, Jing Yang, Yongsuk Choi, Inseok Jung, and Ho Joon Lee.

I would like to thank my aunt Yanli He, who let me live with her when I arrived in the United States for the first time. Her help and suggestions made my life in Boston much easier. I also want to thank my friends, namely He Qi, Wei Cai, Weifu Li, Wei Wei, Wei Li, Zijian Chen, Ke Chen, Linbin Chen, Chenye Yang and so on, for the happy memories at Northeastern University.

At last, my gratitude goes to my dear parents for their love and support. I could not have made it so far without their help and encouragement.
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1. INTRODUCTION

1.1. Application overview

The demand for low-power integrated circuits is continuing to increase in applications such as wireless sensor networks, energy harvesting, battery-operated medical devices (e.g., pacemakers [1]-[3] and blood glucose meters), as well as radio-frequency identification (RFID) systems [4]-[6]. Ideally, the batteries of these devices should last for years without being changed or recharged. Fig. 1 displays a generalized block diagram of an RFID transponder as an example [6]. Typical RFID systems consist of tags (transponders) and readers that are used for low-cost automated inventory management as well as tracking applications. The reader initiates the communication by transmitting an RF signal, and the tag containing the requested information responds by reflecting back a portion of the interrogating RF wave through backscatter modulation. A passive RFID tag is often a tiny device that operates without any internal power source and that only retrieves power from the induced energy picked up from the received RF signal in the range of microwatts. Thus, efficient use of power is a crucial design aspect.

Fig. 1. Simplified block diagram of an RFID transponder.

The clock generator in Fig. 1 provides the clock signals that the processor uses to perform command handling, coding and decoding operations. Table 1 summarizes the RFID frequency bands from [7], which
shows that the transmit/receive frequencies can vary from several kilohertz to gigahertz depending on the application.

Many RFID transponders are in standby mode most of the time, and are woken up at regular intervals for a short time to perform measurements or communication tasks with the help of clock signals from on-chip oscillators. Afterwards, the system is placed into a power-down mode with minimal power consumption to preserve the available battery capacity [8]. In this and the other similar applications mentioned previously, low-power consumption is one of the most important design considerations.

Table I. RFID frequency bands

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Range</th>
<th>Data Speed</th>
<th>Remarks</th>
<th>Regulation</th>
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<tr>
<td>&lt;135 KHz</td>
<td>10cm</td>
<td>Low</td>
<td>Identification and Tracking</td>
<td>Unregulated</td>
</tr>
<tr>
<td>13.56 MHz</td>
<td>1m</td>
<td>Low to moderate</td>
<td>Smart Cards</td>
<td>ISM Band Worldwide</td>
</tr>
<tr>
<td>433 MHz</td>
<td>1–100m</td>
<td>Moderate</td>
<td>Defense Applications</td>
<td>Short Range Devices</td>
</tr>
<tr>
<td>865-868 MHz</td>
<td>1–2m</td>
<td>Moderate to High</td>
<td>EAN, Various Standards</td>
<td>ISM band</td>
</tr>
<tr>
<td>(Europe) 902-928 MHz (North America)</td>
<td>1–2m</td>
<td>Moderate to High</td>
<td>EAN, Various Standards</td>
<td>ISM band</td>
</tr>
<tr>
<td>2450-5800 MHz</td>
<td>1–2m</td>
<td>High</td>
<td>802.11 WLAN, Bluetooth</td>
<td>ISM band</td>
</tr>
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Implantable and portable medical systems span a number of different target applications and are widely used in the therapy. Traditionally, bradycardia pacemakers and tachyarrhythmia defibrillators are the largest markets. Pacemakers are used to treat bradyarrhythmia (a heart rate that is too slow) by monitoring the heart’s rate (how fast it beats) and rhythm (the pattern in which it beats), and by providing electrical
stimulation when the heart does not beat properly [3]. A pacemaker system, as shown in Fig. 2, generally consists of two components: pacing leads and pacemaker device.

Fig. 2. Cardiac pacemaker system [3].

Inserted through a vein into the heart, pacing leads carry impulses from the pacemaker device to the heart, stimulating the heart to beat. They also carry information from the heart back to the device, which is used to assess the status of the patient’s heart.

Implantable devices such as pacemakers have traditionally used a non-rechargeable battery as the energy source for the system. With this approach, longevity becomes a desirable characteristic, minimizing the patient’s exposure to implantation surgery. The battery is typically made of lithium iodine, which gives a life span of up to 10-12 years.
The general block diagram of a pacemaker system is shown in Fig. 3, which is adapted from [3]. It includes a programmable logic device, an analog-to-digital (ADC) converter, memory, a pulse generator, and a power management subsystem. The clock generator provides clock signals for the memory, logic device, ADC involved in the signal detection, and the signal processing blocks. Utilizing ultra-low-power design techniques, a large number of analog and digital processing circuits are being integrated into modern pacemakers to provide new features and functions in the future. Nevertheless, low power consumption is by far the most important design requirement to ensure 10-12 years of reliable operation on a single battery.

1.2. Low-power low-frequency oscillators

Compared to RF transceiver systems for cellular communication, the frequency accuracy is usually not as critical in the abovementioned low-power applications. For example, an accuracy requirement of 15% is a target in a relatively strict RFID case [9]. However, several research works have been reported in this area due to the increasing demand for low-power oscillators.

A crystal oscillator, shown in Fig. 4, uses the mechanical resonance of a piezoelectric material to create an electrical signal with a very high precision. Crystal oscillators outperform other oscillators due to superior frequency stability with respect to variation of the power supply, temperature, and manufacturing
process. Recently, the feasibility of a low-power crystal oscillator implemented in nano-scale technology has been demonstrated in [10]. However, the use of a crystal oscillator is associated with tradeoffs because they are relatively large and expensive, eliminating them as viable candidates for many miniaturized implantable devices and low-cost devices. Moreover, it is desirable to integrate the oscillator into the system instead of using an off-chip crystal oscillator.

![Typical commercial crystal oscillator.](image)

**Fig. 4.** Typical commercial crystal oscillator.

A ring oscillator as shown in Fig. 5 is a type of oscillator composed of a number of inverters connected in a chain, where the output of the last stage is fed back to the input of the first stage. According to Barkhausen’s criteria, the loop should introduce a total phase shift of $360^\circ$ with a gain larger than unity in order to sustain an oscillation. Ring oscillators exhibit good performance when operated in the subthreshold region [11], but their frequency accuracy is strongly affected by process variations, bias current drift, and temperature changes.

![Diagram of a simple 3-inverter ring oscillator.](image)

**Fig. 5.** Diagram of a simple 3-inverter ring oscillator.
A relaxation oscillator is an oscillator based on the behavior of a physical system’s return to equilibrium after being disturbed. A dynamic system within the relaxation oscillator continuously dissipates its internal energy. Relaxation oscillators are often chosen when low-power operation is required with decent accuracy. They consume less power than crystal oscillators at the cost of higher clock jitter, but fortunately clock jitter is not a major concern in the low-power applications mentioned in the previous subsection. Another advantage of relaxation oscillators is that no off-chip components are needed. However, a major design challenge is to avoid susceptibility to temperature changes. Normally, a temperature coefficient of less than 1000ppm°C is required to achieve a frequency variation of less than 10% over the whole industrial temperature range.

Inductor/Capacitor (LC) oscillators are commonly used in radio frequency circuits because of their good phase noise characteristics and their implementation suitability at radio frequencies. The output frequency of LC oscillators is determined by a tuned resonant LC circuit. The oscillation frequency of a simple LC tank is given by

\[ f = \frac{1}{2\pi \sqrt{LC}}. \]  

(1)

From the above equation, one can observe that a large inductor is needed to obtain a low resonant frequency, which implies that a large chip area would be consumed for the target frequency range of less than 100KHz in this project. Furthermore, large on-chip inductors tend to have low quality factors, resulting in degraded phase noise performance.

<table>
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<tr>
<td>Type</td>
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</tr>
<tr>
<td>Typical Implementation</td>
</tr>
<tr>
<td>Frequency</td>
</tr>
<tr>
<td>Frequency Variation vs. Temperature</td>
</tr>
<tr>
<td>Current Consumption</td>
</tr>
<tr>
<td>Size</td>
</tr>
<tr>
<td>Start-up Time</td>
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</table>
Table II lists typical characteristics of different types of oscillators. For highly-integrated low-power devices, crystal oscillators are often avoided because of their high power consumption and printed-circuit board area requirement. From the view of power and area efficiency of on-chip implementations, relaxation oscillators and ring oscillators are comparable, but further comparison reveals that relaxation oscillators often outperform ring oscillators in low-frequency applications in terms of accuracy and area efficiency because low-frequency ring oscillators require a large number of stages. In consideration of the stringent power and area limitations of the target applications, a relaxation oscillator architecture was chosen to improve the state-of-the-art with this research effort.

1.3. Research overview and contribution

In this thesis, a relaxation oscillator with integrated voltage and current reference generation circuitry is presented for on-chip clock signal generation in low-power applications. A novel feature of the integrated voltage and current reference generator is that it has been developed to simultaneously provide two temperature-independent voltages and one temperature-independent current for the oscillator. Designed in standard 0.11μm CMOS technology, the oscillator provides a clock signal at the frequency of 20KHz with a simulated temperature coefficient of 314ppm/°C over a range from -20°C to 80°C. The oscillator’s output signal frequency has a simulated standard deviation of 7.9% under the influence of device mismatches and process variations. It operates with a supply voltage of 1.2V and has a simulated dynamic power consumption of 4.9µW at room temperature. A chip fabricated in Dongbu 0.11μm CMOS technology has a measured power consumption, temperature coefficient and phase noise of 4.2µW, 675ppm/°C and -105dBc/Hz at 10KHz offset, respectively.

A study of temperature variation influence on the performance of relaxation oscillator circuitry was conducted and is summarized in Chapter 2. Several temperature compensation techniques are discussed and evaluated with simulations. A novel method is proposed that can compensate the generated reference voltage and reference current simultaneously. Simulation results indicate that the proposed compensation
approach is robust to process variations and enables to achieve very low temperature coefficients, making it suitable for reliable low-power relaxation oscillators. The remainder of this thesis is organized as follows: in addition to describing the temperature compensation technique, Chapter 2 also focuses on the design issues for the comparator and switches in the relaxation oscillator. Chapter 3 contains discussions of simulation results and a description of chip layout considerations. The design of the printed circuit board for the prototype chip, measurement setup, and measurement results are discussed in Chapter 4. Finally, a summary and conclusions are provided in Chapter 5.

2. CIRCUIT DESIGN AND ANALYSIS

2.1. System-level overview

As justified in the previous chapter, a relaxation oscillator architecture was chosen for this application, which is displayed in Fig. 6. This oscillator contains a reference generator that provides currents $I_{\text{refP}} = I_{\text{refN}} = I_C$ that are used to charge and discharge capacitor $C_T$ [9].

![Relaxation oscillator block diagram.](image)

Two comparators compare the voltage across the capacitor with the threshold voltages $V_{\text{max}}$ and $V_{\text{min}}$, which are also generated by the proposed circuit described later in this chapter. The outputs of the two
comparators are applied to an S-R latch to drive the transmission gates. When the voltage across the capacitor rises above $V_{\text{max}}$, then the output of Comparator 2 will transition to high, $Q'$ becomes 1 and $Q_{\text{bar}}'$ becomes 0. Consequently, the transmission gate that connects to the current sink will turn on to discharge $C_T$. On the other hand, when the voltage across the capacitor falls below $V_{\text{min}}$, the output of the comparator 1 changes to high, $Q'$ becomes 0 and $Q_{\text{bar}}'$ becomes 1, and the capacitor will be charged. The frequency of the resulting oscillation can be expressed as [9]:

$$f = \frac{I_C}{2 C_T (V_{\text{max}} - V_{\text{min}})}.$$  (2)

From equation (2), we can conclude that a nano-scale current is a prerequisite condition for low-frequency oscillation in the kilohertz range. Another observation is that a temperature-independent oscillation signal requires temperature-compensated current and voltage references. Furthermore, the generation of a nano-scale current typically requires that some transistors are biased in the subthreshold region, which necessitates process variation-aware design [14]. Lastly, a load capacitor in the picofarad range should be adopted to create an oscillation frequency in kilohertz range.

### 2.2. Reference voltage generation

Analog and mixed-signal integrated systems extensively incorporate voltage and current reference circuits. These references should exhibit little dependence on temperature, process and supply voltage. For example, the bias current of a differential amplifier must be generated reliably because it affects the voltage gain, noise, and other critical parameters. In systems such as analog-to-digital converters and digital-to-analog converters, precise reference voltages or currents are typically required to quantize the input signals. In the discussed relaxation oscillator, the generation of temperature-insensitive reference voltages and currents is the prerequisite condition for a temperature-independent oscillation. The basic concept behind generating a temperature-independent reference is that if two quantities having opposite temperature coefficients are added with proper weighting, the result displays a zero temperature coefficient. For example, for two voltages $V_1$ and $V_2$ that change in opposite directions with temperature,
we can choose $\alpha_1$ and $\alpha_2$ so that $\alpha_1 \frac{\partial V_1}{\partial T} + \alpha_2 \frac{\partial V_2}{\partial T} = 0$, obtaining a reference voltage of $V_{\text{ref}} = \alpha_1 V_1 + \alpha_2 V_2$ that has a temperature coefficient of zero. Next, voltages that have positive and negative temperature coefficients will be examined.

### 2.2.1. Negative temperature coefficient voltage

The forward voltage of a diode and the base-emitter voltage of a bipolar transistor have a negative temperature coefficient, such that the voltage drop decreases as the temperature increases. The relationship between the collector current ($I_C$) and the base-emitter ($V_{BE}$) voltage of a bipolar transistor is [15]:

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right),$$

where $V_T = kT/q$, $k$ is the Boltzmann constant, and $q$ is the elementary electron charge. The saturation current $I_S$ is

$$I_S = bT^{4+m} \exp\left(-\frac{E_g}{kT}\right),$$

where $b$ denotes the proportionality factor and $m \approx -3/2$. With $V_{BE} = V_T \ln(I_C/I_S)$ from (3), the temperature coefficient for the base-emitter voltage can be calculated. Assuming that $I_C$ is held constant by design, we can obtain the following expression:

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T}.$$  (5)

From equation (4), we can derive

$$\frac{\partial I_S}{\partial T} = b (4 + m)T^{3+m} \exp\left(-\frac{E_g}{kT}\right) + bT^{4+m} \left(\exp\left(-\frac{E_g}{kT}\right)\right)\left(-\frac{E_g}{kT}\right).$$  (6)
Hence,

\[
\frac{V_T}{I_S} \frac{\partial I_S}{\partial T} = (4 + m) \frac{V_T}{T} + \frac{E_g}{kT^2} V_T .
\]  (7)

With the aid of (5) and (7) it can be shown that [15]:

\[
\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4 + m)V_T - E_g/ q}{T} .
\]  (8)

Equation (8) is the temperature coefficient of the base-emitter voltage at a given temperature. With \( V_{BE} = 750\text{mV} \) and \( T = 300\text{ºK} \) for instance, \( \partial V_{BE}/\partial T = -1.5\text{mV/ºK} \). It is quite interesting to notice that the temperature coefficient itself varies with temperature. If the base-emitter voltage is added to a voltage with a constant positive temperature coefficient, then an overall temperature coefficient of zero can only be achieved around a specific temperature.

2.2.2. Positive temperature coefficient voltage

It was noticed in the previous subsection that the difference between two bipolar transistors’ base-emitter voltage \( (V_{BE}) \) is directly proportional to the absolute temperature if two bipolar transistors operate at different current densities. For example, as shown in Fig. 7 (from [15]), if two identical transistors \( (I_{S1} = I_{S2}) \) are biased at collector currents of \( nI_0 \) and \( I_0 \) and their base currents are negligible, then

\[
\Delta V_{BE} = V_{BE1} - V_{BE1} \\
= V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}} .
\]  (9)
Based on equation (9), we can write

\[
\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln(n).
\]  

(10)

Equation (10) indicates that the $V_{BE}$ difference exhibits a positive temperature coefficient.

![Fig. 7. Generation of a proportional-to-absolute temperature voltage.](image)

2.2.3. Bandgap reference

Two voltages with opposite temperature coefficients have been identified in sections 2.2.1 and 2.2.2, making it possible to generate a reference voltage with a zero temperature coefficient through a combination. According to the analysis in Section 2.2, we can write $V_{\text{ref}} = \alpha_1 V_{BE} + \alpha_2 [V_T \cdot \ln(n)]$, where $V_T \cdot \ln(n)$ is the difference between the base-emitter voltages of the two bipolar transistors operating at different current densities as in equation (9). At room temperature $\partial V_{BE} / \partial T = -1.5\text{mV/}^\circ\text{K}$, while $\partial V_T / \partial T = +0.087\text{mV/}^\circ\text{K}$. Basically, $\alpha_1$ can be set to 1, which implies that $\alpha_2 \cdot \ln(n) / (0.087\text{mV/}^\circ\text{K}) = 1.5\text{mV/}^\circ\text{K}$ is required, and that $\alpha_2 \cdot \ln(n) = 17.2$. With these conditions, we obtain

\[
V_{\text{REF}} \approx V_{BE} + 17.2V_T.
\]

(11)

$V_{\text{ref}}$ is typically around 1.25V in CMOS technologies. The bandgap reference in Fig. 8 adds $V_{BE}$ to $17.2V_T$ as needed. Here, the base currents are assumed negligible. Transistor $Q_2$ consists of $n$ units of
transistors in parallel, and Q₁ is a unit transistor. Nodes X and Y are forced to be equal as a result of the operational amplifier feedback.

Fig. 8. A bandgap reference circuit (from [16]).

The reference voltage in Fig. 8 is generated at the output of the amplifier, which can be expressed as:

\[
V_{\text{out}} = V_{BE} + \frac{V_T \ln(n)}{R_3} \cdot (R_2 + R_3)
\]

\[
= V_{BE} + V_T \ln(n) \cdot (1 + \frac{R_2}{R_3})
\]

(12)

In order to achieve a zero temperature coefficient, the ratio of \((1+R_2/R_3)\ln(n)\) should be set to approximately 17.2. From equation (12), one can observe that the output voltage depends on the ratio of the resistors instead of their absolute values, which makes the temperature coefficient of this voltage robust to the temperature coefficient of the resistors and to process variations.

2.2.4. Implementation of a bandgap reference using a proportional-to-absolute temperature current

A proportional-to-absolute temperature (PTAT) current can be generated as shown in Fig. 9. The op-amp drives the voltages at its two inputs to the approximately same voltage, such that \(V_X = V_Y\). Hence, the
voltage difference between node Y and the emitter of $Q_2$ equals $V_T \ln(n)$, and the current in this branch is $V_T \ln(n)/R_1$. This current is copied by the current mirror to generate the PTAT current at the drain of $M_3$ that is equal to $m \cdot V_T \ln(n)/R_1$, where $m$ is the current mirror ($M_3, M_2$) ratio.

![Diagram](image_url)

Fig. 9. Generation of a bandgap reference voltage using a PTAT current [15].

The equation for the output voltage in Fig. 9 can be expressed as

$$V_{out} = V_{BE3} + \frac{V_T \ln(n)}{R_1} R_2,$$

(13)

where all the PMOS transistors are assumed to be identical. The size of $Q_3$ and the values of $R_1$ and $R_2$ are arbitrary as long as the sum of the two terms in equation (13) results in a zero temperature coefficient.

In summary, the bandgap reference is a highly reliable circuit with an output that is robust to temperature and process variations. Nevertheless, there are some severe drawbacks of this circuit, making it an inappropriate candidate for the application in this thesis. First, the bandgap reference voltage is typically around 1.25 V, which is relatively high for modern sub-micron CMOS technologies. Second, the power consumptions of conventional bandgap reference generators are usually in the microwatts range.
which is too high for ultra-low power systems. For the purpose of minimizing power, the resistances can be increased to the megaohm range, which reduces the currents. However, such high resistances would require large areas during on-chip implementations, which again would be unsuitable for the target application. Given the stringent silicon area, power consumption and supply voltage limits, an alternative reference voltage generation has been explored.

2.2.5. Voltage reference circuit consisting of subthreshold MOSFETs

One of the promising areas of research in analog circuit design is the development of ultra-low power circuits with transistors operating in the subthreshold region by biasing them with a gate-source voltage below the threshold voltage. For example, a voltage reference that can operate with sub-microwatt power dissipation and low temperature sensitivity has been reported in [17], which consists of subthreshold MOSFET devices. The basic principle is the generation of a voltage with a negative temperature coefficient and another voltage with positive temperature coefficient, which are summed up to produce an output voltage with a zero temperature coefficient.

Fig. 10. Ultra-low power voltage reference circuit from [17].
Illustrated in Fig. 10, the circuit from [17] consists of a current source subcircuit and a bias-voltage subcircuit. The current source subcircuit is a modified self-biased current generator in which the conventional resistor is replaced with a MOS resistor (M_R). The current source subcircuit generates a current \( I_p \), which is copied by the PMOS current mirrors (M_P) and driven into bias voltage subcircuit to produce a reference voltage \( V_{ref} \). All transistors are biased in the subthreshold region, except for the MOS resistor M_R that operates in the strong inversion, deep-triode region. The details of operation will be elaborated in the following analysis.

The subthreshold drain current \( I_D \) of a MOSFET transistor has an exponential dependence on the gate-source voltage \( V_{GS} \) and the drain-source voltage \( V_{DS} \):

\[
I_D = K I_0 \exp\left( \frac{V_{GS} - V_{TH}}{\eta T} \right) \times (1 - \exp\left( -\frac{V_{DS}}{V_T} \right))
\]

(14)

where

\[
I_0 = \mu C_{ox} (\eta - 1)V_T^2
\]

(15)

\( K \) is the aspect ratio (=W/L) of the transistor, \( \mu \) is the carrier mobility, \( C_{ox} \) is the gate-oxide capacitance, \( V_T (=kT/q) \) is the thermal voltage, \( k \) is the Boltzmann constant, \( T \) is the absolute temperature, \( q \) is the elementary charge, \( V_{TH} \) is the threshold voltage, \( \eta \) is the subthreshold factor [18]. For \( V_{DS} \geq 0.1 \) V, the current \( I_D \) is almost independent of \( V_{DS} \) and can be expressed as

\[
I_D = K I_0 \exp\left( \frac{V_{GS} - V_{TH}}{\eta T} \right)
\]

(16)

In the current source subcircuit of Fig. 10, \( V_{GS1} \) is equal to the sum of \( V_{GS2} \) and drain-source voltage of M_R:

\[
V_{GS1} = V_{GS2} + V_{DSR}
\]

(17)
Assuming that the currents in $M_1$ and $M_2$ are equal due to matched dimensions in both branches, equations (16) and (17) can be combined and rearranged to:

$$V_{DSR} = \eta V_T \ln \left( \frac{K_2}{K_1} \right), \quad (18)$$

where $K_i$ is the aspect ratio ($W/L$) of transistor $M_i$, and $K_2$ is the aspect ratio of transistor $M_2$.

The MOS resistor $M_R$ is biased in strong inversion, deep triode region. Therefore, its resistance can be expressed as

$$R_{MR} = \frac{1}{K_{R1}\mu C_{ox} (V_{ref} - V_{TH})}, \quad (19)$$

where $K_{R1}$ is the aspect ratio of transistor $M_R$. From (18) and (19), it follows that

$$I_p = \frac{V_{DSR}}{R_{MR}} = K_{R1}\mu C_{ox} (V_{ref} - V_{TH}) \eta V_T \ln \left( \frac{K_2}{K_1} \right). \quad (20)$$

In the bias voltage subcircuit of Fig. 10, the gate-source voltages ($V_{GS3}$ through $V_{GS7}$) of the transistors form a closed path, and the currents in $M_4$ and $M_6$ are $3I_p$ and $2I_p$ respectively. Therefore, the output voltage $V_{ref}$ is

$$V_{ref} = V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} = V_{GS4} + \eta V_T \ln \left( \frac{2K_3}{K_5 K_4} \right) + \eta V_T \ln \left( \frac{2K_3}{K_5 K_4} \right). \quad (21)$$
Equation (21) reveals that $V_{ref}$ is a sum of the threshold voltage and several scaled thermal voltages. Since the threshold voltage has a negative temperature coefficient and the thermal voltage has a positive temperature coefficient, the reference voltage can exhibit a zero temperature coefficient if the thermal voltages are properly scaled. More specifically, the temperature dependence of the threshold can be expressed as [17]

$$V_{TH} = V_{TH 0} + \kappa T,$$  \hspace{1cm} (22)

where $V_{TH0}$ is the threshold voltage at 0º K, and $\kappa$ is the temperature coefficient (TC) of the $V_{TH}$. Using equations (20) and (22), the output voltage $V_{ref}$ in (21) can be rewritten as

$$V_{ref} = V_{TH 0} + \kappa T + \eta V_T \ln\left\{ \frac{6 \eta k_B K_1 K_3 K_5 (V_{ref} - V_{TH})}{K_4 K_6 K_7 (\eta - 1)V_T} \ln\left( \frac{K_2}{K_1} \right) \right\},$$  \hspace{1cm} (23)

and the TC of $V_{ref}$ can be expressed as

$$\frac{\partial V_{ref}}{\partial T} = -\kappa + \frac{\eta k_B}{q} \ln\left\{ \frac{6 \eta k_B K_1 K_3 K_5 (V_{ref} - V_{TH})}{K_4 K_6 K_7 (\eta - 1)V_T} \ln\left( \frac{K_2}{K_1} \right) \right\}$$

$$+ \eta V_T \left\{ \frac{1}{V_{ref} - V_{TH}} \left( \frac{\partial V_{ref}}{\partial T} + \kappa \right) - \frac{1}{T} \right\}.$$  \hspace{1cm} (24)

Assuming that $V_{ref} - V_{TH0} \ll \kappa T$ and that $\eta T \ll \kappa T$, the TC of $V_{ref}$ can be simplified to:

$$\frac{\partial V_{ref}}{\partial T} = -\kappa + \frac{\eta k_B}{q} \ln\left\{ \frac{6 q \eta \kappa}{k_B (\eta - 1)} \frac{K_1 K_3 K_5}{K_4 K_6 K_7} \ln\left( \frac{K_2}{K_1} \right) \right\}.$$  \hspace{1cm} (25)

A zero TC can be achieved by satisfying the following condition:
\[ -\kappa + \frac{\eta k_B}{q} \ln \left\{ \frac{6q \eta \kappa}{k_B(\eta - 1)} \frac{K_{K1}K_4K_5}{K_1^2K_6K_7} \ln \left( \frac{K_2}{K_1} \right) \right\} = 0 \]  \hspace{1cm} (26)

If the transistors are properly ratioed according to equation (26), a zero TC reference voltage can be generated using the circuit in Fig. 10. Based on the above equations, we can find that under the assumed conditions:

\[ V_{\text{ref}} = V_{\text{TH}0} \cdot \]  \hspace{1cm} (27)

### 2.3. Reference current generation

Analog integrated systems incorporate current references extensively. Reference current generators are widely used for amplifiers, analog-to-digital converters, digital-to-analog converters, and oscillators for example. In commercial products, the bias currents for these blocks are usually copied with scaling from an on-chip reference current, and then distributed to various circuits on the chip. High-performance analog systems have to rely on precise and highly reliable reference currents and voltages, which have crucial impacts on the power consumption, supply rejection ratio and temperature dependence of the whole system.

#### 2.3.1. Temperature-independent current generation

Fig. 11 shows a current reference circuit with subthreshold CMOS devices [20]. This circuit consists of a bias-voltage subcircuit and a current source subcircuit. The bias-voltage circuit is a self-biasing circuit that uses a MOS resistor (M3) instead of a passive resistor. The generated bias current \( I_B \) is steered into a diode-connected transistor (M4) and generates a bias voltage \( V_B \) for the current source subcircuit. Voltage \( V_B \) is used to bias the current source subcircuit that generates the reference current \( I_{\text{out}} \) that is independent of the temperature and supply voltage. All transistors are operated in the subthreshold region, except for M3 and M4.
Fig. 11. Current reference circuit with subthreshold CMOS devices.

In the current source subcircuit of Fig. 11, $V_{GS1}$ is equal to the sum of $V_{GS2}$ and drain-source voltage of $M_3$, leading to:

$$V_{GS1} = V_{GS2} + V_{DS3}.$$  \hspace{1cm} (28)

Assuming that the currents in $M_1$ and $M_2$ are equal, equation (28) can be rearranged with the aid of (16) to obtain:

$$V_{DS3} = \eta V_T \ln \left( \frac{K_2}{K_1} \right).$$  \hspace{1cm} (29)
where the $K_1$ and $K_2$ are the aspect ratios (= W/L) of $M_1$ and $M_2$. Since the MOS resistor $M_3$ is biased in the strong inversion, deep triode region; its resistance is given by

$$R_{M3} = \frac{1}{K_3\mu C_{ox}(V_B - V_{TH})}.$$  \hspace{1cm} (30)

The diode-connected transistor $M_4$ operates in the strong inversion, saturation region. Thus, its drain current $I_B$ can be expressed as

$$I_B = \frac{K_4\mu C_{ox}}{2}(V_B - V_{TH4})^2.$$  \hspace{1cm} (31)

Since the bias current $I_B$ of $M_3$ is equal to that of $M_4$, $V_B$ becomes

$$V_B = V_{TH4} + \frac{2K_3}{K_4}\eta V_T \ln\left(\frac{K_2}{K_1}\right).$$  \hspace{1cm} (32)

The current through $M_5$ is mirrored to obtain the output current $I_{out}$. This current can be expressed as

$$I_{out} = K_5I_0 \exp\left(\frac{V_B - V_P - V_{TH5}}{\eta V_T}\right).$$  \hspace{1cm} (33)

where $V_P$ is the source voltage of $M_5$:

$$V_P = V_{GS7} - V_{GS6} = \eta V_T \ln\left(\frac{2K_6}{K_7}\right) - \delta V_{TH76}.$$  \hspace{1cm} (34)

$\delta V_{TH76}$ is the difference between the threshold voltages of $M_7$ and $M_6$. In order to bias transistor $M_5$ in the subthreshold region, the voltage $V_P$ has to be set to a large value by adjusting the sizes of $M_6$ and $M_7$. By combining equations (32) to (34), the equation for the output current can be written as
\[ I_{out} = I_0 \exp\left( \frac{\delta V_{TH}}{\eta V_T} \right) \frac{K_5}{2 K_6} \left( \frac{K_2}{K_4} \right)^{\frac{2 K_3}{K_4}}. \]  

where \( \delta V_{TH} = V_{TH7} + V_{TH4} - V_{TH6} - V_{TH5} \), of which the value depends on the transistor dimensions. The temperature dependence of the threshold voltage and the mobility can be expressed as

\[
V_{TH} = V_{TH0} - \kappa T
\]

\[
\mu(T) = \mu(0)(T / T_0)^{-m},
\]

where the \( \mu(0) \) is the carrier mobility at room temperature \( T_0 \), \( m \) is the mobility temperature exponent, \( V_{TH0} \) is the threshold voltage at 0K, and \( \kappa \) is the TC of \( V_{TH} \). By taking the derivative with respect to temperature, the TC of the output current is derived as follows in [20]:

\[
TC = \frac{1}{I_{out}} \frac{dI_{out}}{dT} = \frac{1}{\mu} \frac{d\mu}{dT} + \frac{1}{V_T^2} \frac{dV_T}{dT} + \frac{1}{\exp\left( \frac{\delta V_{TH0}}{\eta V_T} \right)} \frac{d}{dT} \exp\left( \frac{\delta V_{TH0}}{\eta V_T} \right).
\]

\[
= 2 - m - \frac{\delta V_{TH0}}{\eta V_T}.
\]

where the \( \delta V_{TH0} = V_{TH07} + V_{TH04} - V_{TH06} - V_{TH05} \) at 0 K. Therefore, the zero TC condition for the output current is

\[
2 - m - \frac{\delta V_{TH0}}{\eta V_T} = 0.
\]

In summary, this nano-ampere reference current generating technique is feasible for low-power applications, but it has a drawback for the target application in this thesis. It can be observed from
equation (35) that the absolute value of the reference current is exponentially related to the threshold voltage. Typically, the threshold voltage varies up to 20% in different process corner situations, which would cause a large deviation of the reference current. In other words, the reference current generator described above is not process insensitive enough.

![Current reference circuit using subthreshold MOS resistor ladder.](image)

Fig. 12. Current reference circuit using subthreshold MOS resistor ladder.

Shown in Fig. 12 is the nano-ampere current reference circuit from [21], which uses a subthreshold MOS resistor ladder. It consists of a bias-voltage section, a current source section, an offset voltage generation block, and a start-up circuit (not shown). All transistors (except $M_R$) are biased in the subthreshold region, and transistors with the same name ($M_P$) have the same dimensions. The MOS resistor ($M_R$) operates in strong-inversion and is biased in the deep triode region. This has the advantage that the output current is more robust to process variations and mismatches than the design in [20].
The current $I_{\text{ref}}$ in Fig. 12 is determined by the characteristics of the strongly-inverted MOS resistor $M_R$ biased in the deep triode region. When drain-source voltage $V_{DSR}$ is sufficiently small, the current is given by

$$I_{\text{ref}} = \mu_n C_{ox} K (V_{gs} - V_{th}) V_{DSR},$$

(39)

where $C_{ox}$ is the gate-oxide capacitance, $V_{th} (= V_{TH0} - \kappa T)$ is the threshold voltage, $V_{TH0}$ is the threshold voltage at 0 Kelvin, $\kappa$ is the temperature coefficient of the transistors’ threshold voltage, $K$ is the aspect ratio (W/L) of $M_R$, and $\mu_n$ is the carrier mobility that can be modeled with a temperature dependence of

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{-m} ;$$

(40)

where $\mu_0$ is the mobility at room temperature $T_0$, and $m$ is the mobility temperature exponent. Assuming that $V_{DSR}$ has an offset voltage ($\beta$) that is generated by an offset generation block, the temperature dependence of $V_{DSR}$ can be expressed as:

$$V_{DSR} = \alpha T + \beta ,$$

(41)

where $\alpha$ is the temperature coefficient of $V_{DSR}$. From equations (39)-(41), the temperature coefficient $T_{C_1}$ of the reference current $I_{\text{ref}}$ was derived in [21]:

$$T_{C_1} = \frac{1}{\mu} \frac{d\mu}{dT} + \frac{1}{V_{GS} - V_{TH}} \frac{d(V_{GS} - V_{TH})}{dT} + \frac{1}{V_{DSR}} \frac{dV_{DSR}}{dT}$$

$$= \frac{-m}{T} + \frac{1}{T} + \frac{\alpha}{\alpha T + \beta}$$

$$= \frac{l - m}{T} + \frac{1}{T + \frac{\beta}{\alpha}} .$$

(42)
In standard CMOS technology, parameter $m$ is approximately 1.5. Hence, $TC_1$ can be forced to 0 at room temperature by setting the $\beta/\alpha$ ratio to an appropriate value. Without an offset voltage ($\beta = 0$), $TC_1$ is always positive, but $TC_1$ can be set to 0 at 300K when $\beta/\alpha = 300$.

Fig. 13. Subthreshold MOS resistor ladder consisting of $N$ MOSFETs.

Fig. 13 shows the offset voltage generation circuit reported in [21], which consists of several MOSFETs connected in series. All the transistors are operating in the subthreshold linear region except the diode-connected transistor $M_0$ which operates in the subthreshold saturation region. Offset voltages can be obtained from the voltages at each tap of the ladder. To simplify the analysis, the number of the transistors is reduced to three as shown in Fig. 14.
Fig. 14. Subthreshold MOS resistor ladder consisting of 3×MOSFETs.

$M_0$ in Fig. 14 operates in the subthreshold linear region, and $M_1$ and $M_2$ operate in the subthreshold saturation region. The currents through the transistors are

$$I_0 = K_0 I_0 \exp\left( \frac{V_G - V_{D1} - V_{TH}}{\eta V_T} \right), \quad (43)$$

$$I_1 = K I_0 \exp\left( \frac{V_G - V_{D2} - V_{TH}}{\eta V_T} \right) \left( 1 - \exp\left( - \frac{V_{D1} - V_{D2}}{V_T} \right) \right), \quad (44)$$

$$I_2 = K I_0 \exp\left( \frac{V_G - V_{TH}}{\eta V_T} \right) \left( 1 - \exp\left( - \frac{V_{D2}}{V_T} \right) \right). \quad (45)$$

The internal voltage $V_{D2}$ can be expressed as

$$V_{D2} = \frac{\eta^2 K I_0 V_T I}{(\eta K I_0 + I)^2} \left( 1 + \ln\left( \frac{KI_0}{I} \right) \right). \quad (46)$$

$V_{D2}$ can be interpreted as a linear function with respect to the temperature, and equation (46) can be simplified to [21]

$$V_{D2} = \gamma T + \beta. \quad (47)$$

The temperature coefficient and the offset voltage in the above equation can be controlled by setting appropriate number of the transistors and the tap point in the resistor ladder.
Fig. 15. Nano-ampere current reference proposed in [21].

Fig. 15 shows the schematic of the practical nano-ampere current reference from [21], where the internal voltage $V_{SR}$ can be expressed as

$$V_{SR} = \gamma T + \beta .$$

(48)

The drain-source voltage of $M_R$ is

$$V_{DSR} = V_{SR} + V_{GS1} - V_{GS2} = V_{SR} + \eta V_T \ln \left( \frac{K_2}{K_1} \right),$$

(49)

$$= \gamma T + \beta + \eta V_T \ln \left( \frac{K_2}{K_1} \right),$$

$$= \alpha T + \beta$$

where:

$$\alpha = \gamma + \eta V_T \ln \left( \frac{K_2}{K_1} \right).$$

(50)

$K$ is the aspect ratio (=W/L) of a transistor, $\mu$ is the carrier mobility, $C_{OX}$ is the gate-oxide capacitance, $V_T$ (=kT/q) is the thermal voltage, $k$ is the Boltzmann constant, $T$ is the absolute temperature, $q$ is the elementary charge, $V_{TH}$ is the threshold voltage, and $\eta$ is the subthreshold factor [18]. Based on the above
equations, the temperature coefficient of the reference current can be set to zero around room temperature by adjusting $\gamma$ and $\beta$ with the taping point and the aspect ratios of the transistors in the ladder.

Table III. MOS ladder circuit characteristics [21]

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<th>$\beta$ (mV)</th>
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</tr>
<tr>
<td>11</td>
<td>7</td>
<td>93.3</td>
<td>6.28</td>
</tr>
</tbody>
</table>

Table III summarizes the characteristics of the internal voltages with various sets of transistors in the configuration. The results show that we can control $\gamma$ and $\beta$ by deciding on the number of transistors and picking the appropriate tap point. Unfortunately, the temperature compensation for the current ($I_{\text{ref}}$) in Fig. 15 and the voltage ($V_{\text{ref}}$) in Fig. 10 are independent of each other. The proposed method described in the next subsection leads to a circuit that simultaneously generates a reference current and voltages that are temperature-compensated.

2.3.2. Proposed temperature-independent current and voltage reference

![Proposed reference generation circuit](image)

Fig. 16. Proposed reference generation circuit.
Fig. 16 displays the proposed reference generation circuit, which utilizes the current generation
method described in [21] to produce a temperature-compensated reference current $I_{ref}$. This reference
current is copied and forced to flow into the diode-connected transistor $M_8$ to generate the reference
voltage $V_{min}$. By design, $I_{ref}$ has a value that is sufficiently small to ensure that $M_8$ is operating in the
subthreshold region, resulting in a subthreshold drain-source current equal to:

$$I_{M_8} = K_8 I_0 e^{\frac{V_{gs_8} - V_{th}}{\eta V_T}},$$

where $\eta$ is the subthreshold slope factor, $I_0 = \mu_n C_{ox} (\eta - 1)(V_T)^2$, $V_T = k_BT/q$ is the thermal voltage, and the
equation implies that the drain-source voltage is larger than 0.1 V [17]. After equating (39) and (51), the
expression for $V_{gs8}$ can be obtained, which is equal to the reference voltage:

$$V_{min} = V_{gs_8} = \eta V_T \ln \left(\frac{\mu_n C_{ox} K_R (V_{gs_8} - V_{th})}{\mu_n C_{ox} K_8 (\eta - 1) V_T^2}\right) + V_{th}.$$

Thus, the temperature coefficient of $V_{min}$ is:

$$TC_{REF} = \frac{\partial V_{min}}{\partial T} = \frac{\eta k \ln(A)}{q} + \frac{\eta k^3 (B + C - D) K_8 (\eta - 1)}{q^3 K_R (V_{gs} - V_{TH_0} + \kappa T)(\alpha T + \beta)},$$

where:

$$A = \frac{K_R (V_{gs} - V_{TH_0} + \kappa T)(\alpha T + \beta) q^2}{K_8 (\eta - 1) k^2 T^2},$$

$$B = \frac{K_R \kappa (\alpha T + \beta) q^2}{K_8 (\eta - 1) k^2 T^2},$$

$$C = \frac{K_R (V_{gs} - V_{TH_0} + \kappa T) \alpha q^2}{K_8 (\eta - 1) k^2 T^2}.$$
The temperature coefficient of $V_{\text{min}}$ can be compensated around room temperature by selecting the appropriate W/L ratio for $M_8$. Due to the complexity of the equation, the proper W/L ratio was chosen with a sweep during simulations. Notice that equation (52) still has temperature dependence, but this dependence is reduced significantly due to the partial cancellation of the terms. Furthermore, the value of $V_{\text{min}}$ is constrained by the requirements to achieve a near-zero temperature coefficient with the given design parameters and process technology based on equation (52). On the hand, the value of $V_{\text{max}}$ in Fig. 16 is generated with a ratioed resistor ladder, such that a different value of $V_{\text{max}}$ can be generated by adopting a different resistance ratio. In this design, the value of $V_{\text{max}}$ was selected based on the common-mode input range of the comparator and the desired oscillation frequency according to equation (2).

Fig. 16 also shows the output stage configuration with which we can generate the required reference voltage and reference current for the oscillator. The output $I_{\text{ref}} = 26.84\text{nA}$ is copied by a 1:4 current mirror (transistors $M_9 - M_{12}$), such that the final output currents are: $I_{\text{refP}} = I_{\text{refN}} = 118\text{nA}$. The two reference voltages $V_{\text{min}}$ and $V_{\text{max}}$ are 484.6mV and 663.5mV at room temperature, where $V_{\text{max}}$ is generated from a ladder with high-resistance polysilicon resistors. In order to minimize the effects of process variations, the resistor ladder is composed of 30 segments of 25KΩ high-resistance polysilicon resistors, and a common-centroid layout technique was used.

2.4. Comparator design

The relaxation oscillator architecture in Fig. 6 contains two comparators. In general, a comparator is defined as a device that has a binary output whose value is based on the comparison of two analog inputs. Basically, the comparator is a 1-bit ADC with the ideal transfer function shown in Fig. 17, where the output is equal to $V_{\text{OH}}$ when $V_{\text{inP}} - V_{\text{inN}} > 0$ and equal to $V_{\text{OL}}$ when $V_{\text{inP}} - V_{\text{inN}} < 0$. An ideal comparator has infinite gain, zero offset voltage and zero root-mean-square (RMS) noise.

\[
D = \frac{2 K_r (V_{\text{gs}} - V_{\text{TH}0} + \kappa T)(\alpha T + \beta)q^2}{K_s (\eta - 1) k^2 T^3}.
\]
In a practical situation, the comparator has a finite gain and is affected by the non-zero offset and RMS noise, for which the impact on the relative transfer function is visualized in Fig. 18 with exaggeration. The non-ideal gain can be defined as

\[ A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}, \]  

(57)

where \( V_{IH} - V_{IL} \) represents the input voltage difference that is required to saturate the comparator output at its upper \( V_{OH} \) and lower limit \( V_{OL} \). Hence, \( V_{IH} - V_{IL} \) indicates the resolution of the comparator.

Another non-ideality is the input-referred offset voltage, labeled \( V_{OS} \) in Fig. 18, which could be positive or negative. This offset voltage varies randomly from chip to chip due to mismatches caused by fabrication process variations. Comparator offset is a concern for the relaxation oscillator design in Fig. 6.
because the offset voltage directly impacts the oscillation frequency determined by equation (2). For instance, assuming that \( V_{\text{max}} - V_{\text{min}} = 200\text{mV} \) and an input-referred offset of \( \pm 10\text{mV} \), the variation of the frequency would be 10%.

### 2.4.1. Open-loop comparator

The open-loop comparator in Fig. 19 [22] is a single-stage amplifier without compensation to obtain a fast response time. Stability is not a concern because the amplifier is used without feedback from its output to its input. Nevertheless, the transistor dimensions should be carefully selected to minimize the effect of parasitic capacitances in order to minimize the response time.

![Open-loop comparator](image)

**Fig. 19. Open-loop comparator.**

The amplifier in Fig. 19 was designed for the application in the relaxation oscillator of Fig. 6. Transistors \( M_1 \) and \( M_2 \) in Fig. 19 have the same dimensions, and equal-sized transistors \( M_3 \) and \( M_4 \) form a 1:1 current mirror. The amplifier’s gain can be expressed as

\[
A_v = g_{m1} \left( \frac{r_{o2} r_{o4}}{r_{o2} + r_{o4}} \right),
\]

(58)

where the \( g_{\text{mX}} \) and \( r_{oX} \) are the transconductance and output resistance of the corresponding transistor \( M_X \).
The comparator has one dominant pole frequency \((\omega_p)\) of interest, which is created at the output. This pole in the frequency response can be approximated as

\[
\omega_p = \frac{1}{C_1 \left( \frac{r_{o2} r_{o4}}{r_{o2} + r_{o4}} \right)}, \quad (59)
\]

\[
r_{eX} \approx \frac{1}{\lambda I_{dX}}; \quad (60)
\]

where the \(C_1\) represent the sum of the capacitances connected to nodes \(V_p\) in Fig. 19, and \(I_{dX}\) is the drain-source current of transistor \(M_X\). The frequency response of the comparator can be estimated as

\[
A(s) = \frac{A_v}{1 + \frac{s}{\omega_p}}, \quad (61)
\]

From the above equations, it can be observed that the bandwidth of the comparator is strongly affected by the parasitic capacitances and drain-source resistances, as well as the transconductance that determines the voltage gain. Since a high transconductance value requires a large bias current, there is a trade-off between power consumption and speed. However, the oscillator design presented in this thesis is intended for target frequencies below 100KHz, allowing to design with low power consumption by sacrificing speed. The components dimensions used in the open-loop comparator design (Fig. 19) are listed in Table IV.

**Table IV. Dimensions of the devices in the comparator**

<table>
<thead>
<tr>
<th>Component Name (in Fig. 19)</th>
<th>Dimensions [(width/length)×segments] or Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(M_1)</td>
<td>(800nm / 1µm) \times 2</td>
</tr>
<tr>
<td>(M_2)</td>
<td>(800nm / 1µm) \times 2</td>
</tr>
<tr>
<td>(M_3)</td>
<td>(500nm / 4.5µm) \times 2</td>
</tr>
<tr>
<td>(M_4)</td>
<td>(500nm / 4.5µm) \times 2</td>
</tr>
<tr>
<td>(M_5)</td>
<td>(1.6µm / 1µm) \times 2</td>
</tr>
<tr>
<td>(C_1)</td>
<td>200fF</td>
</tr>
</tbody>
</table>
2.5. Switch design

Two conventional transmission gates are used to control the charging and discharging the capacitor $C_T$ in Fig. 6. In comparison to employing a single transistor for each switch, the use of transmission gates has the benefit that the on-resistance is lower and less dependent on the voltages on the terminals connected to $C_T$ and the reference current source. The additional parasitic capacitances from the second transistor are not critical in this low-frequency application.

2.6. SR latch design

A latch is a circuit that has two stable states and can be used to store state information. The relaxation oscillator in Fig. 6 uses a basic SR latch, where “S” and “R” stand for Set and Reset. Such a latch can be constructed from a pair of cross-coupled NOR logic gates as shown in Fig. 20, where the stored bit is present at the output marked Q.

![SR latch diagram](image)

Fig. 20. A SR latch constructed from a pair of cross-coupled NOR gates.
When the S and R inputs in Fig. 20 are both low, the feedback keeps the Q and Q\text{bar} outputs in a constant state, where Q\text{bar} is the complement of Q. If S (Set) is pulsed high while R (Reset) is held low, then the Q output is forced high, and stays high when S returns to low. Similarly, if R is pulsed high while S is held low, then the Q output is forced low, and stays low when R returns to low. The Q and Q\text{bar} outputs are supposed to be in opposite states. When both the S and R inputs are equal to 1, then both Q and Q\text{bar} become 0. For this reason, having both S and R equal to 1 is considered an invalid or illegal state for the SR latch. Otherwise, applying inputs of S = 1 and R = 0 "sets" the latch such that Q = 1 and Q\text{bar} = 0. Conversely, applying R = 1 and S = 0 "resets" the latch in the opposite state (Q = 0, Q\text{bar} = 1). When S and R are both equal to 0, the latch's outputs "latch" into their prior states. The truth table that summarizes the SR latch operation is provided in Table V. In this application, the sizes of PMOS and NMOS transistors
should be properly scaled to keep the trip point of the latch equal to $V_{DD}/2$. Fig. 21 shows the schematic of the SR latch designed for the relaxation oscillator, and the corresponding transistor dimensions are listed in Table VI.

Table V. Truth table of the SR latch

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q_{\text{bar}}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Latch</td>
<td>Latch</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Invalid</td>
<td>Invalid</td>
</tr>
</tbody>
</table>

Table VI. Dimensions of the devices in the SR latch

<table>
<thead>
<tr>
<th>Component Name (in Fig. 21)</th>
<th>Dimensions [(width/length)×segments] or Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>(500nm / 500nm) × 2</td>
</tr>
<tr>
<td>$M_2$</td>
<td>(500nm / 500nm) × 2</td>
</tr>
<tr>
<td>$M_3$</td>
<td>(2.1\mu m / 500nm) × 2</td>
</tr>
<tr>
<td>$M_4$</td>
<td>(2.1\mu m / 500nm) × 2</td>
</tr>
<tr>
<td>$M_5$</td>
<td>(500nm / 500nm) × 2</td>
</tr>
<tr>
<td>$M_6$</td>
<td>(500nm / 500nm) × 2</td>
</tr>
<tr>
<td>$M_7$</td>
<td>(2.1\mu m / 500nm) × 2</td>
</tr>
<tr>
<td>$M_8$</td>
<td>(2.1\mu m / 500nm) × 2</td>
</tr>
</tbody>
</table>
3. SIMULATION RESULTS

3.1. Reference generator simulation results

The performance of the design in Dongbu 0.11µm CMOS technology was assessed with Cadence Spectre simulations. The relaxation oscillator in Fig. 6 operates with a supply voltage of 1.2V, and consumes a total power of 4.9µW. Table VII lists the most relevant dimensions and values of components. It can be observed from the table that large dimensions and multipliers are selected to allow the use of the common-centroid layout technique to make the performance more robust to process variations and mismatches.

Fig. 22 shows the reference current as a function of temperature. From the figure it can be observed that the current varies very little around the temperature compensation point of 25ºC. The temperature coefficient is 166ppm/ºC over a range from -20ºC to 80ºC. Fig. 23 displays the temperature dependence of the reference voltage $V_{\text{max}}$. The reference voltage is 663.5mV at room temperature and has a temperature coefficient of 7.5ppm/ºC over a range from -20ºC to 80ºC. Fig. 24 reveals how reference voltage $V_{\text{min}}$ varies with temperature. The generated reference voltage is 484.6mV at room temperature with a temperature coefficient of 16ppm/ºC over the -20ºC to 80ºC range.
Table VII. Design parameters of proposed reference current/voltage generator and the relaxation oscillator (0.11µm CMOS, 1.2V supply)

<table>
<thead>
<tr>
<th>Component Name (in Fig. 6 and Fig. 16)</th>
<th>Dimensions [ (width/length)×segments ] or Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>M₁</td>
<td>(60µm / 3µm) × 1</td>
</tr>
<tr>
<td>M₂</td>
<td>(54µm / 3µm) × 1</td>
</tr>
<tr>
<td>M₃</td>
<td>(24µm / 3µm) × 2</td>
</tr>
<tr>
<td>M₄</td>
<td>(4.5µm / 3µm) × 2</td>
</tr>
<tr>
<td>M₅</td>
<td>(24µm / 3µm) × 2</td>
</tr>
<tr>
<td>M₆</td>
<td>(4.5µm / 3µm) × 2</td>
</tr>
<tr>
<td>M₇</td>
<td>(4.5µm / 3µm) × 2</td>
</tr>
<tr>
<td>M₈</td>
<td>(1µm /9µm) × 1</td>
</tr>
<tr>
<td>M₉</td>
<td>(6µm / 3µm)×2</td>
</tr>
<tr>
<td>M₁₀</td>
<td>(6µm / 3µm) × 2</td>
</tr>
<tr>
<td>M₁₁</td>
<td>(6µm / 3µm)×8</td>
</tr>
<tr>
<td>M₁₂</td>
<td>(6µm / 3µm) × 8</td>
</tr>
<tr>
<td>M₁₃</td>
<td>(6µm / 3µm) × 8</td>
</tr>
<tr>
<td>M₁₄</td>
<td>(6µm / 3µm) × 8</td>
</tr>
<tr>
<td>M₉⁺</td>
<td>(6µm / 3µm) × 2</td>
</tr>
<tr>
<td>M₉⁻</td>
<td>(1.5µm / 1µm)×1</td>
</tr>
<tr>
<td>M₉⁺</td>
<td>(1µm / 48µm) × 4</td>
</tr>
<tr>
<td>R₁</td>
<td>250KΩ [1µm / 10µm] × 10</td>
</tr>
<tr>
<td>R₂</td>
<td>500KΩ [1µm / 10µm] × 20</td>
</tr>
<tr>
<td>R₃</td>
<td>250KΩ [1µm / 10µm] × 10</td>
</tr>
<tr>
<td>Cₜ</td>
<td>20pF</td>
</tr>
</tbody>
</table>
Fig. 22. Simulated reference current ($I_{\text{ref}}$ in Fig. 16) vs. temperature.

Fig. 23. Simulated reference voltage $V_{\text{max}}$ vs. temperature.
Fig. 24. Simulated reference voltage $V_{\text{min}}$ vs. temperature.

Fig. 25 and Fig. 26 visualize the distributions of $V_{\text{min}}$ and $V_{\text{max}}$ obtained from 100 Monte Carlo simulations with foundry-supplied device models. The standard deviations ($\sigma$) are 1.023mV and 0.767mV, resulting in very low variations as evident after normalization with the mean values ($\mu$): $\sigma/\mu$ is 0.2% for $V_{\text{min}}$ and 0.11% for $V_{\text{max}}$. Fig. 27, Fig. 28 and Fig. 29 display the distributions of $I_{\text{ref}}$ obtained from 100 Monte Carlo simulations at 27°C, -20°C, and 80°C, respectively. In all cases, the standard deviation of $I_{\text{ref}}$ is less than 6% of its mean value. The Monte Carlo simulation results suggest that the reference current is robust to device mismatches, which leads to reliable currents $I_{\text{refP}}$ and $I_{\text{refN}}$ because they are copied from $I_{\text{ref}}$ using current mirrors with a multiplication factor of 4.
Fig. 25. Histogram of $V_{\text{min}}$ obtained from 100 Monte Carlo simulations.

Fig. 26. Histogram of $V_{\text{max}}$ obtained from 100 Monte Carlo simulations.
Fig. 27. Histogram of $I_{ref}$ after 100 Monte Carlo simulations at 27 °C.

Fig. 28. Histogram of the $I_{ref}$ after 100 Monte Carlo simulations at -20 °C.
Table VIII. Simulated reference generator output values for different process corners at room temperature

<table>
<thead>
<tr>
<th>Process Corner</th>
<th>$V_{\text{max}}$</th>
<th>$V_{\text{min}}$</th>
<th>$I_{\text{ref}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT</td>
<td>484.6mV</td>
<td>663.5mV</td>
<td>26.84nA</td>
</tr>
<tr>
<td>FF</td>
<td>438mV</td>
<td>628mV</td>
<td>27.81nA</td>
</tr>
<tr>
<td>SS</td>
<td>533mV</td>
<td>699mV</td>
<td>25.82nA</td>
</tr>
</tbody>
</table>

Table VIII. summarizes the simulated values of the reference voltages and reference current for different process corner cases. The results indicate that reference current is robust to the process variations. On the other hand, the absolute value of the reference voltage varies significantly. However, the difference between the two reference voltages changes only ±11mV, which leads to a robust oscillation frequency as dictated by equation (2) based on this voltage difference. The correlation of the reference voltages stems from the fact that $V_{\text{max}}$ is generated from $V_{\text{min}}$ using a resistive divider as shown in Fig. 16. Hence, it is important that resistors $R_1$, $R_2$ and $R_3$ are matched in the layout such that the correlation between $V_{\text{min}}$ and $V_{\text{max}}$ that reduces the variation of the difference ($V_{\text{max}} - V_{\text{min}}$) depends on the following equation:
Table IX. Comparison with other reference generation circuits

<table>
<thead>
<tr>
<th></th>
<th>This work*</th>
<th>[23]**</th>
<th>[17]**</th>
<th>[21]*</th>
<th>[24]**</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.11µm</td>
<td>0.18µm</td>
<td>0.35µm</td>
<td>0.35µm</td>
<td>3µm</td>
</tr>
<tr>
<td>V_{DD}</td>
<td>1.2V</td>
<td>1.5V</td>
<td>1.4-3V</td>
<td>2.5V</td>
<td>5V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>1µW</td>
<td>17.25µW</td>
<td>300nW</td>
<td>0.81µW</td>
<td>10µW</td>
</tr>
<tr>
<td>Output Reference Voltage</td>
<td>484.6 mV 663.5 mV</td>
<td>621mV</td>
<td>745mV</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Output Reference Current</td>
<td>26.84nA</td>
<td>N/A</td>
<td>N/A</td>
<td>92.7nA</td>
<td>774nA</td>
</tr>
<tr>
<td>TC of The Output Voltage</td>
<td>7.5ppm/ºC (663.5mV)</td>
<td>16ppm/ºC (484.6mV)</td>
<td>11.5ppm/ºC</td>
<td>7ppm/ºC</td>
<td>N/A</td>
</tr>
<tr>
<td>TC of the Output Current</td>
<td>166ppm/ºC</td>
<td>N/A</td>
<td>N/A</td>
<td>288ppm/ºC</td>
<td>375ppm/ºC*</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-20 - 80ºC</td>
<td>-20 - 120ºC</td>
<td>-20 - 80ºC</td>
<td>-20 - 100ºC</td>
<td>0 - 80ºC</td>
</tr>
</tbody>
</table>

* The temperature dependence was reported as 3% from 0ºC to 80ºC.
* Simulation result.
** Measurement result.

Table IX compares the performance of the integrated reference generator with other reference circuits. The proposed reference generator can generate two different output voltages and a nano-ampere range current simultaneously, which is a feature that the other reference generation circuits do not have. In comparison, the dual reference voltage/current generation circuit from this work has relatively low temperature coefficients and low power consumption, making it suitable for low-power applications.
3.2. Comparator simulation results

As described in Section 2.4, the amplifier adopted in this design is used as open-loop comparator. Thus, the open-loop phase margin is not a critical design concern as for amplifiers used in a closed-loop configuration where stability has to be guaranteed with feedback. Nevertheless, standard simulations were completed to characterize the amplifier. Fig. 30 shows the simulated frequency response, from which it can be observed that the amplifier has a DC gain of 43.8dB (154V/V) and a phase margin of 70.37º.

Fig. 30. Simulated open-loop gain and phase shift vs. frequency of the amplifier used as comparator.
Fig. 31. Histogram of the comparator’s input-referred offset voltage obtained with 100 Monte Carlo simulations.

Fig. 31 illustrated the histogram of the comparator’s input-referred offset voltage, showing a mean value ($\mu$) of 139$\mu$V, and a standard deviation of 1.6mV. Compared with the difference of the two reference voltages, which is at the scale of hundreds of millivolts, the input-referred offset voltage has a negligible impact on the oscillation frequency. The specifications of the amplifier used as an open-loop comparator are listed in Table X.

### Table X. Simulated open-loop comparator specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain</td>
<td>43.8dB</td>
</tr>
<tr>
<td>$f_{3dB}$</td>
<td>95KHz</td>
</tr>
<tr>
<td>Unity Gain Bandwidth, $f_u$</td>
<td>12.87MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>70.37$^\circ$</td>
</tr>
<tr>
<td>Input Referred Offset</td>
<td>139$\mu$V</td>
</tr>
<tr>
<td>CMRR (dB at 10KHz)</td>
<td>76.6dB</td>
</tr>
<tr>
<td>PSRR (dB at 10KHz)</td>
<td>43.8dB</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>1.95$\mu$W</td>
</tr>
</tbody>
</table>
3.3. Oscillator simulations

The oscillator in Fig. 6 was designed with a target oscillation frequency of 20KHz as confirmed by the transient output waveform in Fig. 32. Its temperature dependence is visualized in Fig. 33, showing that the oscillation frequency is 20.0KHz at room temperature with a 5pF load capacitance. From the figure, an oscillation frequency variation of 0.64KHz occurs over the 100ºC range, over which the temperature coefficient is 314ppm/ºC. Monte Carlo simulations were performed with the foundry’s statistical device models. Fig. 34 shows the variation of the oscillation frequency in the presence process variations and mismatches, resulting in an estimated standard deviation of 7.9% with 100 samples, which is acceptable in many low-power applications. As shown in Fig. 35 and Fig. 36, the simulated phase noise and RMS period jitter are -91.15dBc/Hz at 10kHz offset and 52.23ns, respectively, confirming the low-noise characteristics of the oscillator.

Fig. 32. Simulated output waveform at node Q’ with 5pF load capacitance.
Fig. 33. Simulated oscillation frequency vs. temperature.

Fig. 34. Histogram of the oscillation frequency obtained from 100 Monte Carlo simulations.
A summary of the simulated oscillator specifications is compared with previous works in Table XI. In comparison to the 842ppm/°C oscillator in [9] with 1.06µW at 80KHz, the oscillator with the proposed
dual reference generator exhibits a relatively good temperature coefficient of 314ppm°C for its power consumption of 4.9µW, which is still low. In this design, the capacitor $C_T$ in Fig. 6 was set to 20pF. By changing the value of the capacitor to 1pF, the oscillation frequency of this design can be varied from 20KHz to 612KHz. Reference [8] achieves an ultra-low power consumption of 0.011µW at 3.3KHz with a reported temperature coefficient of <500ppm/°C and at the expense of a more complex bias current generator with adjustable ratio for tuning. The other works in Table XI consume more power and have a higher temperature coefficient compared to the oscillator presented in this thesis.

<table>
<thead>
<tr>
<th>Table XI. Comparison with other reported oscillators</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>0.11µm</td>
</tr>
<tr>
<td>Frequency</td>
</tr>
<tr>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>Variation with Temperature</td>
</tr>
<tr>
<td>Power Consumption</td>
</tr>
</tbody>
</table>

* The temperature dependence was reported as ±0.09% from -30 °C to 70 °C.
** With tuning using a programmable current mirror.
* Simulation result.
** Measurement result.
4. CHIP LAYOUT DESIGN, PCB DESIGN AND MEASUREMENT RESULTS

Fig. 37 and Fig. 38 show the oscillator layout overview and the die micrograph of the prototype chip.

The die has a total area (with pads) of 400µm × 800µm.

Fig. 37. Oscillator chip layout.

Fig. 38. Die micrograph of the prototype chip.
Fig. 39. Screenshot of the PCB schematic.
Fig. 39 shows the screenshot of the printed circuit board (PCB) schematic from the KiCad software. This PCB schematic is redrawn in Fig. 40 to give a more comprehensive and clear illustration.

Fig. 40. PCB schematic.

The PCB consists of three main sections: the on-board voltage regulators and supply generation circuits, DC bias circuits, and off-chip buffers. Voltage regulators are used to provide low-noise supply voltages on the board. A set of adjustable bias circuits are implemented to generate the desired DC bias conditions for the chip. Furthermore, off-chip reference current and reference voltage generation circuits are realized on the PCB to evaluate the on-chip generators through a results comparison. The digital input
CTR2 can be set high or low on the PCB to control whether on-chip or off-chip reference currents are used during the oscillator operation. Off-chip buffers with enough driving capability are employed to drive the spectrum analyzer that has a 50Ω input resistance. In the PCB layout, the buffer block is placed as close to the chip as possible to minimize noise pick-up. The power consumption in the buffers driving the off-chip load is excluded from the total power consumption of the chip. In a normal application, the on-chip buffer would drive logic gates, resulting in typical transient currents in the nanoampere range when minimum transistor dimensions are used, which generates negligible power dissipation in the first buffer stage compared to the oscillator power consumption. The layout of the PCB is displayed in Fig. 41.

Fig. 41. PCB layout.
Fig. 42 and Fig. 43 show the equipment connections and measurement setup for the chip characterization. An oscilloscope was used to capture the output waveform of the off-chip buffer, and a spectrum analyzer was used to measure its phase noise.

Fig. 42. PCB and measurement equipment.
With off-chip reference currents and voltages, the measured oscillator output frequency is 20KHz. However, as shown in Fig. 44, the frequency of the output is 7.39KHz with on-chip reference currents and voltages, which deviates approximately 12KHz from the designed frequency. There are two possible causes for this discrepancy, either an inaccuracy of the reference current/voltages provided by the on-chip reference generator, or a capacitance deviation (C_T in Fig. 6). In order to determine the value of the on-chip load capacitance, the off-chip reference voltages and current were applied to the chip. Based on the data points in Table XII and equation (2), the average capacitance value of 19.82pF was calculated, which is very close to the designed value of 20pF. Given the values of the measured on-chip reference voltages, it is possible to calculate the value of I_C according to equation (2). The measured on-chip reference voltages are 641mV and 470mV, yielding I_C = 23.7nA. Hence, it can be concluded that the reference current is only around 20% of the designed value (115nA).
Fig. 44. Measured output waveform of the oscillator chip using on-chip references.

Table XII. Oscillation frequencies for different off-chip reference currents

<table>
<thead>
<tr>
<th>$I_{\text{ref}}$</th>
<th>220nA</th>
<th>190nA</th>
<th>160nA</th>
<th>250nA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{max}}$</td>
<td>671mV</td>
<td>671mV</td>
<td>671mV</td>
<td>671mV</td>
</tr>
<tr>
<td>$V_{\text{min}}$</td>
<td>488mV</td>
<td>488mV</td>
<td>488mV</td>
<td>488mV</td>
</tr>
<tr>
<td>frequency</td>
<td>28.7KHz</td>
<td>26.6KHz</td>
<td>23.3KHz</td>
<td>34.3KHz</td>
</tr>
</tbody>
</table>

The schematic in Fig. 45 can be used to assess how much variation of the threshold voltage can result in the observed deviation of the output reference current. Since transistor $M_R$ plays the most critical role in the reference current generation, a voltage source ($V_b$) was inserted at its gate to model threshold voltage variation by sweeping the value of this voltage source. As indicated by the simulation result in Fig. 46, a 24mV threshold voltage change for $M_R$ is enough to cause a reduction of $I_{\text{refP}}/I_{\text{refN}}$ to a value close to 24nA.
In order to decrease the deviation caused by process variations, the transistor \( M_R \) can be separated into several segments instead of using a single large device, which is visualized in Fig. 47. Note that all gates are connected together, and three pairs of transistors are connected in series. Since the sources and drains of each pair are connected in parallel, the drain-source resistances of the two transistors appear in
parallel. In this example, the transistor \( M_R \) (width of 1\( \mu \)m, length of 48\( \mu \)m) was split into six equal-sized transistors \( M_{R'} \) (width of 0.3\( \mu \)m, length of 10.5\( \mu \)m) such that the simulated resistances of both configurations are identical. By implementing multipliers, the transistors can be matched in the layout to reduce the impact of process variations. Monte Carlo simulations were performed to confirm the improvement of the robustness to process variations. The corresponding result is shown in Fig. 48.

![Fig. 47. Replacing \( M_R \) with components with multiplier.](image1)

![Fig. 48. Histogram of the \( I_{ref} \) obtained with 100 Monte Carlo simulations after replacing \( M_R \) with multiple devices.](image2)

Fig. 48 shows the distribution of \( I_{ref} \) after 100 Monte Carlo simulations, where the standard deviation is 3.5\%, which is an improvement compared to the 6\% case in Section 3.1. More reduction of the standard
deviation can be expected if a layout matching technique is used for the configuration with multiple transistors [31]. Furthermore, the transistor variation (and thereby the reference current variation) could be reduced more by using larger sizes for $M_{R}'$, since the standard deviations of device parameters are inversely proportional to the square root of the device area [32].

The phase noise of the oscillator output was measured with the aid of the spectrum analyzer. Fig. 49 reveals a phase noise of -105dBc/Hz at 10kHz offset from the 20KHz fundamental frequency with off-chip references. A frequency counter was used to measure the RMS period jitter (standard deviation of the period), which is 52.55ns (with off-chip current/voltage references) as displayed in Fig. 50. On the other hand, the phase noise and RMS period jitter with on-chip references were also measured. Fig. 51 and Fig. 52 reveal a phase noise of -102.8dBc/Hz at 5KHz offset and a RMS period jitter of 171.7ns. The spike around the offset frequency of 7.5KHz in Fig. 51 can be ignored because it results from the fundamental oscillation frequency component. Generally, it is more appropriate to evaluate the phase noise response at offset frequencies that are smaller than the oscillation frequency.

![Fig. 49. Measured phase noise with off-chip current/voltage references.](image-url)
Fig. 50. Measured RMS period jitter with off-chip current/voltage references.

Fig. 51. Measured phase noise with on-chip current/voltage references.
Fig. 52. Measured RMS period jitter with on-chip current/voltage references.

Table XIII. Comparison of test chip measurement results with other designs

<table>
<thead>
<tr>
<th></th>
<th>This work** (off-chip references)</th>
<th>This work** (on-chip references)</th>
<th>[33]**</th>
<th>[36]**</th>
<th>[35]**</th>
<th>[37]**</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>20KHz</td>
<td>7.39KHz</td>
<td>3.2MHz</td>
<td>2MHz</td>
<td>6.8MHz</td>
<td>1.5MHz</td>
</tr>
<tr>
<td>Power</td>
<td>3.3µW*</td>
<td>4.2µW**</td>
<td>38.4µW</td>
<td>3µW</td>
<td>20mW</td>
<td>38.4µW</td>
</tr>
<tr>
<td>Phase noise</td>
<td>-105dBc/Hz at 10KHz offset</td>
<td>-102.8 dBc/Hz at 5KHz offset</td>
<td>-70dBc/Hz at 10KHz offset</td>
<td>-55 dBc/Hz at 10KHz offset</td>
<td>-110 dBc/Hz at 10KHz offset</td>
<td>-102 dBc/Hz at 10KHz offset</td>
</tr>
<tr>
<td>FOM (dB)</td>
<td>165.8</td>
<td>159.97</td>
<td>164.2</td>
<td>156</td>
<td>153.6</td>
<td>150.7</td>
</tr>
</tbody>
</table>

* Simulation result.
** Measurement result.
* Excludes power of reference generation circuits.
** Includes power of reference generation circuits.

\[
FOM = 10 \log \left( \frac{f_{osc}^2}{f_m^2 \cdot L(f_m) \cdot \frac{1}{P_{diss}}} \right),
\]  \hspace{1cm} (63)
The figure of merit (from [37]) in equation (63) can be used to evaluate the performances of different oscillator designs. A summary of the measurement results of the presented oscillator is compared with other designs in Table XIII. In comparison to the design in [33], the proposed oscillator achieves a slightly higher FOM due to the lower power consumption and phase noise. The FOMs of the other designs in Table XIII are relatively low because of either higher power consumption or higher phase noise. Based on this evaluation, the proposed oscillator is competitive in comparison with other state-of-the-art designs.

The temperature coefficient of the test chip was measured by placing the PCB in a conventional oven, and setting the oven to different temperatures to obtain data points. Only the 7.39KHz case with on-chip references was tested in order to characterize the temperature dependence of the chip as described because the references generated outside of the chip (20KHz case) exhibit a different temperature dependence during the heating process than the on-chip components. The measurement results are summarized in Table XIV. Fig. 53 visualizes the temperature dependence of the oscillation frequency, which has a measured temperature coefficient 675ppm/°C. This value is 360ppm/°C higher than the simulation result. This difference is in part caused by the previously discussed process variation related to transistor $M_R$ in Fig. 45, which lead to a non-ideal operating point. However, the measurement setup using a conventional oven also creates discrepancies. More accurate characterization results for the temperature dependence could be obtained if a temperature-controlled chamber is available.
Table XIV. On-chip reference voltages and the oscillation frequencies at different temperatures

<table>
<thead>
<tr>
<th>Temperature</th>
<th>25°C</th>
<th>37°C</th>
<th>44°C</th>
<th>49°C</th>
<th>65°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{max}}$</td>
<td>643mV</td>
<td>641mV</td>
<td>642mV</td>
<td>642mV</td>
<td>639mV</td>
</tr>
<tr>
<td>$V_{\text{min}}$</td>
<td>472mV</td>
<td>468mV</td>
<td>466mV</td>
<td>468mV</td>
<td>467mV</td>
</tr>
<tr>
<td>Frequency</td>
<td>7.30KHz</td>
<td>7.36KHz</td>
<td>7.40KHz</td>
<td>7.42KHz</td>
<td>7.50KHz</td>
</tr>
</tbody>
</table>

Fig. 53. Measured oscillation frequency vs. temperature.
5. CONCLUSIONS AND FUTURE WORK

5.1. Conclusion

Several design considerations for low-power oscillators were discussed in this thesis. A circuit that combines the generation of the reference currents and voltages for a relaxation oscillator was proposed and analyzed. This circuit was employed during the design of a temperature-compensated relaxation oscillator with low power consumption. In the presented design, the two output reference voltages are 484.6mV and 663.5mV, which have simulated temperature coefficients of 7.5ppm/ºC and 16ppm/ºC respectively. The output reference current is 26.84nA, which has a temperature coefficient of 166ppm/ºC. The total power consumption of the relaxation oscillator is 4.9µW with a 1.2V supply in 0.11µm CMOS technology. A prototype chip was fabricated in Dongbu 0.11µm CMOS technology to demonstrate the feasibility of the design technique. The relaxation oscillator has a measured power consumption of 4.2µW, a temperature coefficient of 675ppm/ºC, a phase noise of -102.8dBc/Hz at 5 KHz offset with on-chip references, and a phase noise of -105dBc/Hz at 10KHz offset with off-chip references.

5.2. Future work

As described in Chapter 4, the on-chip reference current value of the fabricated chip was approximately 20% of the value specified during the design process, leading to a significant deviation of the oscillation frequency. To counteract the effect of the process variation that caused the difference, an on-chip self-calibration method could be developed. The implementation of this method could potentially solve the reference current variation challenge. On the other hand, a re-design in which transistor M_R occupies a larger die area and has dimensions that allow to employ layout matching techniques can also result in significant improvement of the reference current accuracy after fabrication.
REFERENCES


