A Design Approach and Integration of a Parametric Measurement Unit onto a 600MHz DCL

A Thesis Presented
by
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to
The Department of Electrical and Computer Engineering

A thesis submitted in partial fulfillment for the degree of Masters of Science in Electrical Engineering

in the field of
Electronic Circuits, Semiconductor Devices, and Microfabrication

NORTHEASTERN UNIVERSITY
Boston, Massachusetts

September 2010
Abstract

The Department of Electrical and Computer Engineering

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This document proposes a design approach to a Parametric Measurement Unit (PMU) as well as integration of the PMU onto the same Integrated Circuit (IC) as a 600MHz Driver, Comparator, and Active Load (DCL). These circuits are necessary components of many Automated Test Equipment (ATE) systems used to test ICs and are often referred to collectively as the Pin Electronics (PE). While PMUs have been used in test systems for many years, to the author’s knowledge a design approach to such circuits has yet to be published. PMUs are high accuracy low bandwidth circuits that have to drive a range of capacitive loads. The need for high accuracy requires the use of feedback and high gain operational amplifiers. The trade off to be made in these circuits is between accuracy and settling time. Better accuracy requires higher gain which requires more aggressive compensation which increases settling time.

This paper will give an overview of a typical PMU architecture, modes of operation, stability considerations, and important performance metrics. Then a design approach will be proposed that strikes a balance between DC accuracy and settling time. In areas of the circuit that affect the speed of the test path, design techniques will be used to minimize the output capacitance of the PMU allowing its integration onto the 600MHz DCL.
Acknowledgements

I would like to acknowledge Anthony Turvey of Analog Devices Inc. and Dr. Kim of Northeastern University for their technical assistance during the research and writing phases of this paper. During my years at ADI Tony has been a great mentor. He has always been eager to answer any questions I have had in a very thorough and thoughtful manner. I would like to thank Dr. Kim for having the flexibility and patience required to advise a part-time student writing a thesis and for allowing me the freedom to choose this topic.

I would also like to thank Jon Read and Steve Goldstein of Analog Devices Inc. for their assistance in the early phases of this research. Their knowledge of the design topic helped me overcome many obstacles. I would also like to thank Steve for reviewing a draft of the thesis and providing invaluable inputs pertaining to both the technical content and structure of this paper.
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Chapter 1

Introduction

1.1 Motivation

In past Automated Test Equipment (ATE) systems, the Driver, Comparator, Active Load (DCL) and PMU circuits were discrete components. These discrete components were then assembled onto a circuit board referred to as the Pin Electronics (PE) board. This approach was successful for many years, but as IC processes became faster interconnect capacitance and resistance on the PE board began to limit the accuracy of timing measurements made by the Comparator. Critical timing specifications such as rise and fall times and propagation delay were greatly affected due to the RC time constant of these board parasitics. To reduce the board parasitics, the Driver and Comparator were integrated onto the same IC. This was an acceptable solution for increased performance for many years. However, the pressure to decrease the cost of the PE board motivated further integration. The Active Load was the next circuit to be integrated with the Driver and Comparator because the Active Load could easily use the same high speed bipolar process required for the Driver and Comparator. Figure 1.1 shows a high level block diagram of an ATE system with the Driver, Comparator and Active Load on a single IC and the PMU on a separate IC.

To realize a fully cost effective solution it became clear that the PMU needed to be integrated onto the same IC as the DCL. This would increase the number of channels on a test system. Therefore, increasing tester throughput as it would permit more devices to be tested in parallel. Each Device Under Test (DUT) often has multiple pins and each of the pins needs to be tested. Hence, if there are more PE circuits on the PE board more devices can be tested in parallel. Integration of the PMU also allows the removal of one of the mechanical relays in figure 1.1. This reduces cost and increases system reliability as mechanical relays are typically the least reliable component on the PE board.
Figure 1.1: IC Tester Block Diagram Prior to PMU Integration.

While PMUs have been in use in test systems for many years, to the authors knowledge a design approach to such circuits has yet to be published. A good design approach will minimize the number of iterations for a given design and allow the design engineer to make trade offs in performance in various stages of the design process. In a discrete PMU the two major trade offs are DC measurement accuracy and settling time. In order to integrate the PMU with the DCL the output capacitance of the PMU must be taken into account which will require different design techniques as compared to a discrete PMU implementation.

1.2 Design Challenges

Integrating the PMU onto the same IC as the DCL is difficult for two main reasons. First, it often requires the use of high voltage CMOS transistors which are needed for analog switches. Secondly, PMU circuits often have outputs that are capacitive in nature due to their low speeds of operation and the requirement for large feedback compensation capacitors. This output capacitance limits the bandwidth of the test path which then limits the accuracy of critical timing operations of the Driver and Comparator. When the PMU is a separate IC from the DCL a mechanical relay is used to switch the PMU off the test path during high speed measurements, thereby isolating its capacitance. At the present state of the art, PMU’s have been integrated onto the same IC as DCLs with speeds of up to 400MHz. There is now a market need for the PMU to be integrated onto
DCLs with speeds at 600MHz and higher. This paper will propose a design approach to a PMU to meet precise DC and AC specifications while at the same time minimizing its output capacitance allowing it to be integrated onto a 600MHz DCL.

1.3 Thesis Outline

Chapter 2 describes the PMU’s modes of operation and gives a qualitative description of each mode. The PMU is used to force a voltage or a current to a pin of a DUT (commonly referred to as the DUT pin) and measure the corresponding voltage or current at the DUT pin. The accuracy of the forced and measured voltages and currents must be very high. This requires the use of operational amplifiers with large open loop gain. Since the PMU is a closed loop system using negative feedback, it requires compensation to achieve stability. A previous architecture is described and design objectives are given for the new design.

Chapter 3 discusses the DC design of the PMU in all of its modes of operation. A previously determined model of an operational amplifier’s nonlinearity is introduced. This model is used to meet a given nonlinearity specification for each mode of operation by determining a minimum value of the amplifier’s open loop gain. The design of the amplifiers is then discussed and simulations of the circuit are compared to the model.

Chapter 4 details the AC design of the PMU. Its effects on the bandwidth of the overall test path are discussed, and a maximum value of output capacitance is determined. The PMU is then compensated for each mode of operation, and settling times are then determined. Design techniques for decreasing settling time and reducing output capacitance are also introduced. Simulation results are then compared to theoretical values.

Chapter 5 summarizes the results and includes a number of suggestion for future works and potential design improvements.
Chapter 2

Background

2.1 Modes of Operation

A Four Quadrant PMU is capable of forcing and measuring positive and negative voltages and currents and in general will have the following four modes of operation:

1. Force Voltage/Measure Current (FVMI)
2. Force Voltage/Measure Voltage (FVMV)
3. Force Current/Measure Voltage (FIMV)
4. Force Current/Measure Current (FIMI)

The Force parameter is an input to the PMU which gets driven to the DUT and the Measure parameter is the output of the PMU as measured at the DUT. A typical application of the PMU in FVMI mode is to measure input bias current on a single DUT pin, where the PMU forces a voltage onto the DUT pin and measures the corresponding current. A typical application of the PMU in FIMV mode is continuity testing of a DUT pin, where a current is forced into the pin being tested (while every other pin on the DUT is grounded) and the voltage at the pin is measured. Since all ICs have ESD protection, the measured voltage should be the diode drop of the corresponding ESD device.

It is useful for the PMU to have a wide dynamic range allowing it to be used in a broad range of applications. Low current ranges are required when measuring leakage currents and high current ranges are required for measuring low input resistances. Figure 2.1 shows a high level block diagram of a common PMU architecture. The circuit consists of two operational amplifiers, an instrumentation amplifier, a variable sense resistor, two sets of analog switches for selecting the force and measure parameters and a compensation capacitor $C_C$ used to compensate the system.
2.2 Qualitative Description

When forcing a voltage the Force V switch is closed and the Force I switch is opened and the feedback forces

\[ V_{DUT} = V_{IN} \frac{a_1}{1 + \frac{a_1 a_2}{1 + a_2}} \]  

(2.1)

where \( a_1 \) and \( a_2 \) are the DC open loop gain of the Force Amp and Measure Amp respectively. If \( a_1 \) and \( a_2 \) are large \( V_{DUT} \approx V_{IN} \) and the PMU acts as a voltage follower.

When forcing a current the Force I switch is closed and the Force V switch is opened and the feedback forces the difference of the InAmp inputs to be approximately equal to \( \frac{V_{IN}}{G} \). This voltage is impressed across \( R_s \) causing a current \( I_{DUT} \) to flow giving the following expression

\[ I_{DUT} \approx \frac{V_{IN}}{R_s G} \]  

(2.2)

By using a constant InAmp gain \( G \) and varying \( V_{IN} \) the current to and from the DUT can be varied. By varying \( R_s \) the dynamic range can be made to span several orders of magnitude.

When measuring a voltage the Measure V switch is closed and the Measure Amp act as a voltage follower yielding the following equation for the voltage on the measure out pin

\[ V_{MO} = V_{DUT} \frac{a_2}{1 + a_2} \]  

(2.3)
if \( a_2 \) is very large \( V_{MO} \approx V_{DUT} \).

When measuring a current the Measure I switch is closed and either the Force V or the Force I switch is closed. The InAmp simply measures the voltage drop across the resistor and outputs a voltage

\[
V_{MO} \approx I_{DUT} R_S G
\]

(2.4)

Compensation capacitor \( C_c \) is used to stabilize the system and will determine the settling time of the PMU.

### 2.3 Previous Architectures

Figure 2.2 shows a common architecture of a PMU where the variable resistor in Figure 1.2 has been replaced by 5 resistors in series and switches which are used to select the desired sense resistors. In this configuration \( R_{S1} \) is used for the highest current range, \( R_{S1} + R_{S2} \) is used for the second highest current range, \( R_{S1} + R_{S2} + R_{S3} \) is used for the third highest current etc.. For example, If the highest current range is to be selected the force and sense switches to the left of \( R_{S1} \) are closed while all the other switches remain open.

---

![Figure 2.2: Architecture of a Discrete PMU.](image-url)
open. To close the loop, either the Force I or Force V switch must be closed depending on whether Force Voltage or Force Current operation is desired.

### 2.4 Design Objectives

The goal of this thesis is to develop a design approach to a PMU. The approach will allow the PMU to make very accurate DC measurements while minimizing its output capacitance and settling time. The architecture in figure 2.2 will be used as a starting point and modifications will be made as necessary to improve PMU accuracy and minimize the capacitance it provides to the DUT pin. Before the design process begins the desired current and voltage ranges must be specified as this will determine the value of the sense resistors as well as the required drive capability of the Force Amp. This PMU will support the five current ranges and output voltage range listed in table 2.1.

<table>
<thead>
<tr>
<th>Range</th>
<th>Target units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Range 1</td>
<td>+/- 40 mA</td>
</tr>
<tr>
<td>Current Range 2</td>
<td>+/- 1 mA</td>
</tr>
<tr>
<td>Current Range 3</td>
<td>+/- 100 µA</td>
</tr>
<tr>
<td>Current Range 4</td>
<td>+/- 10 µA</td>
</tr>
<tr>
<td>Current Range 5</td>
<td>+/- 2 µA</td>
</tr>
<tr>
<td>Voltage Range</td>
<td>-5 to +5 V</td>
</tr>
</tbody>
</table>

It is convenient to break the design of the PMU into 2 main sections with 4 subsections each.

1. **DC Operation**
   - Measure Voltage
   - Force Voltage
   - Measure Current
   - Force Current

2. **AC Stabilization**
   - Measure Voltage
   - Force Voltage
   - Measure Current
   - Force Current
Chapter 2. Background

The most important DC specification is often the linearity of the forced and measured voltage and current. Therefore, this DC parameter is optimized in the design methodology that follows. The only AC specification of importance is settling time as this determines how quickly accurate DC measurements can be made. There is a fundamental trade off between DC and AC performance in a PMU (or any other feedback system for that matter) such that higher DC accuracies requires longer settling times. This is because higher accuracies require larger open loop gains of the op amps which requires more aggressive compensation to stabilize the loop. This additional compensation reduces the slew rate of the amplifiers which increases settling time. Therefore, a fundamental trade off exists between DC linearity and AC settling time. It will be the goal of this thesis to reach a practical trade off between linearity and settling time.
Chapter 3

DC Design

This chapter explores the DC design of the PMU in all modes of operation. The specification that this chapter will focus on is the linearity of the forced and measured voltages and currents. A previously developed model for an amplifier’s open loop gain will be used to predict the nonlinearity of the forced and measured voltages and currents. Then amplifiers will be designed to meet the gain requirements while also obtaining practical values of Common Mode Rejection and Power Supply Rejection.

3.1 Measure Voltage

The design of the Measure Voltage function will be approached first because it is the least complex mode of the PMU, and it is also part of the Force Voltage loop. It is desirable to have a higher degree of accuracy in Measure Voltage mode compared to Force Voltage mode, as one would like to be able to accurately measure the voltage that they are forcing. The desired specifications in Measure Voltage mode are listed in table 3.1.

<table>
<thead>
<tr>
<th>Measure Voltage specification</th>
<th>target</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Range</td>
<td>± 5 V</td>
<td></td>
</tr>
<tr>
<td>Nonlinearity</td>
<td>± 150 μV</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>≥ 80 dB</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>≥ 80 dB</td>
<td></td>
</tr>
</tbody>
</table>

In Measure Voltage mode the PMU acts as a voltage follower applying to the Measure Out pin a buffered version of the DUT voltage \( V_{DUT} \). A diagram of the PMU in FIMV mode is shown in Figure 3.1. Measure Out and DUT are generally brought out as package pins and \( V_{IN} \) can be generated by an on-chip Digital to Analog Converter (DAC)
or be brought in by a package pin. In FIMV mode the Force I switch is used to close the
loop, and the Measure V switch is closed to select voltage as the measured parameter.
In this example current range 1 is selected by closing the force and sense switches to the
left of $R_{S1}$. Inspection of the feedback circuit yields the following expression for $V_{MO}$

$$V_{MO} = V_{DUT} \frac{a_2}{1 + a_2}$$  \hspace{1cm} (3.1)

The linearity of the measured voltage $V_{MO}$ is an important parameter as many
testers only use a 2 point calibration algorithm to correct for instrument errors. This
allows for correction of any offset and first order gain errors of the PMU. Therefore,
any higher order gain errors the PMU introduces into the system will show up directly
in the voltage measurement result. This nonlinearity is caused by the change in the
measure amps open loop gain as its output voltage is varied\(^1\). This can be expressed
quantitatively as\(^1\)

$$a_2(V_{MO}) = \begin{cases} 
a_{2m} \left[ 1 - \left( \frac{V_{MO}}{V_{SAT}} \right)^2 \right] & |V_{MO}| \leq |V_{SAT}|, \\
0 & |V_{MO}| \geq |V_{SAT}| \end{cases}$$  \hspace{1cm} (3.2)

Where $V_{SAT}$ is the voltage at which the output of the measure amp saturates. For op
amps designed to have a large input and output common mode range $V_{SAT}$ is approx-
imately 1.5V from the power supplies. From equation 3.2 it can be seen that as $V_{MO}$

\(^1\)This error is caused by the nonlinear characteristics of the transistors used in the amplifier design.
approaches $V_{SAT}$, $a_2$ approaches zero and when $V_{MO} = 0$, $a_2$ is at its maximum value $a_{2m}$. A plot of equation 3.2 is shown in figure 3.2 for an $a_{2m}$ and $|V_{SAT}|$ of 50kV and 5V respectively. The actual curve of an op amp will become more nonlinear than the

![Graph of equation 3.2 showing $a_2$ vs $V_{MO}$]

Figure 3.2: Op Amp Open Loop Gain vs Output Voltage.

model predicts as $V_{MO}$ approaches $V_{SAT}$. However, if the circuit is operated far enough away from this region this equation will yield accurate results. To ensure this condition this PMU will use $\pm 8V$ power supplies for a $\pm 5V$ output range. The minimum value of $a_{2m}$ for a given Measure Voltage nonlinearity can be determined by defining the overall circuit nonlinearity as

$$INL_{V_{MO}} = V_{MO_{ideal}} - V_{MO_{model}}$$

(3.3)

Where $V_{MO_{ideal}}$ assumes that $a_2$ is constant and equal to its maximum value $a_{2m}$. Replacing $a_2$ in equation 3.1 with its maximum values gives

$$V_{MO_{ideal}} = V_{DUT} \frac{a_{2m}}{1 + a_{2m}}$$

(3.4)

\[2\] This deviates from the end point definition of linearity. However, it simplifies the analysis considerably and is conservative by a factor of two for the given model.
The modeled measured voltage can be written by replacing $a_2$ in equation 3.1 with equation 3.2 for $|V_{MO}| \leq V_{SAT}$ which gives

$$V_{MO_{model}} = V_{DUT} \frac{a_2 m \left(1 - \left(\frac{V_{MO}}{V_{SAT}}\right)^2\right)}{1 + a_2 m \left(1 - \left(\frac{V_{MO}}{V_{SAT}}\right)^2\right)}$$  \hspace{1cm} (3.5)$$

Substituting equation 3.5 and equation 3.4 into equation 3.3 and solving for $INL_{VMO}$ produces

$$INL_{VMO} = V_{DUT} \frac{a_2 m \left(\frac{V_{MO}}{V_{SAT}}\right)^2}{1 + a_2 m \left(2 - \left(\frac{V_{MO}}{V_{SAT}}\right)^2\right) + a_2^2 m \left(1 - \left(\frac{V_{MO}}{V_{SAT}}\right)^2\right)}$$  \hspace{1cm} (3.6)$$

This equation gives the resultant nonlinearity for a given $a_2 m$, $V_{SAT}$, $V_{DUT}$ and $V_{MO}$. Since the measure amp is acting as a voltage follower, $V_{MO} \approx V_{DUT}$ and the above equation can be rewritten as

$$INL_{VMO} = V_{DUT} \frac{a_2 m \left(\frac{V_{DUT}}{V_{SAT}}\right)^2}{1 + a_2 m \left(2 - \left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right) + a_2^2 m \left(1 - \left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right)}$$  \hspace{1cm} (3.7)$$

This equation reaches its maximum value as $V_{DUT}$ approaches $V_{SAT}$. Therefore, the maximum error will occur at the ends of the output voltage range. The interest of this design is to determine what value of $a_2 m$ is required for a given nonlinearity. This can be accomplished by rearranging equation 3.7 into polynomial form

$$a_2^2 \left(INL_{VMO} \left(1 - \left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right)\right) + a_2 \left(\frac{INL_{VMO}}{V_{DUT}} \left(V_{DUT} \left(\frac{V_{DUT}}{V_{SAT}}\right)^2 - \left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right)\right) + \frac{INL_{VMO}}{V_{DUT}} = 0 \hspace{1cm} (3.8)$$

The minimum required value of $a_2 m$ for a specified INL, $V_{SAT}$ and $V_{DUT}$ can now be determined by solving the above equation for $a_2 m$. Using a value of 5V for $V_{DUT}$ and using $|V_{SAT}| = |V_{DD} - 1.5V| = |V_{SS} - 1.5V| = 6.5V$, an INL error of 150µV requires that $a_2 m \geq 48.3 kV$. A curve of equation 3.7 for the calculated value of $a_2 m$ is shown in figure 3.3. This curve is the predicted nonlinearity of the measure amp using the aforementioned nonlinear gain model and assuming that $V_{MO} \approx V_{DUT}$. Before continuing it is prudent to verify the assumption that $V_{MO} \approx V_{DUT}$ yields accurate results. This will be done using a graphical approach, since a third order equation is involved. A curve of $V_{MO}$ vs $V_{DUT}$ can be constructed by rearranging equation 3.5 to its polynomial form.

$$V_{MO}^3 a_2 m \left(\frac{1}{V_{SAT}}\right)^2 - V_{MO}^2 a_2 m V_{DUT} \left(\frac{1}{V_{SAT}}\right)^2 - V_{MO} \left(1 + a_2 m\right) + V_{DUT} a_2 m = 0 \hspace{1cm} (3.9)$$
Figure 3.4 shows a family of curves for values of $V_{DUT}$ from -5V to +5V and an $a_{2m}$ of 48.3kV. Each curve has three real roots: two at $\pm V_{SAT}$ and a third close to the given value of $V_{DUT}$. The latter is the root of interest and a curve of $V_{MO}$ vs $V_{DUT}$ is shown in figure 3.5. A curve of the nonlinearity error of the measure amp can be produced by subtracting the curve in figure 3.5 from the ideal curve of $V_{MO}$ given by

$$V_{MO\text{ideal}} = V_{DUT} \frac{a_{2m}}{1 + a_{2m}}$$

and this curve is shown in figure 3.6. Finally, the approximation error in assuming $V_{MO} \approx V_{DUT}$ can be obtained by subtracting the curve in figure 3.6 from the curve in figure 3.3. This curve is shown in figure 3.7 and the approximation error is 37.3nV or 0.025% of the predicted nonlinearity and this assumption will be made in all subsequent analysis\(^3\).

\(^3\)The approximation error is subject to the numerical accuracy of the graphical approach. In this approach the accuracy of each root is accurate to within 100nV which is more than enough to support the assumption that $V_{MO} \approx V_{DUT}$ yields accurate results.
**Figure 3.4**: Roots of $V_{MO}$.

**Figure 3.5**: $V_{MO}$ vs $V_{DUT}$. 
Figure 3.6: MV Modeled Nonlinearity.

Figure 3.7: Nonlinearity Approximation Error.
Now that the required gain has been determined, design of the measure amp may begin. The non inverting input of the measure amp ties directly to the DUT pin, and any input bias current will affect the PMU’s ability to accurately measure current. The easy solution is to use a CMOS input stage. However, a single stage CMOS op amp with a gain of $48.3k \frac{V}{V}$ is very difficult to realize so a two stage design will have to be used. The main disadvantage of a two stage design is that it is harder to compensate due to the additional pole added by the second stage. Fortunately, the measure voltage amp will only need to drive a maximum capacitance of 30pF making compensation easier. An overall gain $A_v = A_{v1}A_{v2}$ of $100k \frac{V}{V}$ can be easily accomplished with a two stage design and that will be the target of this design. The first stage will have a gain of $1k \frac{V}{V}$ and the second stage a gain of $100 \frac{V}{V}$. Using a gain of $100k \frac{V}{V}$ in equation 3.8 and solving for INL gives an expected nonlinearity error of $72 \mu V$.

Common mode rejection and power supply rejection are also important DC specifications and this design will strive to meet a minimum PSRR and CMRR of 80dB.

The design of the uncompensated measure amp is shown in figure 3.8. A differential input cascode is a good choice for the first gain stage due to its large gain and common mode rejection. The gain of this stage is $A_{v1} = g_{m1}R_{O1}$, where $g_{m1} = \sqrt{2k'_{n}(W_1/L_1)I_{D1}}$, $I_{D1} = \frac{I_T}{2}$ and $R_{O1} \approx g_{m6}r_{os6}r_{os8} || g_{m4}r_{os4}r_{os2}$. Where $r_{os}$ are the incremental output resistances of the transistors. The gain of the second stage is $A_{v2} = g_{m9}R_{O2}$, where

\footnote{Compensation will be considered in the AC design portion of this paper.}
\( g_{m9} = \sqrt{2k_p(W_9/L_9)I_{D9}} \) and \( R_{O2} \approx g_{m9}r_o10r_o9 \parallel g_{m11}r_o11R_{11} \). Choosing \( I_T = 100\mu A \) a \( W_1/L_1 \) of 15 is required to achieve a gain of \( 1kV/V \) for the first stage. Setting \( I_{D9} \) to 200\( \mu A \) requires a \( W_9/L_9 \) of 16 to achieve a gain of \( 100V/V \) for the second stage. Figure 3.9 shows a plot of the measure amp gain vs frequency which meets the required DC gain of 100dB.

![Figure 3.9: Measure Amp Gain.](image)

Figure 3.10 shows a plot of the simulated nonlinearity overlaid on the predicted nonlinearity. The total nonlinearity error is 61\( \mu V \) which is less than the 72\( \mu V \) predicted by the model and much lower than the specification of 150\( \mu V \). There is less error for negative voltages due to the asymmetrical design of the measure amplifier. This can be corrected by having two different values for \( V_{SAT} \) which changes the nonlinear gain equation to

\[
a_2(V_{MO}) = \begin{cases} 
  a_{2m} \left[ 1 - \left( \frac{V_{MO}}{V_{SAT^+}} \right)^2 \right] & 0 \leq V_{MO} \leq V_{SAT^+}, \\
  a_{2m} \left[ 1 - \left( \frac{V_{MO}}{V_{SAT^-}} \right)^2 \right] & 0 \geq V_{MO} \geq V_{SAT^-}, \\
  0 & |V_{MO}| \geq |V_{SAT^+}^-| 
\end{cases} 
\]

(3.11)

Since positive values of \( V_{MO} \) more closely fits the model and gives a worst case error, this portion of the curve will be used for determining \( a_{2m} \).
A simulation of the open loop gain of the measure amp overlaid on the model is shown in figure 3.11 over a $V_{DUT}$ range of $\pm 5V$. The actual curve closely approximates the model over the given range.
The CMRR of the measure amp can be approximated as

\[
CMRR \approx (1 + 2g_m(dp)r_{\text{tail}})g_m(mir)\left|\frac{r_o(dp)}{r_o(mir)}\right|
\]

(3.12)

where \(g_m(dp)\) is the transconductance of the input differential pair, \(g_m(mir)\) is the transconductance of the current mirror load, \(r_o(dp)\) and \(r_o(mir)\) are the small signal output resistance of the input differential pair and current mirror load respectively. Using

\[
k'_n = 26.4 \frac{\mu A}{\sqrt{V}} \quad \text{and} \quad k'_p = 10.6 \frac{\mu A}{\sqrt{V}}
\]

yields a CMRR of 111dB. Figure 3.12 shows a simulation of the measure amp CMRR which is well above the desired 80dBs and close to the calculated value of 111dB. The PSRR of the measure amp is also an important parameter and is defined as \(PSRR = A_{dm} - A_{sup}\) where \(A_{sup}\) is the gain from the supply to the amplifier output. Plots of \(PSRR_{vdd}\) and \(PSRR_{vss}\) are shown in figures 3.13 and 3.14 respectively. Both are above the design target of 80dB and the DC portion of the measure amp design is complete.
Figure 3.13: Measure Amp VSS PSRR.

Figure 3.14: Measure Amp VDD PSRR.
3.2 Force Voltage

The function of the PMU in Force Voltage mode is to force an accurate voltage at the DUT pin. As in Measure Voltage mode, nonlinearity, CMRR and PSRR are the key DC parameters and the targets are listed in Table 3.2.

<table>
<thead>
<tr>
<th>specification</th>
<th>target units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force Voltage</td>
<td></td>
</tr>
<tr>
<td>Output Range</td>
<td>± 5 V</td>
</tr>
<tr>
<td>Non Linearity</td>
<td>± 0.5 mV</td>
</tr>
<tr>
<td>CMRR</td>
<td>≥ 75 dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>≥ 75 dB</td>
</tr>
</tbody>
</table>

In Force Voltage mode the PMU acts as a voltage follower applying to the DUT pin a buffered version of the input voltage $V_{IN}$. A diagram of the PMU in Force Voltage mode is shown in Figure 3.15.

![Figure 3.15: Force Voltage Block Diagram.](image-url)
The Force V switch is closed as well as the force and sense switches just to the left of $R_{S1}$\textsuperscript{5}. The nonlinearity in Force Voltage mode is due to the nonlinear gain of the force amp and measure amp with respect to their output voltages and can be expressed as before.

\[
a_1(V_{DUT}) = \begin{cases} 
  a_{1m} \left[1 - \left(\frac{V_F}{V_{SAT}}\right)^2\right] & V_F \leq V_{SAT}, \\
  0 & V_F \geq V_{SAT}.
\end{cases} \tag{3.13}
\]

\[
a_2(V_{MO}) = \begin{cases} 
  a_{2m} \left[1 - \left(\frac{V_{MO}}{V_{SAT}}\right)^2\right] & V_{MO} \leq V_{SAT}, \\
  0 & V_{MO} \geq V_{SAT}.
\end{cases} \tag{3.14}
\]

Where the value of $V_{SAT}$ is assumed to be the same for both the force amp and the measure amp. To simplify the analysis and determine how each amplifier’s gain impacts force voltage nonlinearity, the circuit will first be analyzed driving an open circuit. In this mode there is no drop across the sense resistor, hence $V_F = V_{DUT}$ and the following equations can be written.

\[
V_{MO} = V_{DUT} \frac{a_2}{1 + a_2} \tag{3.15}
\]

\[
V_{DUT} = a_1(V_{IN} - V_{MO}) \tag{3.16}
\]

Substituting equation 3.15 into equation 3.16 and solving for $V_{DUT}$ gives.

\[
V_{DUT} = V_{IN} \frac{a_1 (1 + a_2)}{1 + a_2 + a_1 a_2} \tag{3.17}
\]

As in measure voltage mode the circuit nonlinearity is defined as

\[
INL = V_{DUT\text{ideal}} - V_{DUT\text{model}} \tag{3.18}
\]

Where $V_{DUT\text{ideal}}$ is obtained by replacing $a_1$ and $a_2$ in equation 3.17 with their maximum values which produces.

\[
V_{DUT\text{ideal}} = V_{IN} \frac{a_{1m} (1 + a_{2m})}{1 + a_{2m} + a_{1m} a_{2m}} \tag{3.19}
\]

The predicted nonlinear DUT voltage is obtained by replacing $a_1$ and $a_2$ in equation 3.17 with equations 3.13 and 3.14 which yields

\[
V_{DUT\text{model}} = V_{IN} \frac{a_{1m} \left(1 - \left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right) + a_{1m} a_{2m} \left(1 - \left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right) \left(1 - \left(\frac{V_{MO}}{V_{SAT}}\right)^2\right)}{1 + a_{2m} \left(1 - \left(\frac{V_{MO}}{V_{SAT}}\right)^2\right) + a_{1m} a_{2m} \left(1 - \left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right) \left(1 - \left(\frac{V_{MO}}{V_{SAT}}\right)^2\right)} \tag{3.20}
\]

\textsuperscript{5}The sense resistors are not necessary for Force Voltage Measure Voltage mode. However, it is required for Force Voltage Measure Current mode as will be seen later.
Subtracting equation equation 3.20 from equation 3.19, and assuming \( V_{MO} \approx V_{DUT} \) yields the following equation for the PMU nonlinearity in force voltage mode.

\[
INL_{FV} = V_{IN} \frac{a_{1m}^2 a_{2m} \beta^2 (\beta^2 - 1) + a_{1m} \left[ \beta^2 + a_{2m} \beta^2 (2 - \beta^2) + a_{2m} \beta^2 (1 - \beta^2) \right]}{1 + a_{1m}^2 \left( 1 - 2 \beta^2 + \beta^4 \right) + a_{1m} a_{2m} \left( 2 - 3 \beta^2 + \beta^4 \right) + a_{2m} \left( 1 - \beta^2 \right) + a_{2m} \left( 1 - \beta^2 \right)}
\]

(3.21)

where \( \beta = \frac{V_{DUT}}{V_{SAT}} \).

It is instructive to plot \( INL_{FV} \) vs \( a_{1m} \) for the given \( a_{2m} \) of 100kV and this plot is shown in figure 3.16. Observation of figure 3.16 reveals that for a given \( a_{2m} \) there is a single value of \( a_{1m} \) that will yield zero nonlinearity and that this value is approximately equal to the given value of \( a_{2m} \). It also shows that there is very little benefit in making \( a_{1m} > a_{2m} \). To find the exact value of \( a_{1m} \) that yields zero INL, equation 3.21 can be set to zero which produces the following equation

\[
0 = a_{1m}^2 a_{2m} \beta^2 (\beta^2 - 1) + a_{1m} \left[ \beta^2 + a_{2m} \beta^2 (2 - \beta^2) + a_{2m} \beta^2 (1 - \beta^2) \right]
\]

(3.22)

Figure 3.16: Force Voltage Nonlinearity vs \( a_{1m} \).

Setting \( a_{2m} \) to 100kV and solving for \( a_{1m} \), gives \( a_{1m} \approx 100kV \), and two identical op amps may be used to achieve a minimum INL error for the special case of \( R_{DUT} = \infty \).
Before deriving a more general solution for force voltage nonlinearity it is beneficial to construct a plot of force voltage nonlinearity vs $a_{2m}$ with the value of $a_{1m}$ required to meet the design goal of 0.5mV. Setting equation 3.21 to 0.5mV produces a minimum $a_{1m}$ of $12.7k \frac{V}{V}$. Figure 3.17 shows a plot of $INL_{FV}$ vs $a_{2m}$ for the calculated value of $a_{1m}$. The plot shows that if $a_{2m} \geq 100k \frac{V}{V}$ it will have little impact on $INL_{FV}$ and may be neglected\(^6\). Since the PMU will have to drive a range of resistive loads a more general solution is required. The equation representing $V_{DUT}$ with finite $R_{DUT}$ can be obtained by inspection of figure 3.15

$$V_M = V_{DUT} \frac{a_2}{1 + a_2}$$  \hspace{1cm} (3.23)

$$V_F = a_1(V_{IN} - V_M) = I_{DUT}(R_s + R_{DUT})$$  \hspace{1cm} (3.24)

$$I_{DUT} = \frac{V_{DUT}}{R_{DUT}}$$  \hspace{1cm} (3.25)

Substituting equations 3.23 and 3.25 into 3.24 and solving for $V_{DUT}$ gives

$$V_{DUT} = V_{IN} \frac{a_1}{1 + \frac{R_s}{R_{DUT}} + \frac{a_1 a_2}{1 + a_2}}$$  \hspace{1cm} (3.26)

Where $R_s$ is the selected sense resistor $R_{DUT}$ is the resistance seen looking into the DUT and $a_1$, $a_2$ are the DC open loop gain of the force amp and measure amp respectively.

---

\(^6\)This is because the force amp’s nonlinear gain component dominates the INL error.
Neglecting $a_2$ equation 3.26 can be rewritten as

$$V_{DUT} = \frac{a_1}{1 + a_1} \frac{V_{IN}}{1 + R_s R_{DUT}}$$  \hspace{1cm} (3.27)

Since $R_s$ will modulate $V_F$ it must be included in the analysis and rewriting $V_F$ in terms of $V_{DUT}$ gives

$$a_1(V_{DUT}) = \begin{cases} 
  a_{1m} \left[ 1 - \left( \frac{V_{DUT} \left( 1 + \frac{R_s}{R_{DUT}} \right)}{V_{SAT}} \right)^2 \right] & V_{DUT} \left( 1 + \frac{R_s}{R_{DUT}} \right) \leq V_{SAT}, \\
  0 & V_{DUT} \left( 1 + \frac{R_s}{R_{DUT}} \right) > V_{SAT}
\end{cases} \hspace{1cm} (3.28)$$

Replacing $a_1$ in equation 3.26 with its maximum values gives

$$V_{DUT_{ideal}} = \frac{a_{1m}}{1 + a_{1m}} \frac{V_{IN}}{1 + \frac{R_s}{R_{DUT}}} \hspace{1cm} (3.29)$$

The modeled DUT voltage due to $a_1$ can be obtained by substituting equation 3.28 into equation 3.27 which yields

$$V_{DUT_{model}} = V_{IN} \frac{a_{1m} \left[ 1 - \left( \frac{V_{DUT} \left( 1 + \frac{R_s}{R_{DUT}} \right)}{V_{SAT}} \right)^2 \right]}{\left( 1 + a_{1m} \left[ 1 - \left( \frac{V_{DUT} \left( 1 + \frac{R_s}{R_{DUT}} \right)}{V_{SAT}} \right)^2 \right] \right) \left( 1 + \frac{R_s}{R_{DUT} a_{1m} \left[ 1 - \left( \frac{V_{DUT} \left( 1 + \frac{R_s}{R_{DUT}} \right)}{V_{SAT}} \right)^2 \right] \right)} \hspace{1cm} (3.30)$$

As in Measure Voltage mode the force amp act as a voltage follower and $V_{DUT}$ in equation 3.30 can be replaced with $V_{IN}$ to provide a closed ended solution. The nonlinearity of the circuit due to $a_1$ is determined by subtracting 3.30 from 3.29. Referring to table 3.2 the non linearity target of 0.5mV yields a minimum value for $a_{1m}$ of $16k \frac{V}{V}$ and a gain of $17k \frac{V}{V}$ will be targeted. The force amp will have to drive capacitive loads up to 2000pF, have a very wide input and output common mode range while maintaining good CMRR and PSRR. A single stage folded cascode op amp is a good choice for these requirements, and its design will now be considered.

Input bias current is not a concern in the force amp since both inputs are being driven by a low impedance. The inverting input is buffered from the DUT pin by the measure amp and the non inverting terminal will be driven by a low impedance source. This allows the use of a bipolar input stage which has a much higher $g_m$ per unit area than an MOS implementation. Due to the requirements of wide input and output common mode range and high PSRR and CMRR a folded cascode topology will be used, and the force amp design is shown in figure 3.18. Transistors Q1 and Q2 are the input differential pair. Each receives a collector current of $I_{C1} = I_{C2} = \frac{I_T}{2}$ which is generated from current mirror transistors Q9-Q12. Transistors Q3 and Q4 provide
the bias current for the cascode devices Q5 and Q6 which “fold” the input signal back down to the negative supply allowing for a wide input and output common mode voltage range. $I_{C5}$ and $I_{C6}$ are: $I_{C5} = I_{C3} - I_{C1}$ and $I_{C6} = I_{C4} - I_{C2}$. The currents required can be determined by the required gain of $17k \frac{V}{\sqrt{A}}$ which is determined by the $g_m$ of the input differential pair times the parallel combination of $R_{O1}$ and $R_{I2}$ as shown in equation 3.31.

$$A_V = g_m (R_{O1} \parallel R_{I2}). \quad (3.31)$$

Where $g_m = \frac{I_T}{2V_T}$, $R_{O1}$ is the parallel combination of the resistance seen looking into the collectors of $Q_6$ and $Q_7$ and $R_{I2}$ is the parallel combination of the resistance seen looking into the bases of $Q_{14}$ and $Q_{15}$. The resistance seen looking into the collector of $Q_6$ is

$$R_{O6} = r_{o6} (1 + g_{m6} (r_{o2} \parallel (r_{o4} (1 + g_m R_4)))) \quad (3.32)$$

The resistance seen looking into the collector of $Q_7$ is

$$\frac{\beta r_{o7}}{2} \quad (3.33)$$

The input resistance of the output buffer is

$$R_{I2} = (r_{\pi14} + (r_{\pi18} (1 + g_m R_{18}) \parallel (r_{\pi16} + \beta_n (R_{16} + R_s + R_{DUT})))) \quad (3.34)$$

Where $R_s$ is the sense resistor for the given range. Using $R_s = 5k\Omega$, $R_{DUT} = 50k\Omega$ and
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\( R_{16} = 10\Omega \) an iterative process yields the following currents to obtain the desired gain:

- \( I_T = 400\mu\text{A} \)
- \( I_{C3} = I_{C4} = 350\mu\text{A} \)
- \( I_{C14} = I_{C15} = 100\mu\text{A} \)
- \( I_{C16} = I_{C17} = 420\mu\text{A} \)

Figure 3.19 shows a plot of the uncompensated force amp gain vs frequency, the force amp has a DC gain of 84.5dB which is very close to the target of 84.6dB. The modeled

![Figure 3.19: Force Amp Gain.](image)

and simulated Force Voltage nonlinearity are shown in Figure 3.20. The maximum error is 400\( \mu\text{V} \) which is less than than the desired 0.5mV. In this case the model is aggressive for positive voltages lower than 4.5V and future work would benefit from a more accurate model. A plot of the force amp gain vs output voltage is shown in figure 3.21. The plot shows that the bipolar force amp does not match the model as well as the CMOS measure amp does and this deviation explains the inaccuracy of the results.

The CMRR of the force amp is defined as \( CMRR = A_{dm} - A_{cm} \) where \( A_{dm} \) is the differential mode gain shown in figure 3.19 and \( A_{cm} \) is the force amp’s common mode gain. \( A_{cm} \) is highly dependent on the output resistance of the current source used to bias the input differential pair and can be approximated as \( CMRR \approx 4gm1R_{O13}[3] \), where \( R_{O13} \approx \frac{\beta r_{o13}}{2} \). Using an early voltage of 100 and a \( \beta \) of 100 yields a CMRR of 116dB. Figure 3.22 shows a simulation plot of the force amp CMRR. The amplifier has a CMRR of 115dB at low frequencies which is well above the 75dB design goal and
Figure 3.20: Force Voltage Non Linearity.

Figure 3.21: Force Amp Open Loop Gain vs Output Voltage.
close to the calculated value of 116dB. For completeness the force voltage PSRR is also

\[ PSRR = A_{dm} - A_{sup} \]

where \( A_{sup} \) is the gain from the supply to the amplifier output. Plots of \( PSR_{vss} \) and \( PSR_{vdd} \) are shown in figures 3.23 and 3.24 respectively. Both values meet the design target of 75dB and the force amp design is complete.

**Figure 3.22:** Force Amp CMRR.
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Figure 3.23: Force Amp $PSRR_{V_{SS}}$.

Figure 3.24: Force Amp $PSRR_{V_{DD}}$. 
3.3 Measure Current

In Measure Current mode the PMU can either force a voltage or current and measure the resulting current. A typical application of FVMI mode is to measure the input bias current of a specific DUT pin, where the PMU forces a voltage to the DUT and measures the resulting current. Table 3.3 list the targeted DC specifications in Measure Current mode. A diagram of the PMU in FVMI mode is shown in figure 3.25.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Target</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measure Current</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1</td>
<td>+/- 40</td>
<td>mA</td>
</tr>
<tr>
<td>Current Range 2</td>
<td>+/- 1</td>
<td>mA</td>
</tr>
<tr>
<td>Current Range 3</td>
<td>+/- 100</td>
<td>µA</td>
</tr>
<tr>
<td>Current Range 4</td>
<td>+/- 10</td>
<td>µA</td>
</tr>
<tr>
<td>Current Range 5</td>
<td>+/- 2</td>
<td>µA</td>
</tr>
<tr>
<td>Voltage Range</td>
<td>-5 to +5</td>
<td>V</td>
</tr>
<tr>
<td>Nonlinearity</td>
<td>+/- 0.001%</td>
<td>full scale range</td>
</tr>
</tbody>
</table>

Figure 3.25: PMU in FVMI mode.
Inspection of the figure yields the following equations

\[ V_4 = V_{DUT} \frac{a_2}{1 + a_2} - \left( V_{DUT} \frac{a_2}{1 + a_2} - V_{MI} \right) \frac{R_1}{R_1 + R_2} \]  (3.35)

\[ V_5 = V_{o1} \frac{a_2}{1 + a_2} \frac{R_2}{R_1 + R_2} \]  (3.36)

\[ V_{MI} = a_2 (V_5 - V_4) \]  (3.37)

\[ I_{DUT} = \frac{V_{o1} - V_{DUT}}{R_s} \]  (3.38)

Where \( R_s \) is the selected sense resistor. Combining 3.35, 3.36 and 3.38 and solving for \( V_{MI} \) gives

\[ V_{MI} = \left( \frac{a_2}{1 + a_2} \right) \left( \frac{R_2}{R_2 + R_1 (1 + a_2)} \right) (I_{DUT} R_s) \]  (3.39)

It is interesting to note that the measured voltage is independent of \( a_1 \) due to the fact that the instrumentation amplifier senses the voltage across the sense resistor \( R_s \) regardless of the accuracy of the forced voltage or current. \( V_{MI_{\text{ideal}}} \) is obtained by replacing \( a_2 \) in equation 3.39 with its maximum value \( a_{2m} \) which gives

\[ V_{MI_{\text{ideal}}} = \left( \frac{a_{2m}^2}{1 + a_{2m}} \right) \left( \frac{R_2}{R_2 + R_1 (1 + a_{2m})} \right) (I_{DUT} R_s) \]  (3.40)

\( V_{MI_{\text{model}}} \) is obtained by replacing \( a_2 \) in equation 3.39 with its nonlinear model which yields

\[ V_{MI_{\text{model}}} = \left( \frac{a_{2m}^2}{1 + a_{2m}} \right) \left( 1 - \left( \frac{V_{MI}}{V_{SAT}} \right)^2 \right) \left( \frac{R_2}{R_2 + R_1 \left( 1 + a_{2m} \left( 1 - \left( \frac{V_{MI}}{V_{SAT}} \right)^2 \right) \right)} \right) (I_{DUT} R_s) \]  (3.41)

The nonlinearity of the measured current is obtained by subtracting equation 3.41 from equation 3.40 which yields

\[ INL_{V_{MI}} = \frac{a_{2m} I_{DUT} R_s \left( \frac{V_{MI}}{V_{sat}} \right)^2 (R_1 + R_2)}{a_{2m}^2 R_1^2 \left( 1 - \left( \frac{V_{MI}}{V_{sat}} \right)^2 \right) + a_{2m} R_1 \left( 2 - \left( \frac{V_{MI}}{V_{sat}} \right)^2 \right) (R_1 + R_2) + (R_1 + R_2)^2} \]  (3.42)
It is desirable to have $INL_{V_{MI}}$ as a function of $I_{DUT}$ since that is the parameter being measured. This can be done by noting that $V_{MI} \approx I_{DUT} R_s \frac{R_2}{R_1}$ which gives

$$INL_{V_{MI}} = \frac{a_{2m} I_{DUT} R_s \left( I_{DUT} R_s \frac{R_2}{R_1} \right)^2}{a_{2m}^2 R_1^2 \left( 1 - \left( I_{DUT} R_s \frac{R_2}{R_1} \right)^2 \right) + a_{2m} R_1 \left( 2 - \left( I_{DUT} R_s \frac{R_2}{R_1} \right)^2 \right) (R_1 + R_2) + (R_1 + R_2)^2}$$

(3.43)

Since the inputs to the InAmp are involved in measuring current, any input bias current will contribute to measurement error. It would be ideal if the Measure Voltage amplifier could be used for the 3 amplifiers in the measure current block. The gain of $a_{2m}$ determined in the Measure Voltage section can now be used to calculate the resulting measure current nonlinearity and then compared to the desired specification. Using $a_{2m} = 110k \frac{\text{V}}{\text{V}}$ and $I_{DUT} R_s = 1mA \times 500\Omega = 0.5V$ results in an INL error of $24\mu\text{V}$. This can be translated into a current by recalling $V_{MI} \approx I_{DUT} R_s G$, which can be rearrange to give $\frac{I_{DUT}}{V_{MI}}$. In range 2 this translates to a 9.6nA error which is less than the desired specification of 20nA (0.001% FSR). Figure 3.26 shows a plot of the modeled and simulated Measure Current nonlinearity. As in the Measure Voltage case the simulation is more accurate than the model for negative values due to the asymmetry of the amplifier. However, it is the maximum error that is of interest and the model is conservative by 27% compared to the simulated circuit.

---

\(^7\)FSR stands for Full Scale Range, for example in range 2 the current range is $\pm 1mA$ and the FSR is 2mA.
Figure 3.26: Measure Current Non Linearity.
3.4 Force Current

Table 3.4 lists the five current ranges the PMU will accommodate and the specifications the design will strive to meet. Figure 3.27 shows a diagram of the PMU in Force Current mode in Range 1.

<table>
<thead>
<tr>
<th>specification</th>
<th>target</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force Current</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1</td>
<td>+/- 40</td>
<td>mA</td>
</tr>
<tr>
<td>Current Range 2</td>
<td>+/- 1</td>
<td>mA</td>
</tr>
<tr>
<td>Current Range 3</td>
<td>+/- 100</td>
<td>µA</td>
</tr>
<tr>
<td>Current Range 4</td>
<td>+/- 10</td>
<td>µA</td>
</tr>
<tr>
<td>Current Range 5</td>
<td>+/- 2</td>
<td>µA</td>
</tr>
<tr>
<td>Voltage Range</td>
<td>-5 to +5</td>
<td>V</td>
</tr>
<tr>
<td>Nonlinearity</td>
<td>+/- 0.05%</td>
<td></td>
</tr>
</tbody>
</table>

In Force Current mode the Force V switch is open and the Force I switch is closed placing the InAmp inside the feedback path. Since the feedback is negative the force amp will force the output of the InAmp to be approximately equal to the input voltage or

\[ V_{MI} \approx V_{in} \]  

\[(3.44)\]
The transfer function of the InAmp is

$$V_{MI} \approx (V_{IA}^+ - V_{IA}^-)G$$  \hspace{1cm} (3.45)$$

Where $G$ is the gain of the InAmp, setting 3.44 and 3.45 equal to each other gives

$$V_{in} \approx (V_{IA}^+ - V_{IA}^-)G$$  \hspace{1cm} (3.46)$$

If no current flows into the input terminals of the InAmp or the Measure V amp then

$$I_{DUT} \approx \frac{V_{IA}^+ - V_{IA}^-}{R_{s1}}$$  \hspace{1cm} (3.47)$$

Substituting 3.47 into 3.46 and solving for $I_{DUT}$ gives

$$I_{DUT} \approx \frac{V_{IN}}{R_{s1}G}$$  \hspace{1cm} (3.48)$$

For headroom reasons it is advantageous to have $I_{DUT}R_s$ be as small as possible as any voltage drop across the sense resistor limits the range of the output voltage due to the headroom limitations of the force amp. A drop of 0.5V across the sense resistors will be the target for this design. With this in mind a gain of 5 for the InAmp is convenient as this gives a 5V span on the measure out pin for $\pm$ full scale current. Using this gain the required values of the sense resistors can be calculated and are listed below.

- $R_{s1} = 12.5\Omega$
- $R_{s2} = 500\Omega - R_{s1} = 487.5\Omega$
- $R_{s3} = 5k\Omega - R_{s2} - R_{s1} = 4.5k\Omega$
- $R_{s4} = 50k\Omega - R_{s3} - R_{s2} - R_{s1} = 45k\Omega$
- $R_{s5} = 250k\Omega - R_{s4} - R_{s3} - R_{s2} - R_{s1} = 200k\Omega$

A detailed diagram of the PMU in Force Current mode is shown in figure 3.28. Inspection of figure 3.28 yields.

$$V_{MI} \approx (V_{o1} - V_{DUT})\frac{R_2}{R_1}$$  \hspace{1cm} (3.49)$$

Comparing equations 3.49 and 3.45 yields $G = \frac{R_2}{R_1}$

The preceding equations assumed that $a_1$ and $a_2$ of the op amps were infinite, which is never the case. To get a better understanding of how the finite nonlinear gain of the op amps affects the circuits performance a more detailed analysis must be done. Referring to Figure 3.28 the following equations can be written:

$$V_{o1} = a_1(V_{IN} - V_{MI})$$  \hspace{1cm} (3.50)$$

$$V_{o2} = V_{DUT}\frac{a_2}{1 + a_2}$$  \hspace{1cm} (3.51)$$
Chapter 3. DC Design

**Figure 3.28:** Force Current Circuit.

\[ V_{o3} = V_{o1} \frac{a_2}{1 + a_2} \]  
(3.52)

\[ V_4 = V_{DUT} \frac{a_2}{1 + a_2} - (V_{DUT} \frac{a_2}{1 + a_2} - V_{MI}) \frac{R_1}{R_1 + R_2} \]  
(3.53)

\[ V_5 = V_{o1} \frac{a_2 R_2}{1 + a_2 R_1 + R_2} \]  
(3.54)

\[ V_{MI} = a_2(V_5 - V_4) \]  
(3.55)

\[ I_{DUT} = \frac{V_{o1} - V_{DUT}}{R_s} \]  
(3.56)

Where \( R_s \) is the selected sense resistor. Substituting 3.53 and 3.54 into 3.55 and solving for \( V_{MI} \) gives

\[ V_{MI} = \frac{a_2^2}{1 + a_2} \frac{R_2}{R_1 + R_2 + a_2 R_1}(V_{o1} - V_{DUT}) \]  
(3.57)

Solving for \( V_{o1} - V_{DUT} \) in equation 3.56 and for \( V_{MI} \) in equation 3.50 and substituting the results into equation 3.57 and solving for \( I_{DUT} \) yields

\[ I_{DUT} = V_{IN} \frac{a_1 R_1}{1 + a_2 a_1 R_2 R_s + R_1(R_{DUT} + R_s)} \]  
(3.58)

Which reduces to equation 3.48 as \( a_1 \) and \( a_2 \) approach infinity as expected. The ideal linear equation for \( I_{DUT} \) can be written by assuming \( a_1 \) and \( a_2 \) are constant and equal
to their maximum values $a_{1m}, a_{2m}$ which gives

$$I_{DUT\text{ideal}} = V_{IN} \frac{a_{1m} R_1}{1 + a_{2m} a_{1m} R_2 R_s + R_1 (R_{DUT} + R_s)}$$  \(3.59\)

The predicted nonlinearity is defined as the difference between this ideal linear curve and the output curve produced using the nonlinear gain model. Substituting the nonlinear gain equations for $a_1$ and $a_2$ in equation 3.58 gives an expression for $I_{DUT}$ that includes the nonlinearities of $a_1$ and $a_2$.

$$I_{DUT\text{model}} = V_{IN} \frac{a_{1m} R_1 (1 - \alpha^2) (1 + a_{2m} (1 - \alpha^2))}{a_{1m} a_{2m} R_2 R_s \left(1 - \left(\frac{V_{DUT}}{V_{SAT}}\right)^2\right) (1 - \alpha^2) + R_1 a_{2m} (1 - \alpha^2) (R_{DUT} + R_s) + R_1 (R_{DUT} + R_s)}$$  \(3.60\)

where $\alpha = \frac{V_{MI}}{V_{SAT}}$. Since $V_{MI}$ and $V_{DUT}$ are both dependent on $V_{IN}$, a closed end solution is not possible. However, if $R_{DUT}$ is chosen such that it will produce the maximum allowable voltage of 5V when the current is at its maximum value then $V_{DUT} \approx 2V_{IN}$.

Since the feedback is negative and $a_1$ is large, $V_{MI} \approx V_{IN}$. The nonlinearity in Force Current mode is obtained by subtracting equation 3.60 from equation 3.59 while using the aforementioned approximations. A plot of this curve is overlaid on the nonlinearity of the simulated circuit in figure 3.29. The modeled nonlinearity is extremely conservative compared to simulated circuit. Referring to table 3.4 the target specification of 0.05% of full scale range is 100nA in range 3. Therefore, the values of $a_{1m}$ and $a_{2m}$ for Measure Voltage and Force Voltage modes offer sufficient margin for Force Current mode. Hence, no modifications need to be made to the force and measure amplifier designs.
Figure 3.29: Force Current Non Linearity.
Chapter 4

AC Design

While the PMU is a DC measurement circuit its output capacitance reduces the bandwidth of the test path. When the PMU is a separate IC from the Driver, Comparator and Load(DCL) a relay is used to isolate its capacitance from the test path and no care need be taken to minimize its output capacitance. When the PMU is integrated onto the same IC as the DCL the utmost care must be taken to minimize its contribution to the total output capacitance of the DCL.

The DCL specification that is most sensitive to the PMU’s output capacitance is the bandwidth of the comparators. The comparators are used to make 20/80 rise time measurement by setting the low threshold to the 20% value of the input signal and measuring the propagation delay and then setting the high threshold to the 80% value of the input signal and the measurement is repeated. The difference in the propagation delays is the rise time. Any rise time measurement will be affected by the rise time of the system being used to measure it (the comparator). Assuming a gaussian waveshape a good approximation of the measured rise time is\[4].

\[
t_{\text{rise}} = \sqrt{(t_{\text{rise measurement system}})^2 + (t_{\text{rise signal}})^2} \quad (4.1)
\]

A measurement error of 5% is tolerable for most applications which gives

\[
(1.05t_{\text{rise signal}})^2 = (t_{\text{rise system}})^2 + (t_{\text{rise signal}})^2 \quad (4.2)
\]

Solving for \(t_{\text{rise system}}\) yields

\[
t_{\text{rise system}} = 0.32t_{\text{rise signal}} \quad (4.3)
\]
Assuming a first order system, the 20/80 rise time of a signal and the bandwidth of that system are determined by the time constant of the system by the following relationships

\[ t_{20/80} = 1.4\tau \]  \hspace{1cm} (4.4)
\[ f_{3db} = \frac{1}{2\pi\tau} \]  \hspace{1cm} (4.5)

Solving for \( \tau \) in equation 4.4 and substituting this into equation 4.5 gives

\[ t_{20-80} = \frac{0.22}{f_{3dB}} \]  \hspace{1cm} (4.6)

Where \( f_{3dB} \) is the 3dB roll off of the system. Substituting equation 4.6 into equation 4.3 produces

\[ f_{3dB_{\text{system}}} = 3.12 \times f_{3dB_{\text{signal}}} \]  \hspace{1cm} (4.7)

This states that the bandwidth of the measurement system must be at least three times the bandwidth of the signal being measured to preserve a 5% tolerance on the measured rise and fall times. Since the comparator will be expected to measure rise times of signals having a 600MHz bandwidth its bandwidth must be 1.87GHz.

The maximum allowable output capacitance of the PMU can now be obtained by observing figure 4.1. and noting that the 3dB roll off of the system is determined by the time constant created by the total impedance seen by the input of the comparator(neglecting inductance).

\[ f_{3dB_{\text{system}}} = \frac{1}{2\pi R_{OUT} C_{OUT}} \]  \hspace{1cm} (4.8)

where \( C_{OUT} = C_{\text{driver}} + C_{\text{load}} + C_{\text{PMU}} + C_{\text{comph}} + C_{\text{compl}} \) and \( R_{OUT} = 50\Omega \parallel 50\Omega = 25\Omega \). For a bandwidth of 1.87GHz equation 4.8 yields a \( C_{OUT} \) of 3.4pF. Allowing 400fF for \( C_{\text{comph}} + C_{\text{compl}} \) allows the Driver, Active Load, and PMU to each have a maximum capacitance of 1pF and that will be the goal of this design.

Since the PMU is a closed loop system, its stability is critical to its performance as it is used to make very accurate DC measurements and must settle to within 1% of its final value in as short a time as possible. If the PMU is not stable it will oscillate and never settle to a final value. Furthermore, if it is over compensated it will have an overdamped response, and the settling time will be needlessly increased. The design approach in this section will be to stabilize the architecture in figure 4.2 for each mode of operation while meeting the settling time targets listed in tables 4.2, 4.3 and 4.4.
Chapter 4. AC Design

Figure 4.1: DCL Bandwidth Diagram.

Figure 4.2: PMU Architecture.
### Table 4.1: Measure Voltage AC Specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Target</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measure Voltage Settling Time to 1%</td>
<td>1</td>
<td>µs</td>
</tr>
<tr>
<td>$V_{DUT}$=5V Step, 30pF Load</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 4.2: Force Voltage AC Specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Target</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force Voltage Settling Time to 1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$=5V step, $C_{DUT}$ = 2nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1, 2000pF load</td>
<td>50</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 2, 2000pF load</td>
<td>50</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 3, 2000pF load</td>
<td>75</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 4, 2000pF load</td>
<td>250</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 5, 2000pF load</td>
<td>750</td>
<td>µs</td>
</tr>
</tbody>
</table>

### Table 4.3: Measure Current AC Specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Target</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measure Current Settling Time to 1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DUT}$ = 0.5FSR step, 30pF load</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1, 2000pF load</td>
<td>5</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 2, 2000pF load</td>
<td>5</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 3, 2000pF load</td>
<td>25</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 4, 2000pF load</td>
<td>250</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 5, 2000pF load</td>
<td>750</td>
<td>µs</td>
</tr>
</tbody>
</table>

### Table 4.4: Force Current AC Specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Target</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force Current Settling Time to 1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$ = 2.5V step, $C_{DUT}$ = 2nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1, 2000pF $\parallel$ 125Ω load</td>
<td>50</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 2, 2000pF $\parallel$ 5kΩ load</td>
<td>50</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 3, 2000pF $\parallel$ 50kΩ load</td>
<td>500</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 4, 2000pF $\parallel$ 500kΩ load</td>
<td>5</td>
<td>ms</td>
</tr>
<tr>
<td>Current Range 5, 2000pF $\parallel$ 2.5MΩ load</td>
<td>25</td>
<td>ms</td>
</tr>
</tbody>
</table>
4.1 Measure Voltage

In Measure Voltage mode the PMU can either force a current and measure the resulting voltage or force a voltage and measure the resulting voltage. The settling time in these modes will be dominated by the force loop due to the large capacitances that need to be driven at the DUT pin. Therefore, it is sufficient to merely stabilize the Measure Voltage loop without concern for its settling times. However, it is possible to have the PMU measure the voltage at the DUT pin while not forcing anything. This mode will be referred to as Force Nothing Measure Voltage (FNMV) and a settling time of 1µs will be targeted for this mode.

A system will be stable if its phase is less than $-180^\circ$ when the magnitude of its loop gain $|T(s)|$ is unity and the difference between its phase and $-180^\circ$ is known as the phase margin, quantitatively

$$PM = 180^\circ + \angle(|T(s)| = 1)$$

(4.9)

A circuit with 0$^\circ$ phase margin will have an undamped response and will never settle to within 1% of its final value. As will be seen in section 4.2 it is advantageous to have the measure amplifier approach a first order system, which will have a minimum phase margin of 90$^\circ$. Gain margin is also a requirement for stability, and the gain margin of a system is defined as the gain of the system when the phase of the system is $180^\circ$. This can be expressed quantitatively as

$$GM = 0 - |T(s)|, \angle(T(s) = -180)$$

(4.10)

The system must have a gain margin greater than zero for it to have a stable response and a minimum gain margin of 5$^\circ$ will be targeted.

The measure amp from section 3.1 is repeated in figure 4.3 with the addition of a compensation capacitor $C_{\text{comp}}$. Its uncompensated ($C_{\text{comp}} = 0$) gain and phase characteristics are shown in figure 4.4. The uncompensated amplifier is obviously unstable as it has negative phase margin so compensation must be added. The most obvious place to put $C_{\text{comp}}$ is between the drains of M6 and M10 in order to take advantage of Miller multiplication at the high impedance nodes. However, this compensation scheme has the disadvantage of having a right hand plane (RHP) zero at a frequency of $\frac{g_{m}}{C_{\text{comp}}}[2]$ which can be close to the crossover frequency of the amplifier making stability difficult to achieve. This zero can be pushed out to a higher frequency by placing a resistor in series with the capacitor. A few iterations yields a value of 4pF for $C_{\text{comp}}$ and a resistance of 6kΩ to give a phase margin of 82$^\circ$\footnote{A larger phase margin can be achieved by increasing $C_{\text{comp}}$, however this will reduce the dominant pole location which will destabilize the system in Force Voltage mode.} and a gain margin of 10dB.
Figure 4.3: Compensated Measure Amp Design.

|T(s)| \(\phi(s)|
\begin{array}{c}
-120 \\
-100 \\
-80 \\
-60 \\
-40 \\
-20 \\
0 \\
20 \\
40 \\
60 \\
80 \\
100 \\
120 \\
\end{array}
\begin{array}{c}
0.001 \\
0.01 \\
0.1 \\
1 \\
10 \\
1e3 \\
1e4 \\
1e5 \\
1e6 \\
1e7 \\
1e8 \\
\end{array}

PM = -76°, GM = -30dB

Figure 4.4: Measure Amp Uncompensated Gain and Phase.
The bode plot of the compensated measure amp is shown in figure 4.5 and it has a dominant pole at 72Hz.

\[ PM = 82^\circ, \ GM = 10\text{dB} \]

The slew rate of the measure amplifier is determined by the tail current of the amplifier and the compensation capacitor and is defined as

\[ SR = \frac{I_T}{C_{comp}} = \frac{100\mu A}{4pF} = 25\frac{V}{\mu s} \quad (4.11) \]

This circuit will have a minimum settling time of 200ns if there is no overshoot or undershoot. The rising and falling edge step response is shown in figures 4.6 and 4.7 respectively. The rising edge settling time is 197ns and the falling edge settling time is 425ns. The deviation from the expected values is caused by the charging and discharging of the the body capacitance on M1 and M2. However, both values are well below the design target of 1us.

Figure 4.5: Compensated Measure Amp.
Figure 4.6: Measure Amp Step Response.

Figure 4.7: Measure Amp Step Response.
4.1.1 Measure Voltage Capacitance

Now that the settling time has been verified, the measure amplifier’s contribution to the PMU’s output capacitance will be considered. The non-inverting input of the measure amplifier ties directly to the DUT pin, hence, its capacitance will add directly to the output capacitance of the chip. This input capacitance is due to the gate capacitances of M2 in figure 4.3 and is given by

$$C_{in, MV} = C_{gs2} + C_{gd2} \left(1 + \frac{g_{m2}}{g_{m4}}\right) + C_{gb2}$$ (4.12)

Where $C_{gs} = 237\text{fF}$, $C_{gd} = 31.4\text{fF}$, and $C_{gb} = 55.2\text{fF}$, and $g_{m2} \approx g_{m4}$. This gives an input capacitance of 355fF, which is more than one third of the entire 1pF budget. Since this amplifier is also used in force and measure current modes, this capacitance must be minimized. Since the capacitance is directly related to the area of the input device $M2$, making the devices smaller will decrease the input capacitance of amplifier. However, this will decrease the $g_m$ of the input stage which decreases the open loop gain. This decrease in open loop gain will increase the nonlinearity error which is undesirable.

An effective means of isolating capacitance is to place a resistor in series with the capacitance as shown in appendix A. This resistor reduces the current flowing into the capacitor and acts to reduce the capacitance seen by the DUT signal. An effective capacitance of 25fF is acceptable, and this requires a resistance of 14kΩ. If this resistance is made very large it will have an impact on settling time as this resistance and the input capacitance of the measure amp form a low pass filter. The time constant of a 14kΩ resistor and the input capacitance form a time constant of 5ns, which will have a negligible impact on settling time.
4.2 Force Voltage

In Force Voltage mode the PMU will have to drive capacitive loads of up to 2nF making it much more difficult to stabilize than the Measure Voltage loop. Figure 4.8 shows a diagram of the circuit that will be used for stability analysis. Since the force amp will have to drive large capacitive loads, its open loop output resistance $R_o$ must be taken into account. This is especially true in the higher current ranges as it appears in series with $R_s$. Inspection of figure 4.8 produces the following equations

$$V_F = -V_M a_1(s) \quad (4.13)$$

$$V_M = V_T \frac{a_2(s)}{1 + a_2(s)} \quad (4.14)$$

$$V_F = V_T \left( 1 + sC_{DUT} \right) \frac{R_o + R_s}{R_{DUT} + R_o + R_s} \left( \frac{R_{DUT}}{R_{DUT} + R_o + R_s} \right) \quad (4.15)$$

Substituting equations 4.15 and 4.14 into equation 4.13 and solving for $-\frac{V_F}{V_T}$ gives

$$T(s) = \frac{V_R}{V_T} = \frac{R_{DUT}}{R_{DUT} + R_o + R_s} \frac{a_1(s)a_2(s)}{1 + a_2(s)} \left( 1 + sC_{DUT}R_{DUT} \frac{R_o + R_s}{R_{DUT} + R_o + R_s} \right) \quad (4.16)$$

To simplify the analysis the measure amp will be considered a single pole system and it’s frequency response can be represented by the following equation

$$a_2(s) = \frac{a_{2m}}{1 - \frac{s}{\omega_p}} \quad (4.17)$$
Chapter 4. AC Design

The force amp schematic is repeated in figure 4.9 and its uncompensated bode plot is shown in figure 4.10. The Bode plot shows that the force amp approximates a two pole system at frequencies up to 1GHz. The first pole is at 700kHz and is determined by the resistance and capacitance on it’s high impedance node. The second pole is at approximately 600MHz and is determined by the combined resistance and capacitance on the collector of $Q_5$. As can be seen from its bode plot the uncompensated force amp has a PM of $-74^\circ$, and compensation must be added.
If the force amp can be compensated such that it approximates a single pole system its transfer function will be

\[
a_1(s) = \frac{a_{1m}}{1 - \frac{s}{p_1}}
\] (4.18)

Substituting equation 4.17 and equation 4.18 into equation 4.16 produces the following equation for \( T(s) \)

\[
T(s) = \frac{R_{DUT}}{R_{DUT} + R_o + R_s} \cdot \frac{a_{1m}a_{2m}}{1 + a_{2m}} \left( 1 - \frac{s}{p_1} \right) \left( 1 - \frac{s}{p_2(1+a_{2m})} \right) \left( 1 - \frac{s}{p_3} \right)
\] (4.19)

Where \( p_1 \) is the dominant pole of the force amp, \( p_2 \) is the dominant pole of the measure amp and \( p_3 \) is the pole created by \( R_s, R_o \) and the parallel combination of \( R_{DUT} \) and \( C_{DUT} \). The location of \( p_3 \) is determined by setting the right most term in the denominator of equation 4.16 equal to zero and solving for \( s \) which gives

\[
p_3 = -\frac{1}{C_{DUT}(R_o + R_s)} R_{DUT} \] (4.20)

The measure amps pole \( p_2 \) appears as a pole in \( T(s) \), however, it has an effective value of \( p_2(1 + a_{2m}) \) due to it being in a unity gain configuration and will be referred to as

\[
p_2' = p_2(1 + a_{2m}) = 72Hz(1 + 110k \frac{V}{V}) = 7.9MHz
\] (4.21)

From equation 4.19 it can be seen that as \( R_{DUT} \) approaches zero the loop gain approaches zero and \( |p_3| \) approaches \( \infty \) which acts to stabilize the system. If \( R_{DUT} \) approaches infinity equation 4.19 reduces to

\[
T(s) = \frac{a_{1m}a_{2m}}{1 + a_{2m}} \left( 1 - \frac{s}{p_1} \right) \left( 1 - \frac{s}{p_2'} \right) \left( 1 - \frac{s}{p_3} \right)
\] (4.22)

Where \( |p_3| = \frac{1}{C_{DUT}(R_o + R_s)} \). This is the worst case scenario for instability and is the only condition that will be considered because if the system is stable for \( R_{DUT} = \infty \) it will be stable for all other values of \( R_{DUT} \).

Since all ranges must be able to drive a load capacitance of 2nF, the lowest frequency of \( p_3 \) will be in range 5 which has an \( R_o \) of 250kΩ. It is possible for the loop to be unstable if \( p_3 \) approaches \( p_1 \) while there is still positive loop gain as the phase of the system will approach \(-180^\circ\) giving zero phase margin and sustained ringing in the time domain. In order to prevent this \( |p_1| \) must be made sufficiently small such that the systems loop gain approaches zero as it approaches \( p_3 \). The optimal phase margin for most applications is \( 45^\circ \) as the circuit is critically damped. A critically damped circuit will have some overshoot, but will settle to within 1% of its final value, faster than an overdamped...
circuit. Therefore, 45° of phase margin will be the target of this design.

In range 5 the pole created by \( R_S \) and \( C_{DUT} \) is

\[
|p_3| = \frac{1}{2\pi R_s C_{DUT}} = \frac{1}{(2\pi)(250k\Omega)(2nF)} = 318\text{Hz} \tag{4.23}
\]

A force amp gain of \( 17k \frac{V}{V} \) requires

\[
|p_1| = \frac{|p_3|}{17k \frac{V}{V}} = 18.7\text{mHz} \tag{4.24}
\]

Noting that \( p_1 \) is determined by the combined resistance \( R_{O1} \) in figure 4.10 and capacitance on the force amp’s gain node it is possible to adjust \( p_1 \) by adding capacitance to this node. The value of the required compensation capacitor \( C_c \) can now be determined by noting that

\[
|p_1| = \frac{1}{2\pi R_{O1} C_c} \tag{4.25}
\]

Using a value of \( 2.2M\Omega \) for \( R_{O1} \) and solving for \( C_c \) with the required pole location of 18.7mHz produces \( C_c = 3.9\mu F \). Using this value of \( C_c \) the large signal settling time of the PMU will be dominated by the slew rate of the op amp which is defined as

\[
SR = \frac{dV}{dt} = \frac{I_{\text{slew}}}{C_c} = \frac{350\mu A}{3.9\mu F} = \frac{90\mu V}{\mu s} \tag{4.26}
\]

This gives a minimum value for settling time of \( 5V \frac{1\mu s}{90\mu V} = 55\text{ms} \). This is an undesirable time to wait before taking a measurement and the architecture needs to be modified.

In order to reduce settling time the loop gain transfer function \( T(s) \) will have to contain a zero that acts to cancel \( p_3 \). This can be accomplished with lead compensation by placing a capacitor \( C_{ff} \) in parallel with \( R_s \) as shown in figure 4.11[5]. Re-analyzing the circuit gives

\[
T(s) = \frac{a_{1m}a_{2m}}{1 + a_{2m}} \left( 1 + \frac{R_s C_{ff}}{s} \right) \left( 1 - \frac{s}{p_1} \right) \left( 1 - \frac{s}{p_2'} \right) \left( 1 - \frac{s}{p_3} \right) \left( 1 - \frac{s}{p_4} \right) \tag{4.27}
\]

which can be re-written as

\[
T(s) = \frac{a_{1m}a_{2m}}{1 + a_{2m}} \frac{1 - \frac{s}{z_1}}{\left( 1 - \frac{s}{p_1} \right) \left( 1 - \frac{s}{p_2'} \right) \left( 1 - \frac{s}{p_3} \right) \left( 1 - \frac{s}{p_4} \right)} \tag{4.28}
\]
where

\[
|z_1| = \frac{1}{R_s C_{ff}}
\]

\[
p_{2'} = p_2(1 + a_{2m})
\]

\[
|p_{3,4}| = \left| -\frac{C_{DUT}(R_s + R_o) + C_{ff}R_s}{2R_oR_s C_{ff}C_{DUT}} \right| \pm \sqrt{\frac{(C_{DUT}(R_s + R_o) + C_{ff}R_s)^2 - 4R_oR_s C_{ff}C_{DUT}}{2R_o R_s C_{ff}C_{DUT}}} -
\]

Poles \(p_3\) and \(p_4\) will always be real because \(C_{DUT}(R_s + R_o) + C_{ff}R_s > 4R_oR_s C_{ff}C_{DUT}\).

The total magnitude of the system can be expressed by taking the logarithm of equation 4.28 which yields

\[
|T(s)| = 20 \log \left( \frac{a_{1m}a_{2m}}{1 + a_{2m}} \right) + 10 \log \left( 1 + \left( \frac{f}{z_1} \right)^2 \right) -
\]

\[
10 \log \left( 1 + \left( \frac{f}{p_1} \right)^2 \right) - 10 \log \left( 1 + \left( \frac{f}{p_2'} \right)^2 \right) -
\]

\[
10 \log \left( 1 + \left( \frac{f}{p_3} \right)^2 \right) - 10 \log \left( 1 + \left( \frac{f}{p_4} \right)^2 \right)
\]

\[
(4.29)
\]
The total phase of the system can be obtained by summing the inverse tangent of each pole and zero which yields

$$\phi = \arctan \frac{f}{|z_1|} - \arctan \frac{f}{|p_1|} - \arctan \frac{f}{|p_2'|} - \arctan \frac{f}{|p_3|} - \arctan \frac{f}{|p_4|}$$  \hspace{1cm} (4.30)

The above equations are not very intuitive in trying to understand $C_{ff}$’s effects on the circuit, however, by observing the circuit in figure 4.11 the following conclusions can be made.

- As $R_s \to \infty$, little current will flow through $R_s$ and $|p_3| \to |z_1| \to 0$, $C_{ff}$ and $C_{DUT}$ appear in series and $|p_4| \to \frac{1}{\omega C_{DUT} C_{ff}}$

- As $R_s \to 0$, all of the current will flow through $R_s$ and $|p_3| \to \frac{1}{\omega C_{DUT}}$, $|z_1| \to \infty$ and $|p_4| \to \infty$

- As $C_{ff} \to \infty$, $|p_3| \to |z_1| \to 0$, $|p_4| \to \frac{1}{\pi C_{DUT}}$

The actual values of $C_{ff}$ and $R_s$ will obviously lie between these two extremes and a better understanding can be obtained by graphing the system poles and zeros as a function of $C_{ff}$. Figures 4.12 and 4.13 show all of the poles and the single zero from $C_{ff} = 100pF$ to $C_{ff} = 3nF$ for ranges 1 and 5 respectively.

![Figure 4.12: Range 1 Force Voltage Poles and Zeros.](image)

In range 1 where $R_s$ is small there is little cancellation between $p_3$ and $z_1$ until $C_{ff} > 2nF$. However, increasing $C_{ff}$ beyond 500pF moves $|p_4|$ to a lower frequency
which tends to destabilize the system. Therefore, in range 1 capacitor \( C_c \) has much more of an impact on stability than \( C_{ff} \) and \( C_{ff} \) may be neglected. Setting \( C_{ff} \) to zero and iterating equations 4.29 and 4.30 requires that \( |p_1| = 122 \) Hz to achieve a phase margin of 45°. Figures 4.14 and 4.15 show plots of the theoretical and simulated gain and phase in range 1. The simulated phase margin is within 7% of the theoretical value.

The required value of \( C_c \) is determined by substituting 122 Hz into equation 4.25 which gives \( C_c = 592 \) pF, and a 600 pF capacitor will be used.

In the lower current ranges where \( R_s \) is larger than \( R_o \), \( C_{ff} \) will need to be increased to stabilize the system. If \( C_{ff} \) remains zero in range 2, the system only has a phase margin of 11° which is unacceptable. Increasing \( C_{ff} \) to 430 pF results in a phase margin of 45° for range 2. As \( R_s \) is increased \( |z_1| \) and \( |p_3| \) become closer and better pole zero cancellation occurs which increases the phase margin of the system. Therefore, range 2 will determine the minimum required value of \( C_{ff} \) as ranges 3 through 5 will have higher phase margin than range 2.

From a stability standpoint it would be advantageous to make \( C_{ff} \) larger than the minimum required value of 430 pF, however, its impacts on settling time need to be considered. When an input step is applied to the PMU the output of the force amp begins to slew. At this instant \( C_{ff} \) appears in series with \( C_{DUT} \) and the force amp will charge \( C_{DUT} \) through \( C_{ff} \). However, all of the DUT current will eventually flow through the resistor and this happens at a time constant of \( \tau = R_s C_{ff} \). An accurate current measurement cannot be made until this voltage has settled. Therefore, it is this time constant that will determine the settling time in the lower current ranges and the
Figure 4.14: Range 1 Force Voltage Bode Theoretical.

Figure 4.15: Range 1 Force Voltage Bode Actual.
smallest possible value of $C_{ff}$ that yields $45^\circ$ of phase margin will be used. Table 4.5 lists the poles, zero, crossover frequency and phase margin for every range using the previously calculated values for $C_c$ and $C_{ff}$ of 600pF and 430pF respectively.

### Table 4.5: Force Voltage poles, zeros, crossover frequency and phase margin.

<table>
<thead>
<tr>
<th>Range</th>
<th>$R_s$(Ω)</th>
<th>$p_1$(Hz)</th>
<th>$p_2$(Hz)</th>
<th>$p_3$(Hz)</th>
<th>$p_4$(Hz)</th>
<th>$z_1$(Hz)</th>
<th>$f_c$(Hz)</th>
<th>PM(°)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>250k</td>
<td>122</td>
<td>7.9M</td>
<td>262</td>
<td>25.7M</td>
<td>1.48k</td>
<td>366k</td>
<td>86</td>
</tr>
<tr>
<td>4</td>
<td>50k</td>
<td>122</td>
<td>7.9M</td>
<td>1.3k</td>
<td>25M</td>
<td>7.5k</td>
<td>366k</td>
<td>86</td>
</tr>
<tr>
<td>3</td>
<td>5k</td>
<td>122</td>
<td>7.9M</td>
<td>13k</td>
<td>25M</td>
<td>74k</td>
<td>372k</td>
<td>77</td>
</tr>
<tr>
<td>2</td>
<td>500</td>
<td>122</td>
<td>7.9M</td>
<td>128k</td>
<td>26M</td>
<td>740k</td>
<td>571k</td>
<td>45</td>
</tr>
<tr>
<td>1</td>
<td>12.5</td>
<td>122</td>
<td>7.9M</td>
<td>2.6M</td>
<td>53M</td>
<td>30M</td>
<td>1.7M</td>
<td>45</td>
</tr>
</tbody>
</table>

Before calculating the resulting settling time, $C_{ff}$’s impact on output capacitance must be considered. Since $C_{ff}$ is connected directly to the PMU’s output pin, all off its capacitance will add directly to the output capacitance of the chip. This would violate the maximum output capacitance specification of 1pF. Fortunately, the PMU must only present a low output capacitance when it is disabled allowing $C_{ff}$ to be isolated from the DUT pin.

When the PMU is a separate IC from the DCL it is switched off of the test path using a mechanical relay. Typical high speed mechanical relays have a capacitance of less than 500fF and an on resistance of less than 200mΩ. Solid state switches are unable to achieve such low resistance to capacitance ratio due to the carrier mobility limitations of the silicon. One approach to isolate the PMU’s capacitance is to place a switch in series with the output of the PMU as shown in figure 4.16. However, all of the PMU’S current would flow through this switch and this can significantly decrease the headroom of the PMU. For instance, in range 1 the PMU must source and sink 40mA of current. Allowing for a 1V drop across this switch requires the maximum resistance of the switch to be 25Ω. Such a switch would have a capacitance larger than the 1pF budget. Therefore, the switch must be placed in series with $C_{ff}$ to isolate its capacitance from the DUT pin when the PMU is disabled. It would be advantageous to make this switch as physically small as possible to minimize the capacitance it presents to the DUT pin. However, this would cause the switch to have a high on resistance that may be detrimental to the PMU’S stability and these effects will now be analyzed.

Figure 4.17 shows the PMU in Force Voltage mode with the $C_{ff}$ switch modeled by resistor $R_{ff}$. Analysis of the modified circuit gives the following equation for the

---

2The capacitance of the $C_{ff}$ switch will be orders of magnitude lower than $C_{ff}$ and may be neglected.
Figure 4.16: Series Switch Isolation.

Figure 4.17: Force Voltage Loop Analysis with $C_{ff}$ Switch.
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loop gain including $R_{ff}$

$$T(s) = T_0 \frac{1 + C_{ff} (R_s + R_{ff})}{(1 - \frac{s}{p_1})(1 - \frac{s}{p_2}) (1 + s [C_{DUT} (R_s + R_o) + C_{ff} (R_s + R_{ff})] + s^2 C_{DUT} C_{ff} (R_s R_o + R_s R_{ff} + R_o R_{ff}))}$$  

(4.31)

which changes the location of $p_3$ and $p_4$ to

$$|p_{3,4}| = \left| -\frac{C_{DUT}(R_s+R_o)+C_{ff}(R_s+R_{ff})}{2C_{ff}C_{DUT}(R_s R_o+R_s R_{ff}+R_o R_{ff})} \pm \frac{\sqrt{(C_{DUT}(R_s+R_o)+C_{ff}(R_s+R_{ff}))^2 - 4(C_{DUT}C_{ff}(R_s R_o+R_s R_{ff}+R_o R_{ff}))}}{2(C_{DUT}C_{ff}(R_s R_o+R_s R_{ff}+R_o R_{ff}))} \right|$$  

(4.32)

Comparing equation 4.31 with equation 4.28 shows that the on resistance of the switch changed the location of $z_1$ from $\frac{1}{R_{DUT}}$ to $\frac{1}{C_{ff}(R_s+R_{ff})}$. The effect that $R_{ff}$ has on $p_3$ and $p_4$ can be understood by plotting their locations as a function of $R_{ff}$. Figures 4.18, 4.19, 4.20 show plots of $p_3$, $p_4$ and $z_1$ for ranges 5, 2, and 1 respectively.

![Figure 4.18: $p_3$, $p_4$, $z_1$ vs $R_{ff}$ range 5.](image)

In range 5 where $R_{ff} << R_s$, $R_{ff}$ has little effect on $z_1$ and $p_3$, however, it moves $p_4$ to a lower frequency which will reduce the phase margin of the system. In range 1 as $R_{ff}$ increases $|z_1| \rightarrow |p_3|$ and $|p_4| \rightarrow |p_3|$. This keeps the phase margin relatively constant as the negative phase contributed by $p_4$ is offset by the positive phase contributed by $z_1$. In
Figure 4.19: $p_3, p_4, z_1$ vs $R_{ff}$ range 2.

Figure 4.20: $p_3, p_4, z_1$ vs $R_{ff}$ range 1.
range 2, \(|z_1| \) approaches \(|p_3| \) more slowly than \(|p_4| \) approaches \(|p_3| \), thus the phase margin of the system is reduced. A phase margin reduction of \(5^\circ\) will be tolerated in range 2 which leads to a maximum \(R_{ff}\) of 225\(\Omega\). The new poles, zero, crossover frequency and phase margin are shown in table 4.6 for \(R_{ff} = 225\Omega\).

Table 4.6: Force Voltage poles, zeros, crossover frequency and phase margin with cff switch.

<table>
<thead>
<tr>
<th>Range</th>
<th>(R_s(\Omega))</th>
<th>(p_1(\text{Hz}))</th>
<th>(p_2'(\text{Hz}))</th>
<th>(p_3(\text{Hz}))</th>
<th>(p_4(\text{Hz}))</th>
<th>(z_1(\text{Hz}))</th>
<th>(f_c(\text{Hz}))</th>
<th>(PM(\circ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>250k</td>
<td>122</td>
<td>7.9M</td>
<td>262</td>
<td>1.8M</td>
<td>1.5k</td>
<td>360k</td>
<td>76</td>
</tr>
<tr>
<td>4</td>
<td>50k</td>
<td>122</td>
<td>7.9M</td>
<td>1.3k</td>
<td>1.9M</td>
<td>7.4k</td>
<td>361k</td>
<td>75</td>
</tr>
<tr>
<td>3</td>
<td>5k</td>
<td>122</td>
<td>7.9M</td>
<td>13k</td>
<td>1.9M</td>
<td>71k</td>
<td>380k</td>
<td>67</td>
</tr>
<tr>
<td>2</td>
<td>500</td>
<td>122</td>
<td>7.9M</td>
<td>126k</td>
<td>1.8M</td>
<td>510k</td>
<td>616k</td>
<td>40</td>
</tr>
<tr>
<td>1</td>
<td>12.5</td>
<td>122</td>
<td>7.9M</td>
<td>1.5M</td>
<td>2.7M</td>
<td>1.5M</td>
<td>1.7M</td>
<td>46</td>
</tr>
</tbody>
</table>

A CMOS switch with a maximum on resistance of 220\(\Omega\) is shown in figure 4.21 and its resistance curve is shown in figure 4.22. The switches off state capacitance is due to the summation of \(C_{gd_n} = 13fF\), \(C_{db_n} = 11fF\), \(C_{gs_p} = 73fF\) and \(C_{sb_p} = 67pF\) which combine for a total capacitance of 164fF.

Figure 4.21: CMOS Switch.
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The last thing to consider in the Force Voltage design is the switch network that controls which range is selected by switching in the appropriate sense resistor. The switch network is shown in figure 4.23 and \( S_{F1} - S_{F5} \) are the force switches since the forced current flows through them and \( S_{S1} - S_{S5} \) are the sense switches which are used to sense the current flowing through the chosen sense resistor. Each of these switches

\[ R_{xy}(\Omega) \]

\[ V_{xy}(V) \]

\[ v_{force} \]

\[ R_{xy}(\Omega) \]

\[ V_{xy}(V) \]

**Figure 4.22:** Switch On Resistance.

**Figure 4.23:** PMU Block Diagram.
will have an associated resistance and capacitance that must be considered\(^3\). When the PMU is forcing a voltage into a resistive load the current being supplied to the load by the force amp will flow through this switch and any switch resistance will degrade the headroom of the PMU. It will be the goal of this design to limit the drop across this switch to 250mV in ranges 2 through 5 and 0.75V in range 1. Which gives the following for the maximum on resistance of the force switches:

- \( R_{\text{max} F_1} = 18.75\Omega \)
- \( R_{\text{max} F_2} = 250\Omega \)
- \( R_{\text{max} F_3} = 2.5k\Omega \)
- \( R_{\text{max} F_4} = 25k\Omega \)
- \( R_{\text{max} F_5} = 125k\Omega \)

Due to geometry limitations of the high voltage MOS devices, the maximum obtainable switch resistance is 4kΩ and the 2.5kΩ switch designed for range three will also be used in ranges four and five. The 225Ω \( C_{ff} \) switch meets the requirements for range two and this is what will be used. Noting that the capacitance of the \( C_{ff} \) switch is 164fF for an on resistance of 225Ω, a switch with an on resistance of 18.75Ω would be expected to have a capacitance of 2pF. This is double the total allowable capacitance of 1pF, thus an alternative solution for the \( S_{F1} \) switch must be implemented.

### 4.2.1 Total Capacitance

In order to determine the maximum capacitance of the \( S_{F1} \) switch, the total capacitance of the system must be determined. The total output capacitance of the PMU can be obtained by summing all of the individual capacitances of the devices tied to the DUT pin as shown in figure 4.24.

\[
C_{\text{OUT}} = C_{S_{ff}} + C_{Sw} + C_{IA} + C_{MA} \quad (4.33)
\]

where

\[
C_{sw} = C_{eff S_{f1}} + C_{eff S_{s1}} + C_{eff S_{f2}} + C_{eff S_{s2}} + C_{eff S_{f3}} + C_{eff S_{s3}} + C_{eff S_{f4}} + C_{eff S_{s4}} + C_{eff S_{f5}} + C_{eff S_{s5}} \quad (4.34)
\]

\[
C_{sw} = C_{eff S_{f1}} + C_{eff S_{s1}} + C_{eff S_{f2}} + C_{eff S_{s2}} + C_{eff S_{f3}} + C_{eff S_{s3}} + C_{eff S_{f4}} + C_{eff S_{s4}} + C_{eff S_{f5}} + C_{eff S_{s5}} \quad (4.35)
\]

where \( C_{eff_s} \) is the effective capacitance of each switch. The capacitance of the 2.5kΩ switch used for all five of the sense switches and three of the force switches is 15fF

---

\(^3\)These switches will appear in series with the the sense resistors from the perspective of \( C_{ff} \) and their effects on stability will be discussed later in this chapter.
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**Figure 4.24: PMU Output Capacitance.**

and it will be partially isolated by the sense resistors. The effective capacitance of these switches for each range can be obtained by using equation A.7 in appendix A which yields

- \( C_{eff,Sf2} = 162 \text{fF} \)
- \( C_{eff,Sf3} = 14.9 \text{fF} \)
- \( C_{eff,Sf4} = 5.8 \text{fF} \)
- \( C_{eff,Sf5} = 1.4 \text{fF} \)
- \( C_{eff,Ss1} = 15 \text{fF} \)
- \( C_{eff,Ss2} = 15 \text{fF} \)
- \( C_{eff,Ss3} = 14.9 \text{fF} \)
- \( C_{eff,Ss4} = 5.8 \text{fF} \)
- \( C_{eff,Ss5} = 1.4 \text{fF} \)

When the PMU is disabled all of the force and sense switches will be opened and \( C_{IA+} \) will not add to the output capacitance of the PMU. However, the inverting terminal of the InAmp ties directly to the DUT pin and its capacitance will contribute directly to the output capacitance of the PMU. Since this is the same amplifier that is used
for the measure voltage amplifier, a 14kΩ resistor will be placed in series with this input as well as the input of the measure voltage amplifier. This results in an effective capacitance of 25 fF for $C_{IA^-}$ and $C_{MA}$. Inserting all of the above capacitance values into equation 4.33, setting $C_{OUT} = 1pF$ and solving for $C_{eff_{S1}}$ produces a maximum capacitance of 547.8pF.

Since the range 1 sense resistor is only 12.5Ω it will offer virtually no isolation and the design target of this switch will be 500fF. Therefore, the new $S_{F1}$ switch must meet the following criteria:

- It must be capable of sourcing and sinking 40mA of current
- Its output capacitance must be less than 500fF
- The voltage drop across the switch must be less than $\pm$ 0.75V

The above requirements can be accomplished using a tri-stateable buffer as shown in figure 4.25.

---

Figure 4.25: Range 1 Buffer.

This circuit is a basic diamond buffer with tri-state ability provided by diodes $D_1$ and $D_2$ and transistors $Q_9$ – $Q_{18}$. When the circuit is enabled, $Q_9$ and $Q_{16}$ provide 500µA of current to input transistors $Q_3$ and $Q_4$ via the current mirrors composed of $Q_5$ – $Q_8$. When the circuit is disabled the 500µA is split between $Q_{17}$ and $Q_{18}$. $I_{C17}$ flows through $D_5$ and $Q_{21}$ driving the base of $Q_1$ to $vclp\_high + 2V_{be}$. $I_{C18}$ biases up $Q1$ which puts its emitter voltage at $vclp\_high + 3V_{be}$. If the output voltage is less than
\[ v_{clp_{high}} + 2V_{be} \ D_1 \text{ will be reversed biased. Similar analysis shows that } D_2 \text{ will be reversed biased as long as the output voltage is greater than } v_{clp_{low}} - 2V_{be}. \] Setting \( v_{clp_{high}} \) and \( v_{clp_{low}} \) to +3V and -3V respectively ensures that the output will remain tri-stated for DUT pin voltages from -5.5V to +5.5V.

Currents \( I_6 \) and \( I_8 \) must be large enough to supply the base currents of \( Q_1 \) and \( Q_2 \) in addition to providing bias current to \( Q_3 \) and \( Q_4 \). \( I_{b1} \) will be larger than \( I_{b2} \) due to the smaller \( \beta \) of \( Q_1 \). For this process \( \beta_n \approx 100 \) and \( \beta_p \approx 50 \). Recalling that this buffer must source and sink 40mA of current, and allotting 0.5mA for biasing \( Q_3 \) and \( Q_4 \) under full load, gives a minimum value of 1.3mA for \( I_6 \) and \( I_8 \) and a current of 1.5mA will be used. The Quiescent value of the output current can be determined by KVL around the input and output devices which gives

\[
V_{be_4} + V_{D_4} - V_{be_2} - V_{D_2} - V_{D_1} - V_{be_1} + V_{D_3} + V_{be_3} = 0 \quad (4.36)
\]

Since it is the output current we are interested in the \( I_c \) to \( V_{be} \) relationship of the bipolar transistor and the \( I_D \) to \( V_D \) relationship of the pn diode must be used.

\[
V_{be} = v_T \ln \left( \frac{I_C}{A J_{S1}} \right) \quad (4.37)
\]

\[
V_D = v_T \ln \left( \frac{I_D}{A J_{S2}} \right) \quad (4.38)
\]

Where \( A \) is the junction area of the device, \( J_{S1} \) is the saturation current density of the transistor, and \( J_{S2} \) is the saturation current density of the diode, both of which are constant for a given process. Substituting equations 4.37 and 4.38 into equation 4.36 and setting \( I_{C6} = I_{C8} = I \) yields

\[
0 = v_T \ln \left( \frac{I_{C4}}{A_4 J_{S1}} \right) - v_T \ln \left( \frac{I_{C2}}{A_2 J_{S1}} \right) + v_T \ln \left( \frac{I_{C3}}{A_3 J_{S1}} \right) - v_T \ln \left( \frac{I_{C1}}{A_1 J_{S1}} \right) + v_T \ln \left( \frac{I_{D3}}{A_{D3} J_{S2}} \right) - v_T \ln \left( \frac{I_{D1}}{A_{D1} J_{S2}} \right) + v_T \ln \left( \frac{I_{D4}}{A_{D4} J_{S2}} \right) - v_T \ln \left( \frac{I_{D2}}{A_{D2} J_{S2}} \right) \quad (4.39)
\]

If \( A_1 = A_2, \ A_3 = A_4, \ A_{D1} = A_{D2}, \) and \( A_{D3} = A_{D4} \) equation 4.39 reduces to

\[
I_Q = \sqrt{\frac{I}{A_2^2 A_{D2}^2}} \quad (4.40)
\]
The ratio of the two currents are proportional to the area of the output devices $Q_1$, $Q_2$, $D_1$, $D_2$ and the biasing devices $Q_3$, $Q_4$, $D_3$, $D_4$. If the area of the biasing devices is small the circuit will have an unnecessarily large quiescent current causing the device to dissipate excess power. A good trade off between area and power is to make the output devices twice the size of the input devices which produces $I_Q = 3\text{mA}$ for $I = 1.5\text{mA}$.

Since Range 1 is the highest current stage, it will contribute significant capacitance to the DUT pin. Recalling that the output capacitance of this stage cannot exceed 500fF and that all of the capacitance will be due the combination of $D_1$’s cathode capacitance and $D_2$’s anode capacitance, a maximum diode size can be determined. The capacitance of these diodes varies as a function the reverse voltage applied to them, and under worst case circumstances the diodes have a capacitance of $0.455 \frac{\text{pF}}{\mu \text{m}^2}$. Using a capacitance of 500fF gives a total diode area of 879$\mu \text{m}^2$ which will be split evenly between $D_1$ and $D_2$.

The voltage drop across this buffer will be determined by the difference in voltage across input devices $Q_4$, $D_4$ and the output devices $Q_2$ and $D_2$. Each diode will have an associated bulk resistance which can be modeled with a resistor in series with its cathode. The resistance of these diodes is $\frac{4.8\text{k}\Omega}{\text{□}}$ which results in a resistance of $10.7\Omega$ for $R_{D2}$ and $21.4\Omega$ for $R_{D4}$. The drop across this buffer at full load is

$$V_{RA} = I_2R_{D2} + V_{D2} + V_{be2} - I_4R_{D4} - V_{D4} - V_{be4}$$  \hspace{1cm} (4.41)$$

where $V_{be2} = v_T\ln\left(\frac{I_C}{I_{SN}}\right)$, $V_{be4} = v_T\ln\left(\frac{I_C}{I_{SP}}\right)$ and $V_d = v_T\ln\left(\frac{I_D}{I_{SD}}\right)$. Using typical values of $I_s$, $I_2 = 40\text{mA}$ and $I_4 = 1.5\text{mA}$ results in $V_{RA} = 549\text{mV}$, which is less than the required 0.75V. The last thing to consider is the effect that this buffer will have on the PMU’s frequency response. Since the bandwidth of this buffer is much larger than the bandwidth of the Force Voltage loop it will contribute negligible phase into the system. However, its output resistance will appear in series with $R_{s1}$ and this must be taken into account. The output resistance of the buffer is

$$R_{Ob} = (R_{d1} + r_{d1} + r_{e1}) \parallel (R_{d2} + r_{d2} + r_{e2})$$  \hspace{1cm} (4.42)$$

where $r_{d1} = r_{e1} = r_{d2} = r_{e2} = \frac{v_T}{I_Q}$ and $R_{d1}$ is the series resistance of the diodes. Using the previously calculated value of $I_Q = 3\text{mA}$ gives $R_{Ob} = 10\Omega$. This is less than the output resistance of the force amp, which will improve the phase margin slightly compared to its value in table 4.6.

While this buffer adds more power and is much more complex than a simple CMOS transmission gate, it achieves the desired output capacitance necessary to integrate a 40mA current range onto the DCL.

This completes the design of the PMU for Force Voltage operation and the complete PMU schematic is shown in figure 4.26.
Figure 4.26: Top Level Schematic.
Now that the design is complete the simulated magnitude and phase characteristics will be compared to the previously determined theoretical values for all modes. In ranges 3 through 5, the force switches will have negligible impact on stability as it is less than 5% of the overall resistance in these ranges. However, in range 2 the force switch is 45% as large as the sense resistor. This additional resistance will bring $|z_1|$ closer to $|p_3|$ and slightly increase stability. Tables 4.7 and 4.8 lists the theoretical and simulated values of the crossover frequency and phase margin for each range including the resistance of the force switches. The simulated crossover frequency, phase margin and gain margin are within 10% of their theoretical values. Figures 4.27, 4.28, 4.29, 4.30, 4.31, 4.32 show the theoretical and simulated bode plots of ranges 1, 2, and 5 respectively.

<table>
<thead>
<tr>
<th>Range</th>
<th>$R_s$(Ω)</th>
<th>$f_c$(Hz)</th>
<th>PM(°)</th>
<th>GM(dB)</th>
</tr>
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<tbody>
<tr>
<td>5</td>
<td>252.5k</td>
<td>340k</td>
<td>76</td>
<td>29</td>
</tr>
<tr>
<td>4</td>
<td>52.5k</td>
<td>340k</td>
<td>76</td>
<td>29</td>
</tr>
<tr>
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<td>5.225k</td>
<td>358k</td>
<td>68</td>
<td>28</td>
</tr>
<tr>
<td>2</td>
<td>725</td>
<td>521k</td>
<td>43</td>
<td>25</td>
</tr>
<tr>
<td>1</td>
<td>12.5</td>
<td>1.7M</td>
<td>54</td>
<td>16</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Range</th>
<th>$R_s$(Ω)</th>
<th>$f_c$(Hz)</th>
<th>PM(°)</th>
<th>GM(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>252.5k</td>
<td>305k</td>
<td>79</td>
<td>30</td>
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<td>4</td>
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<td>78</td>
<td>30</td>
</tr>
<tr>
<td>3</td>
<td>5.225k</td>
<td>321k</td>
<td>69</td>
<td>30</td>
</tr>
<tr>
<td>2</td>
<td>725</td>
<td>486k</td>
<td>42</td>
<td>27</td>
</tr>
<tr>
<td>1</td>
<td>12.5</td>
<td>1.5M</td>
<td>50</td>
<td>17</td>
</tr>
</tbody>
</table>
Figure 4.27: Range 1 Theoretical Bode Plot.

Figure 4.28: Range 1 Simulated Bode Plot.
Figure 4.29: Range 2 Theoretical Bode Plot.

Figure 4.30: Range 2 Simulated Bode Plot.
Figure 4.31: Range 5 Theoretical Bode Plot.

Figure 4.32: Range 1 Simulated Bode Plot.
The theoretical plots have no more than $-270^\circ$ of phase due to the assumption that $a_2(s)$ and $a_1(s)$ are first order system. The simulated transfer functions has additional poles and a right hand zero at frequencies above 20MHz. Therefore, it is critical that the crossover frequency in all ranges be less than 2MHz for this assumption to yield correct results.

### 4.2.2 Settling Time

Now that the system has been adequately stabilized, settling time results will be verified. The settling time in ranges one and two will be dominated by the slew rate of the force amp which is determined by the compensation capacitor $C_c$ and the current of 350µA available at the gain node. Therefore, the expected settling time in ranges 1 and 2 is

$$ST = \frac{V_{in}}{I_{slew}} \frac{5V}{350\mu A} \frac{1}{600pF} = 8.6\mu s$$  \hspace{1cm} (4.43)

The rising and falling edge settling times for ranges 1 and 2 are shown in figures 4.33, 4.34, 4.35 and 4.36 respectively.
Figure 4.33: Range 1 settling time.

Figure 4.34: Range 1 settling time.
Figure 4.35: Range 2 settling time.

Figure 4.36: Range 2 settling time.
The simulated values in Range 1 are within 1% of their calculated values. The simulated values in range 2 are 35% higher than the predicted value due to the minor overshoot on the waveform. The settling time in Range 5 is not as obvious as the higher current ranges. Since the impedance of the resistor is large compared to $C_{ff}$, all of the current will initially flow through $C_{ff}$ and into $C_{DUT}$. Thus a capacitive divider will form between the two capacitors. For a $V_{DUT}$ change of 5V, the output of the force amp will try to go to $V_f = V_{DUT} \frac{C_{ff} + C_{DUT}}{C_{ff}} = 28V$. However, the output voltage of the force amp will saturate at 6.5V and the current in $C_{ff}$ will go to zero. Hence, the time that it takes for the output to reach 2.5V will be determined by the time constant formed by $R_s$ and $C_{DUT}$. The output of the force amp will swing from -2.5V to 6.5V while the output will only travel 5V. The time that it takes the output to go 5V can be determined using the following equation.

$$V_{DUT} = V_f (1 - e^{-\frac{t}{\tau}})$$  \hfill (4.44)

Using $\tau = R_s C_{DUT} = (252.5k\Omega)(2nF) = 505\mu s$, $V_f = 9V$ and $V_{DUT} = 5V$ and solving for $t$ gives a settling time of $410\mu s$. Figure 4.35 shows a plot of $V_{DUT}$ for a 5V input step and the settling time is within 4% of the calculated value.

![Figure 4.37: Range 5 settling time.](image)
The final settling times in Force Voltage mode are listed in table 4.9.

**Table 4.9:** Force Voltage Settling Time Specifications.

<table>
<thead>
<tr>
<th>specification</th>
<th>value</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force Voltage Settling Time to 1% Vin=5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1, 2000pF load</td>
<td>10</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 2, 2000pF load</td>
<td>15</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 3, 2000pF load</td>
<td>30</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 4, 2000pF load</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 5, 2000pF load</td>
<td>450</td>
<td>µs</td>
</tr>
</tbody>
</table>
4.3 Measure Current

The settling time in measure current mode will be determined by either the time constant associated with $R_s$ and $C_{ff}$ expressed as $\tau = R_sC_{ff}$ or the slew rate of the force amp. This is due to the fact that the force amp output must rise or fall to accommodate the change in voltage across the sense resistor. If $4.6\tau > \frac{\Delta V_{MI}}{SR_{forceamp}} \frac{R_1}{R_2}$ then the settling time will always be determined by $\tau$ and the measure current output will settle to within 1% of its final value in $4.6\tau$. Figure 4.38 will be analyzed to determine the loop gain of the PMU in measure current mode. Inspection of the circuit results in the following equations

\begin{align*}
V_1 & = V_{DUT} \frac{a_2(s)}{1 + a_2(s)} \\
V_2 & = V_F \frac{a_2(s)}{1 + a_2(s)} \\
V_3 & = V_1 - (V_1 - V_{MI}) \frac{R_1}{R_1 + R_2} \\
V_4 & = V_2 \frac{R_2}{R_1 + R_2} \\
V_{MI} & = a_2(s)(V_3 - V_4)
\end{align*}

Figure 4.38: Instrumentation Amplifier.
Substituting equations 4.45 and 4.46 into equations 4.47 and 4.48 and then substituting the result into equation 4.49 yields

\[ H(s) = \frac{V_{MI}}{V_F - V_{DUT}} = \frac{a_2(s)^2 R_2}{1 + a_2(s) \frac{R_1}{R_1 + R_2}} \] (4.50)

Comparing this with the standard form; \( H(s) = \frac{A(s)}{1 + T(s)} \) yields

\[ T(s) = a_2(s) \frac{R_1}{R_1 + R_2} \] (4.51)

Hence, if \( a_2(s) \) exhibits a stable response so will \( T(s) \). Therefore, the same amplifier used for measure voltage operation may be used in the measure current design. Since \( a_2(s) \) approximates a first order system, equation 4.51 can be rewritten as

\[ T(s) = \frac{a_{2m}}{1 - p_2^2 \frac{R_1}{R_1 + R_2}} \] (4.52)

where \( p_2 \) is the dominant pole of the amplifier and is equal to 72Hz from measure voltage analysis.

The magnitude of \( T(s) \) can be determined by taking the logarithm of equation 4.52 which gives

\[ |T(s)| = 20 \log \left( a_{2m} \frac{R_1}{R_1 + R_2} \right) - 10 \log \left( 1 + \left( \frac{f}{p_1} \right)^2 \right) \] (4.53)

The phase of \( T(s) \) is

\[ \phi = \arctan \left( \frac{f}{p_2} \right) \] (4.54)

The DC value of \( T(s) \) can be obtained by replacing setting \( f \) in equation 4.53 to zero and using the previously determined values of \( a_{2m} = 100kV \), \( R_2 = 25k\Omega \) and \( R_1 = 5k\Omega \) which gives \( |T(0)| = 84.6dB \). The crossover frequency can be determined by setting equation 4.53 to zero and solving for \( f \) which gives \( f_c = 1.22MHz \).

A simulation of the \( T(s) \) is shown in figure 4.39 and it has a low frequency value of 84.5dB, a crossover frequency of 1.1MHz, a phase margin of 86°, and a gain margin of 25dB. The response is very stable and will produce a finite settling time.

Since the force amp has a constant slew rate equal to \( \frac{350\mu A}{600pf} \), the time it takes to move 0.5V is 857ns. This can be compared to \( 4.6\tau \) to predict the settling time for each range.

- Range 5: \( 4.6\tau = (252.5k\Omega)(430pf) = 499.5\mu s \)

- Range 4: \( 4.6\tau = (52.5k\Omega)(430pf) = 104\mu s \)
Figure 4.39: Measure Current Bode Plot.

- Range 3: $4.6\tau = (5.225k\Omega)(430pf) = 10.3\mu s$

- Range 2: $4.6\tau = (775\Omega)(430pf) = 1.5\mu s$

- Range 1: $4.6\tau = (12.5\Omega)(430pf) = 25\text{ns}$

The settling time will be determined by $\tau$ in every range except range 1 where the expected settling time will be 857ns. Figures 4.40, 4.41, 4.42, 4.43, 4.40 and 4.45 are plots of the measure current output in ranges 1, 2 and 5.
Figure 4.40: Range 1 Measure Current Settling Time.

Figure 4.41: Range 1 Measure Current Settling Time.
Figure 4.42: Range 2 Measure Current Settling Time.

Figure 4.43: Range 2 Measure Current Settling Time.
Figure 4.44: Range 5 Measure Current Settling Time.

Figure 4.45: Range 5 Measure Current Settling Time.
All of the values are within 5% of their predicted values except for range 2 which is within 16% of its theoretical value. The larger deviation in range 2 is because the time it takes the force amp to slew is not negligible compared to $\tau$ as is the case in ranges 3, 4 and 5. The final settling times are listed in table 4.10.

Table 4.10: Measure Current AC Specifications.

<table>
<thead>
<tr>
<th>specification</th>
<th>value</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measure Current Settling Time to 1% Vin=5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1, 2000pF load</td>
<td>1</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Current Range 2, 2000pF load</td>
<td>2</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Current Range 3, 2000pF load</td>
<td>12</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Current Range 4, 2000pF load</td>
<td>120</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Current Range 5, 2000pF load</td>
<td>525</td>
<td>$\mu$s</td>
</tr>
</tbody>
</table>
4.4 Force Current

The PMU’s stability in Force Current mode can be determined by analyzing figure 4.46 where the loop is broken at the output of the instrumentation amplifier. Capacitor $C_{ff}$ has been removed as it is not known whether it is necessary in Force Current operation.

**Figure 4.46: Force Current Loop Analysis.**
Inspecting figure 4.46 the following equations can be written

\[ Z_{DUT} = \frac{R_{DUT}}{1 + sC_{DUT}R_{DUT}} \] (4.55)

\[ V_F = -V_Ta_1(s) \] (4.56)

\[ V_R = a_2(s)(V_+ - V_-) \] (4.57)

\[ V_+ = V_1' \frac{R_2}{R_1 + R_2} \] (4.58)

\[ V_- = V_{DUT}' \frac{R_2}{R_1 + R_2} + V_T \frac{R_1}{R_1 + R_2} \] (4.59)

\[ V_1 = V_F \frac{R_s + Z_{DUT}}{R_s + Z_{DUT} + R_o} \] (4.60)

\[ V_1' = V_1 \frac{a_2(s)}{1 + a_2(s)} \] (4.61)

\[ V_{DUT}' = V_{DUT} \frac{a_2(s)}{1 + a_2(s)} \] (4.63)

Substituting equation 4.55 into equation 4.60 gives

\[ V_1 = V_F \left( \frac{R_s + R_{DUT}}{R_s + R_{DUT} + R_o} \right) \left( 1 + sC_{DUT} \frac{R_s R_{DUT}}{R_s + R_{DUT}} \right) \left( 1 + sC_{DUT} \frac{R_s + R_o}{R_s + R_o + R_{DUT}} \right) \] (4.64)

Substituting equation 4.64 into equation 4.61 then substituting the result into equation 4.58 produces

\[ V_+ = -V_T \left( \frac{a_1(s)a_2(s)}{1 + a_2(s)} \right) \left( \frac{R_2}{R_1 + R_2} \right) \left( \frac{R_s + R_{DUT}}{R_s + R_{DUT} + R_o} \right) \left( 1 + sC_{DUT} \frac{R_s R_{DUT}}{R_s + R_{DUT}} \right) \left( 1 + sC_{DUT} \frac{R_s + R_o}{R_s + R_o + R_{DUT}} \right) \] (4.65)
Substituting equation 4.62 into equation 4.63 and solving for $V'_{DUT}$ then substituting the result into equation 4.59 gives

$$V_\tau = -V_T \left( \frac{a_1(s)a_2(s)}{1+a_2(s)} \right) \left( \frac{R_{DUT}}{R_s + R_{DUT} + R_o} \right) \left( \frac{1}{1+sC_{DUT} \left( \frac{R_s + R_{DUT}}{R_s + R_{DUT} + R_o} \right)} \right) + V_R \frac{R_t}{R_1 + R_2}$$

(4.66)

Substituting equations 4.65 and equation 4.66 into equation 4.57 and approximating $a_1(s)$ and $a_2(s)$ as first order systems gives

$$T(s) = T_0 \left( 1 - \frac{s}{z_1} \right) \left( 1 - \frac{s}{p_1} \right) \left( 1 - \frac{s}{p_2'} \right) \left( 1 - \frac{s}{p_3'} \right)$$

(4.67)

where

- $T_0 = \left( \frac{a_1 a_2}{1+a_2} \right) \left( \frac{R_2}{R_1 (1+a_2) + R_2} \right) \left( \frac{R_s}{R_s + R_{DUT} + R_o} \right)$
- $|z_1| = \frac{1}{C_{DUT} R_{DUT}}$
- $|p_2'| = p_2 (1+a_2)$
- $|p_2''| = p_2 (1+a_2 \frac{R_1}{R_1 + R_2})$
- $|p_3'| = \frac{1}{C_{DUT} R_{DUT} \left( \frac{R_s + R_o}{R_s + R_o + R_{DUT}} \right)}$

Where $p_1$ and $p_2$ are the dominant pole of the force amp and measure amp respectively.

The magnitude of of $T(s)$ is given by

$$|T(s)| = 20 \log(T_0) + 10 \log \left( 1 + \left( \frac{f}{z_1} \right)^2 \right) - 10 \log \left( 1 + \left( \frac{f}{p_1} \right)^2 \right) - 10 \log \left( 1 + \left( \frac{f}{p_2'} \right)^2 \right) - 10 \log \left( 1 + \left( \frac{f}{p_2''} \right)^2 \right) - 10 \log \left( 1 + \left( \frac{f}{p_3'} \right)^2 \right)$$

(4.68)
The phase of \( T(s) \) is given by

\[
\phi = \arctan \frac{f}{z_1} - \arctan \frac{f}{p_1} - \arctan \frac{f}{p_2} - \arctan \frac{f}{p_3}
\]  

(4.69)

Inspection of equation 4.67 yields the following conclusions.

- if \( a_{2m} \gg 1 \), \( T_0 \approx a_{1m} \frac{R_2}{R_1} \left( \frac{R_s}{R_s + R_{DUT} + R_o} \right) \)

- if \( R_s \gg R_o \), \( |p_3| \rightarrow \frac{1}{C_{DUT}R_{DUT}} \left( \frac{R_s}{R_s + R_{DUT}} \right) \)

- if \( R_{DUT} \rightarrow 0 \), \( |p_3| \rightarrow \infty \), \( |T_0| \rightarrow a_{1m} \frac{R_2}{R_1} \left( \frac{R_s}{R_s + R_o} \right) \)

- if \( R_s \gg R_{DUT} + R_o \), \( |p_3| \approx |z_1| = \frac{1}{C_{DUT}R_{DUT}} \), \( |T_0| \rightarrow a_{1m} \frac{R_2}{R_1} \left( \frac{R_s}{2R_s + R_{DUT}} \right) \)

- if \( R_s \rightarrow R_o \), \( T_0 \rightarrow a_{1m} \frac{R_2}{R_1} \left( \frac{R_s}{2R_s + R_{DUT}} \right) \), \( |p_3| \rightarrow \frac{1}{C_{DUT}R_{DUT}} \left( \frac{2R_s}{2R_s + R_{DUT}} \right) \)

As \( R_s \) becomes much larger than \( R_o \) and \( R_{DUT} \), the pole zero cancellation between \( p_3 \) and \( z_1 \) becomes perfect which tends to stabilize the system. However, the value of \( T_0 \) increases which acts to destabilize the system, so for large values of \( R_s \) one would expect the phase margin to be relatively constant as a function of \( R_{DUT} \). The phase margin for each range can be calculated by setting equation 4.68 equal to zero to find the frequency where \( |T(s)| = 1 \) then substituting that value into equation 4.69 to obtain the phase. Table 4.11 shows the the values for all of the poles, zeros, crossover frequency and the phase margin for Force Current operation in range 3 with varying values of \( \frac{R_{DUT}}{R_s} \). As expected the phase margin is independent of \( R_{DUT} \).

**Table 4.11: Force Current Range 3 Loop Gain, poles, zeros, crossover frequency and phase margin.**

| \( \frac{R_{DUT}}{R_s} \) | \( |T_0|\) (dB) | \( |p_1|\) (Hz) | \( |p_2|\) (Hz) | \( |p_2|\) (Hz) | \( |z_1|\) (Hz) | \( f_c\) (Hz) | \( PM(\degree) \) |
|---|---|---|---|---|---|---|---|
| 0 | 98 | 122 | 7.9M | 1.32M | \( \infty \) | 3.5M | -2.9 |
| 0.5 | 95 | 122 | 7.9M | 1.32M | 4.6k | 3.2k | 3.5M | -2.9 |
| 1 | 93 | 122 | 7.9M | 1.32M | 3.1k | 1.6k | 3.5M | -2.9 |
| 10 | 78 | 122 | 7.9M | 1.32M | 1.8k | 159 | 3.4M | -2.9 |
If $R_s \approx R_o$ one might expect the system to be more stable as $R_{DUT} \rightarrow 0$ because $|p_3| \rightarrow |z_1| \rightarrow \infty$. However, if $R_{DUT}$ is equal to its maximum practical value of $10R_s$ then $|z_1| = \frac{1}{(2\pi)(125\Omega)(2nF)} = 637k\text{Hz}$ and $|p_3| = 6|z_1| = 3.8MHz$. Recalling that $|p_2''| = 1.32MHz$, $z_1$ will act to cancel $p_2''$ before $p_3$ contributes significant phase to the system. This increases the phase margin and makes the circuit more stable as compared to $R_{DUT} = 0$. Therefore, a precondition for circuit stability for all ranges of $R_{DUT}$ in all five current ranges is to stabilize the system for $R_{DUT} = 0$.

Referring to table 4.11, the circuit has negative phase margin which means the output will exhibit significant ringing and never settle. The cause of the instability as compared to Force Voltage operation is due to two factors. The first being that $T_0$ gets multiplied by the gain of the InAmp, $\frac{R_2}{R_1}$ as compared to Force Voltage operation where $T_0 \approx a_1m$. Secondly, there is another pole at $p_2'' = 1.32MHz$. The combination of these two factors causes the phase to drop below $180^\circ$ before $|T(s)| = 1$.

A few obvious approaches to regain phase margin are:

- Decrease the gain of the force amp
- Decrease the frequency of $p_1$
- Increase the frequency of $p_2''$

Decreasing the gain of the force amp will increase its nonlinearity error. To decrease the frequency of $p_1$ a larger compensation capacitor must be used which would increase settling times in Force Voltage and Force Current operation. Increasing the frequency of $p_2''$ would decrease measure current stability, all of which are undesirable. Another approach is to insert a zero into the transfer function to cancel the additional phase added by $p_2''$. This can be accomplished by placing a resistor in series with the compensation capacitor $C_c$. The addition of $z_2$ changes the loop gain to

$$T(s) = T_0 \left( \frac{1}{1 - \frac{s}{z_1}} \right) \left( \frac{1}{1 - \frac{s}{z_2}} \right) \left( \frac{1}{1 - \frac{s}{p_1}} \right) \left( \frac{1}{1 - \frac{s}{p_2'}} \right) \left( \frac{1}{1 - \frac{s}{p_2''}} \right) \left( \frac{1}{1 - \frac{s}{p_3}} \right)$$

(4.70)

\[4\text{Although there is excess phase margin in measure current mode, increasing } p_2'' \text{ will increase the crossover over frequency. If there are additional poles or right hand plane zeros at higher frequencies the system will become unstable.}\]
where \( |z_2| = \frac{1}{c_z R_z} \). This changes equations 4.68 and 4.69 to

\[
|T(s)| = 20 \log(T_0) + 10 \log \left( 1 + \left( \frac{f}{z_1} \right)^2 \right) + 10 \log \left( 1 + \left( \frac{f}{z_2} \right)^2 \right) \\
-10 \log \left( 1 + \left( \frac{f}{p_1} \right)^2 \right) - 10 \log \left( 1 + \left( \frac{f}{p_2^t} \right)^2 \right) - 10 \log \left( 1 + \left( \frac{f}{p_2^u} \right)^2 \right) \\
-10 \log \left( 1 + \left( \frac{f}{p_3} \right)^2 \right) \tag{4.71}
\]

\[
\phi = \arctan \frac{f}{z_1} + \arctan \frac{f}{z_2} - \arctan \frac{f}{p_1} - \arctan \frac{f}{p_2^t} - \arctan \frac{f}{p_2^u} - \arctan \frac{f}{p_3} \tag{4.72}
\]

Iterating equations 4.71 and 4.72 produces \( R_z = 100 \Omega \) for a phase margin of \( 45^\circ \) in range 3. Table 4.12 shows the new values for the crossover frequency, phase margin and gain margin with the addition of \( R_z \). It is interesting to note that \( T_0 \) is half as large in range 1 as compared to the lower current ranges. This is due to the fact that \( R_s \approx R_o \).

Table 4.12: Theoretical Force Current loop gain, crossover frequency, phase margin and gain margin.

| \( R_s (\Omega) \) | \( |T_0| \) | \( f_c (\text{Hz}) \) | \( \text{PM} (^\circ) \) | \( \text{GM} (\text{dB}) \) |
|-----------------|---------|-------------|-------------|-------------|
| 250k            | 99      | 5M          | 45          | 100         |
| 50k             | 99      | 5M          | 45          | 100         |
| 5k              | 99      | 5M          | 45          | 100         |
| 500             | 97      | 4.9M        | 45          | 100         |
| 12.5            | 93      | 3.3M        | 50          | 100         |

Table 4.13 shows the simulated values of \( T_0, f_c \) and PM of the PMU in all ranges for \( R_{DUT} = 0 \).

Table 4.13: Simulated Force Current loop gain, crossover frequency, phase margin and gain margin.

| \( R_s (\Omega) \) | \( |T_0| \) | \( f_c (\text{Hz}) \) | \( \text{PM} (^\circ) \) | \( \text{GM} (\text{dB}) \) |
|-----------------|---------|-------------|-------------|-------------|
| 250k            | 98      | 4.3M        | 45          | 11          |
| 50k             | 98      | 4.2M        | 45          | 12          |
| 5k              | 97      | 4.2M        | 46          | 12          |
| 500             | 93      | 3.4M        | 49          | 14          |
| 12.5            | 93      | 2.8M        | 54          | 18          |
The 4dB deviation of $T_0$ in range 2 is due to the resistance of the 225Ω force switch which is comparable to $R_s$ and appears in series with $R_o$. Bode plots of the of the ideal loop gain and the simulated loop gain for range 3 are shown in figures 4.47 and 4.48 and the simulated phase margin is within 2 degrees of the predicted value.

**Figure 4.47:** Force Current Ideal Bode Plot.

**Figure 4.48:** Force Current Simulated Bode Plot.
Although the system was made stable for $R_{DUT} = 0$, in most practical applications the PMU will be forcing current into a resistive load. In order to produce a 5V swing at the output, the value of $R_{DUT}$ will be set to $10R_s$. In the lower current ranges the settling time will be dominated by the time constant associated with $R_{DUT}$ and $C_{DUT}$. This time constant will be referred to as

$$\tau_{DUT} = R_{DUT}C_{DUT} \quad (4.73)$$

In range 4 the expected settling time is

$$ST_{FI} = 4.6R_{DUT}C_{DUT} = 4.6(500\,k\Omega)(2nF) = 4.6\,ms \quad (4.74)$$

Figure 4.49 shows a transient plot of the output voltage in range 4 and the 1% settling time is 4.61ms as predicted. In ranges 1 and 2, $\tau_{DUT} \ll \frac{\Delta V_{DUT}}{SR}$, where $SR$ is the slew rate of the force amp. The final value of $V_{DUT}$ will be 5V, however, the output of the force amp will have to travel an additional 1.25V to accommodate the 0.5V drop across $R_s$ and the 0.75V drop across the range 1 buffer. Taking this into account The expected
settling time is

\[ ST_{F1} = \frac{6.25V}{0.583V} = 10.7\mu s \]  \hspace{1cm} (4.75)

Figure 4.50 shows a transient plot of the output voltage in range 1 and the settling time is 10.6\mu s. The final 1\% settling times for Force Current mode are listed in Table 4.14

![Figure 4.50: Force Current Transient Range 1.](image)

<table>
<thead>
<tr>
<th>specification</th>
<th>value</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force Current Settling Time to 1%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1, 2000pF \parallel 125\Omega load</td>
<td>11</td>
<td>\mu s</td>
</tr>
<tr>
<td>Current Range 2, 2000pF \parallel 5k\Omega load</td>
<td>46</td>
<td>\mu s</td>
</tr>
<tr>
<td>Current Range 3, 2000pF \parallel 50k\Omega load</td>
<td>500</td>
<td>\mu s</td>
</tr>
<tr>
<td>Current Range 4, 2000pF \parallel 500k\Omega load</td>
<td>5</td>
<td>ms</td>
</tr>
<tr>
<td>Current Range 5, 2000pF \parallel 2.5M\Omega load</td>
<td>23</td>
<td>ms</td>
</tr>
</tbody>
</table>
4.5 Final Settling Times

Now that the PMU has been stabilized in every mode of operation the final settling times will be compared to the design targets in tables 4.15, 4.16, 4.17 and 4.18 respectively.

Table 4.15: Measure Voltage Settling Time.

<table>
<thead>
<tr>
<th>specification</th>
<th>target</th>
<th>final</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measure Voltage Settling Time to 1%</td>
<td>1</td>
<td>0.5</td>
<td>µs</td>
</tr>
<tr>
<td>$V_{DUT}$=5V Step, 30pF Load</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.16: Force Voltage Settling Times.

<table>
<thead>
<tr>
<th>specification</th>
<th>target</th>
<th>final</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force Voltage Settling Time to 1%</td>
<td>50</td>
<td>10</td>
<td>µs</td>
</tr>
<tr>
<td>$V_{IN}$=5V step, $C_{DUT}$ = 2nF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1, 2000pF load</td>
<td>50</td>
<td>15</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 2, 2000pF load</td>
<td>75</td>
<td>30</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 3, 2000pF load</td>
<td>250</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 4, 2000pF load</td>
<td>750</td>
<td>450</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 5, 2000pF load</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.17: Measure Current Settling Times.

<table>
<thead>
<tr>
<th>specification</th>
<th>target</th>
<th>final</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measure Current Settling Time to 1%</td>
<td>5</td>
<td>1</td>
<td>µs</td>
</tr>
<tr>
<td>$I_{DUT}$ = 0.5FSR step, 30pF load</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1, 2000pF load</td>
<td>5</td>
<td>2</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 2, 2000pF load</td>
<td>25</td>
<td>12</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 3, 2000pF load</td>
<td>250</td>
<td>120</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 4, 2000pF load</td>
<td>750</td>
<td>525</td>
<td>µs</td>
</tr>
<tr>
<td>Current Range 5, 2000pF load</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 4.18: Force Current Settling Times.

<table>
<thead>
<tr>
<th>specification</th>
<th>target</th>
<th>final</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Force Current Settling Time to 1% ( V_{IN} = 2.5V ) step, ( C_{DUT} = 2nF )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Range 1, 2000pF</td>
<td></td>
<td>125Ω load</td>
<td>50</td>
</tr>
<tr>
<td>Current Range 2, 2000pF</td>
<td></td>
<td>5kΩ load</td>
<td>50</td>
</tr>
<tr>
<td>Current Range 3, 2000pF</td>
<td></td>
<td>50kΩ load</td>
<td>500</td>
</tr>
<tr>
<td>Current Range 4, 2000pF</td>
<td></td>
<td>500kΩ load</td>
<td>5</td>
</tr>
<tr>
<td>Current Range 5, 2000pF</td>
<td></td>
<td>2.5MΩ load</td>
<td>25</td>
</tr>
</tbody>
</table>

All values are within the design targets and this completes the design of the PMU.
Chapter 5

Conclusion

5.1 Design Summary

This thesis presented a design approach to a PMU and integration of the PMU onto the same IC as a 600MHz DCL. PMUs are an integral part of many Automated Test Equipment (ATE) systems and a design approach to such circuits is a valuable tool to minimize design time by reducing the number of design iterations. As in any closed loop system there is a trade off between DC accuracy and settling times. This is because more accurate DC measurements require larger open loop gains which in turn requires more compensation to stabilize the system.

While PMUs have a large number of DC specifications, in many applications the most important specification is the nonlinearity of the forced and measured voltages and currents, and this work focused on this DC specification. In order to predict the nonlinearity in each mode of operation a previously developed model of an amplifier’s nonlinear open loop gain was introduced. This model was then used to determine the minimum value of the amplifier’s open loop gain to achieve a desired nonlinearity. Measure Voltage mode was analyzed first and a two stage CMOS amplifier was designed that met the targeted nonlinearity specification. Force voltage mode was then analyzed and a single stage bipolar amplifier was designed to meet the targeted nonlinearity specification. Measure Current and Force Current modes were then analyzed, and it was determined that the two amplifiers designed for Force and Measure Voltage modes satisfied the targeted nonlinearity in Force and Measure Current modes. This allowed the entire PMU to be designed using two amplifiers if the system could be adequately stabilized.

The only AC specification of concern in a discrete PMU is the settling time of the forced and measured voltages and currents. Since this PMU was integrated onto the same IC as a 600MHz Driver, Comparator and Active Load (DCL), its effects on the other circuits had to be considered. The DCL specification that is often most sensitive
to the integration of the PMU is the Comparator bandwidth. Any capacitance that the
PMU adds to the main IO pin of the DCL will limit the bandwidth of the test path.
It was determined that in order to measure rise and fall times accurately to within
5%, the bandwidth of the Comparator had to be at least 3 times the bandwidth of
the signal being measured. This placed an upper limit on the output capacitance of
the PMU. When the PMU is a discrete component its output capacitance is isolated
from the test path using a mechanical relay. This thesis introduced design techniques
to reduce the output capacitance of the PMU to 1pF, thus allowing its integration onto
the DCL. Settling times for the forced and measured voltages and currents are also
important parameters as they determine the minimum time required to make an accurate
measurement. Therefore, design targets were listed and design trade offs were made to
meet the targets.

Since this PMU was a negative feedback system with a wide dynamic range, com-
ensation was required to stabilize the various loops. In order to determine the necessary
compensation, the loop gain of the circuit was analyzed in each mode of operation while
approximating the force and measure amplifiers as first order systems. The necessary
location of the circuit poles and zeros for stability was then determined. The theoretical
phase and gain margins were then compared to circuit simulations.

In Measure Voltage mode it was sufficient to stabilize the measure amplifier by
itself as its stability did not depend on the stability of the other loops. However, if
the measure amplifier was over compensated it could cause instability in Force Voltage
operation as its transfer function appeared in the loop gain of Force Voltage operation.
If the measure amplifier was over compensated, its pole appeared close to the loop gain
crossover frequency in Force Voltage operation and would cause the PMU to oscillate.

Compensating the Force Voltage loop was more difficult because the sense resistor
increased the output impedance of the Force loop. This output impedance formed a
pole with the load capacitance which could be as high as 2nF. Simple dominant pole
compensation of the force amplifier was used to compensate the PMU in range 1, since
its sense resistor was only 12.5Ω. However, if dominant pole compensation were used in
the lower current ranges it resulted in extremely long settling times. This was because
a larger compensation capacitor was needed which decreased the slew rate of the force
amplifier. Therefore, a form of lead compensation was used that introduced a zero into
the loop gain. This zero acted to cancel the pole created by the sense resistor and load
capacitance.

Measure Current mode could use the same compensation used in Measure Voltage
mode, because it drove the same load capacitance and the closed loop gain was larger
than the closed loop gain of unity in Measure Voltage mode.

In Force Current mode the inclusion of the instrumentation amplifier in the feedback
path increased the open loop gain of the circuit and also introduced another pole into
the system as compared to Force Voltage operation. Both of these factors decreased circuit stability. Therefore, it was necessary to introduce another zero into the system to cancel the phase of the pole added by the instrumentation amplifier. After the design was complete the final settling times were compared to the design targets and all targets were met.

5.1.1 Future Work

Although this work focused on designing a PMU to meet a targeted nonlinearity specification, there are other DC specifications that PMUs must meet. The common mode rejection ratio (CMRR) of the measure current path is a very important DC parameter as it determines the PMU’s ability to accurately measure a current over a wide DUT pin voltage deviation. Although the amplifiers used in the design had a CMRR greater than 100dB, if the resistors that formed the gain network had greater than a 0.015% mismatch the measure current circuit would have a CMRR less than 80dB. Force Voltage and Force Current output compliance are also important parameters as they determine how accurately the PMU can force a voltage over a wide output current range or force a current over a wide output voltage range. Finally, gain and offset temperature coefficients are also important parameters as they determine how accurately the PMU can force and measure voltages and currents over a given temperature range. All of these specifications must be addressed either by design techniques or fabrication process options.

As the speed of electronic devices increases the speed of the Pin Electronics used to test them must also increase. Many high speed bipolar processes do not have high voltage MOS devices as a process option. This can severely limit the use of CMOS transmission gates as switches and this will likely require a more complex PMU architecture.
Appendix A

Isolating Capacitance

An effective technique for isolating capacitance from a node is to place a resistor in series with the capacitor as shown in figure A.1. The resistor reduces the current that flows into the capacitor which effectively reduces the capacitance seen by the signal \( v_i(t) \). The input waveform \( v_i(t) \) is a ramp function with a slope of \( \frac{d}{dt}(v_i(t)) \) during its transition. This slope is a constant and will be referred to as \( \frac{dV_i}{dt} \). The waveform can be expressed quantitatively as

\[
v_i(t) = \begin{cases} 
  \frac{dV_i}{dt} & 0 < t \leq t_2 \\
  v_2 & t > t_2
\end{cases}
\]  

(A.1)

where \( t_2 = v_2 \frac{dt}{dV_i} \). It is advantageous to express this voltage in the \( s \) domain by taking the Laplace Transform of equation A.1 which gives

\[
V_i(s) = \frac{dV_i}{dt} \left( \frac{1}{s^2} - \frac{e^{-s t_2}}{s^2} \right)
\]  

(A.2)
The voltage across the capacitor can be determined by voltage division which yields

\[ V_c(s) = V_i(s) \frac{1}{1 + s\tau} \]  

(A.3)

where \( \tau = RC \). The current that flows through the capacitor is equal to the current that flows through the resistor which gives

\[ I_c(s) = \frac{V_i(s) - V_c(s)}{R} = V_i(s) \frac{\tau}{R} \frac{s}{1 + s\tau} = V_i(s) \frac{sC}{1 + s\tau} \]  

(A.4)

Taking the inverse Laplace Transform of equation A.4 gives

\[ i_c(t) = C \frac{dV_i}{dt} \left( \left(1 - e^{-t/\tau}\right) - \left(1 - e^{-\left(t - t_2\right)\frac{\tau}{\tau}}\right)u(t - t_2) \right) \]  

(A.5)

The capacitor current will reach its maximum value when \( t = t_2 \). Substituting this into equation A.5 gives

\[ I_{c_{\text{max}}} = i_c(t_2) = C \frac{dV_i}{dt} \left(1 - e^{-\frac{t_2}{\tau}}\right) \]  

(A.6)

The effective capacitance seen by \( v_i(t) \) is

\[ C_{\text{eff}} = \frac{I_{c_{\text{max}}}}{\frac{dV_i}{dt}} = C \left(1 - e^{-\frac{t_2}{\tau}}\right) \]  

(A.7)

Recalling that \( \tau = RC \) equation A.7 can be solved for \( R \) given a desired \( C_{\text{eff}} \) which gives

\[ R = -\frac{t_2}{\ln(1 - \frac{C_{\text{eff}}}{C})C} \]  

(A.8)
Bibliography


