Phase unwrapping using Reconfigurable Hardware


This work was supported in part by Gordon-Carnegie using Reconfigurable Hardware CenterSSIS, the Bernard M. Gordon Center for Subsurface Sensing and Imaging Systems, under the Engineering Research Centers Program of the National Science Foundation (Award Number EEC-9986821).

Goal
Accelerate the performance of the minimum L Norm phase unwrapping algorithm using Field Programmable Gate Arrays (FPGAs)

Abstract
The most computationally intensive part of the minimum L^0 norm phase unwrapping algorithm[1] (its kernel) is the 2D Discrete Cosine Transform (DCT) that computes the variable p in the equation Qpcm using the Proconditioned Conjugate Gradient (PCG) method. The separability of the DCT means that the 2D transform can be decomposed into a series of 1D DCTs that can be implemented in the rows followed by the transforms of the columns. Furthermore, the DCT can be expressed in terms of a Fast Fourier Transform (FFT), which allows the hardware implementation to use a pre-designed FFT core. This paper presents a design that implements the 1D DCT on a Xilinx FPGA that is part of the Wildstar II Pro board.

This implementation performs 1D DCTs on large block sizes using a block floating point format. The DCT was designed to use fewer resources than other popular approaches due to the large point sizes supported which would otherwise consume all available chip area, but at the cost of higher latency. This latency is similar to that required for an identical sized FFT. A 512-point DCT has been shown to take 1771 cycles or 13.3 us at 133 MHz compared to a similarly sized FFT that takes 1757 cycles or 13.2 us (including full data load and unload times).

Reconfigurable Hardware
In order to fully exploit the parallelism exposed in the algorithm, a sufficiently large FPGA with multiple banks of off-chip SRAM is needed. The Wildstar II Pro was selected as the reconfigurable solution that fulfills all these requirements.

Features of the WILDSSTAR™-II PRO/PCI boards:
• Uses two Xilinx® Virtex-II PRO™ FPGAs XC2V70 (33088 slices and 5904Kb BlockRAM)
• 12 ports of DDR II SRAM totally 48MBytes, 2 ports of DDR SDRAM totally 256MBytes
• 11 GBytes/sec memory bandwidth

Algorithm
The procedures for implementing a DCT vary depending on the direction of the transform. For the forward transform:
1) Form a shuffled sequence s from the input x.
2) Take the DFT of s to get V.
3) Multiply s(k) by 2 exp(jπk/2N).
The real part of V(k) is the imaginary part of the negative of the other.

The next step is to apply the 1D DCT on image data and to gauge the performance and quality of the results.

Reconfigurable Hardware

Conclusions and Future Work
The implementation of the algorithm originally presented by Makhou [3] was implemented on an Annapolis Wildstar II Pro and the results are discussed and found to have various attractive properties for larger transform sizes. These are:
• Deterministic overhead compared to an FFT
• Use of FFT core: Design performance is based on it. Large variety available with different tradeoffs.
• Small area requirements: Larger transforms possible

The next step is to apply the 1D transform to a 2D DCT on image data and to

Components

FFT
• 24 bit, block floating point
• BlockRAM storage for twiddle factor storage
• Sub 13 us minimum latency for 512 point transform, 1757 cycle latency.
• Radix-4, supports both forward and inverse transforms.
• Run-time configurable transform length

Sine Cosine
• Complex multiplication handles rotation of input.
• Dataflow shown in Fig. 2.
• Total latency of 10 cycles

Results

Dataflow
Based on the above breakdown, the design was decomposed into the components displayed to the right. The dataflow is indicated by the arrows and is handled by a controller (not shown).

The two operations are closely related allowing for the reuse of much of the functionality. This reduces design area at the cost of added complexity for the controller.

Optical Quadrature Microscopy
Optical quadrant microscopy[3] was developed in 1997 based on techniques developed for coherent laser radar. A single coherent laser beam is split into two paths, one a reference and the other a signal path that passes through the sample under examination. Interference patterns are then captured by CCD cameras. Although the images could be taken with only two cameras, four are used to completely capture the entire signal including the conjugate intensities.

Differential Interference
Contrast
Ep-Fluorescence
Optical Quadrature Microscopy

Keck 3D Fusion
Microscope
• Differential Interference Contrast
• Ep-Fluorescence
• Optical Quadrature Microscopy
• Confocal Reflection & Fluorescence
• Two-Photon

After the interference fringe pattern is taken, four further steps must be undertaken to produce the final image:
1) Phase unwrapping: Assigns integer multiples to the phase values
2) Term elimination: Mathematical removal of setup irregularities
3) Phase evaluation: Produces a phase-map from the spatial distribution of the phase
4) Rescaling: Converts phase to another criteria such as distance

References

This work is a part of the CenSSIS BioBed effort under R1, R3 and S1. Calculating the minimum L^0 norm phase unwrapping takes several minutes per frame to process. This prevents the streaming of live video data from the microscope. Our goal is to develop a hardware/software implementation of phase unwrapping to achieve near real-time performance.